MULTI CYCLE PIPELINED RISCv BASED PROCESSOR

1. Introduction

This document outlines the specifications for the design and implementation of a multi-cycle pipelined RISC-V based processor.

2. Objectives

- Develop a multi-cycle 5 stage pipelined processor
- Implement and verify the functionality of below ALU operations
    a. ADD
    b. SUB
    c. AND
    d. OR
    e. XOR
    f. NOP
- For each operation implement the corresponding instruction of RISCv
- Also write the testbench to verify the working of the processor

3. Instructions format

OPERATION	FUNC7 (7BITS)	RS2 (5BITS)	RS1 (5BITS)	FUNC3 (3BITS)	RD (5BITS)	OPCODE (7 BITS)
ADD	0000000	01001	01000	000	00110	0110011
SUB	0100000	10010	10011	000	00111	0110011
AND	0000000	01111	01110	110	10001	0110011
OR	0000000	01101	01100	111	11111	0110011
XOR	0000000	10111	10110	100	11100	0110011

Note: The above register addresses are given for reference and can be altered in the project as required.

4. Pipelining stages

The processor pipeline will be divided into five stages:

1. Instruction Fetch (IF): Fetches the instruction from memory.
2. Instruction Decode (ID): Decodes the instruction and reads the necessary registers.
3. Execute (EX): Performs the ALU operations.
4. Memory Access (MEM): (If needed, but generally bypassed for ALU operations).
5. Write Back (WB): Writes the result back to the register file.