SASTRA
DEEMED TO BE UNIVERSITY

School of Computing
Second CIA Test –September 2019
Course Code: CSE 105
Course Name: Computer Organization
Duration: 90 minutes
Max Marks: 50

2/3 12-4

PART A

Answer all the questions (10 x 2 = 20)

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1. How to calculate branch target address in the datapath?
2. Illustrate the mechanism involved in generating ALU control input.
3. List the methods to improve the throughput of the processor.
4. Classify the hazards in the pipeline based on its recoverable nature and justify.
5. When will the forwarding method fail and give a suitable example?
6. Which control signals involved in the execution stage of pipelined datapath?
7. Construct five-stage pipeline with the graphical representations for the given instruction
   lw $10, 20 ($1)
8. Identify the dependencies in the following instruction sequence and detect the possible hazards
   sub $2, $1, $3
   and $12, $2, $5
   or $13, $6, $2
9. What is loop unrolling?
10. Define hit time and miss penalty.

PART B

Answer any three questions (3 x 10 = 30)

11. Construct the MIPS datapath neatly with all the control signals and explain the operation of branch-on-equal instruction by high lighting the active blocks in that datapath.

12. What is branch penalty? Explain in detail about the available handling methods to reduce it.

13. a) Summarize the concept of spe[illegible]ion. (3)

b) Compare static and dynamic multiple-issue processors. (3)

c) Model the architecture for dynamically scheduled pipeline and explain how dynamic pipeline scheduling is done? (4)

14. a) Classify the memories based on speed, access time, size, cost, technology and arrange them in hierarchical order. (4)

b) Given this instruction sequence,

50_{hex} sub $1, $12, $14
54_{hex} and $2, $12, $15
58_{hex} or $3, $12, $16
$5C_{hex}$ add $11, $12, $11
60_{hex} slt $5, $16, $17
64_{hex} lw $6, 50($17)
...

Assume the instructions to be invoked on an exception begin like this:

50000150_{hex} sw $22, 2000($0)
50000154_{hex} sw $23, 2004($0)
....

If an overflow exception occurs in the add instruction, answer the following:

i) Deduct the clock cycle at which the exception will be tak into pipeline (assume instruction at 50_{hex} address fetched CC1)? (2

ii) Interpret the PC register value during overflow and af exception? (2

iii) What happens in the pipeline registers during exception? (2

SASTRA
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School of Computing
Third CIA Test – October 2019

Course Code: CSE 105
Course Name: Computer Organisation
Duration: 90 minutes
Max. Marks: 50

PART-A

Answer all the questions (10 X 2 = 20)

1. Subtract $(11011)_2$-$(10011)_2$ using 2's complement.
2. Distinguish pipelining from parallelism.
3. Write the compiled ARM assembly code for the following C Program:

```
int leaf_example (int g, int h, int i, int j)
{
   int f;
   f=(g+h)-(i+j);
   return f;
```

4. Identify the dependencies in the following sequence of instructions.

```
sub $2, $1, $3
and $12, $2, $5
or  $13, $6, $2
add $14, $2, $2
sw  $15, 100($2)
```

5. Why is branch prediction algorithm needed?
6. What is the minimum number of cycles needed to completely execute n instructions on a CPU with a k stage pipeline? Justify your formula.
7. Differentiate virtually addressed cache and physically addressed cache.
8. What are the two characteristics of program memory accesses that caches exploit?
9. Discuss why RAID 3 is not suited for transaction processing applications. What kind of applications is it suitable for and why?
10. Find the AMAT for a processor with a 1 ns clock cycle time, a miss penalty of 20 clock cycles, a miss rate of 0.05 misses per instruction, and a cache access time (including hit detection) of 1 clock cycle. Assume that the read and write miss penalties are same and ignore other write stalls.

PART-B

Answer any two of the following (2 X 10 = 20)

11. (i) Derive an algorithm in flow chart form for non-restoring algorithm method of fixed point binary division? (6 Marks)
    (ii) Assume 185 and 122 are unsigned 8-bit decimal integers. Calculate 185–122. Is there overflow, underflow, or neither? (4 Marks)
12. Explain the hazards caused by unconditional branching statements. (10 Marks)
13. (i) How many total bits required for direct mapped cache with 16KB of data and 4-word blocks, assuming 32-bit address. (4 Marks)
    (ii) Criticize the following statement: "*Using the faster processing chip results in a corresponding increase in the performance of computer even if the main memory speed remains the same*". (6 Marks)

PART-C

Answer the following questions (1 X 10 = 10)

14. (a) Build a datapath for the operational portion of the memory reference and arithmetic-logical instructions that uses a single register file and a single ALU to handle both types of instructions, adding any necessary multiplexors. (3 Marks)
    (b) Elaborate the states involved in a simple cache controller with a neat sketch. (4 Marks)
    (c) Suppose we have a benchmark that executes in 100 seconds of elapsed time, of which 90 seconds is CPU time and the rest is I/O time. Suppose the number of processors doubles every two years, but the processors remain the same speed, and I/O time doesn't improve. How much faster will our program run at the end of six years? (4 Marks)