Self-Project

Simulation of Cascaded H-Bridge (CHB) Converter for STATCOM and Rectifier Application

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Introduction:

With the increasing demand for high-power converters and power quality improvement devices, the Cascaded H-Bridge (CHB) multilevel converter has gained wide attention. It offers advantages such as modularity, high power quality, and reduced harmonic distortion. This project focuses on the simulation of a CHB converter applied in two major areas: STATCOM (Static Synchronous Compensator) and Rectifier operation.

Objective:

- To model and simulate a CHB converter topology in MATLAB/Simulink.
- To demonstrate its performance in **STATCOM** applications for reactive power compensation.
- To evaluate its operation as a **rectifier** for AC-DC conversion.

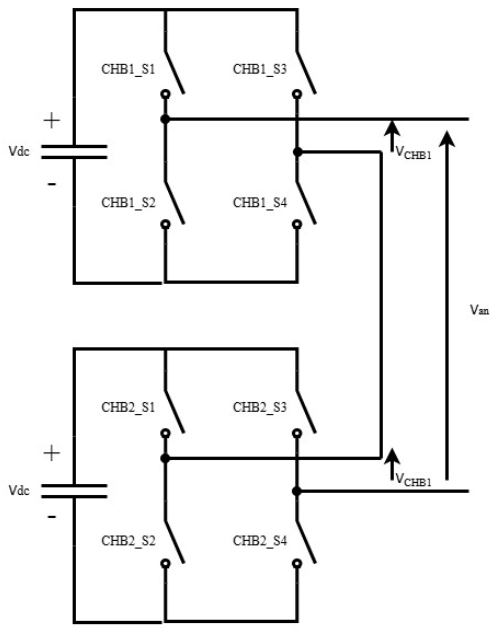
CHB Converter Topology:

Each H-bridge cell generates three voltage levels: +Vdc, 0, and -Vdc. For **n** cells per phase, the output has **2n+1** levels.

Configuration:

- Number of Phases: 3 (for STATCOM)
- Cells per Phase: 2
- No. of Voltage levels: 5
- Switches per Cell: 4
- DC Source: Isolated supply for each H-bridge

The single phase of the three phase CHB with two cells is shown in fig (1). For CHB isolated voltage source is required. For this application dc link capacitor is used. Power required to maintain constant voltage in dc link capacitor is derived form the grid itself.



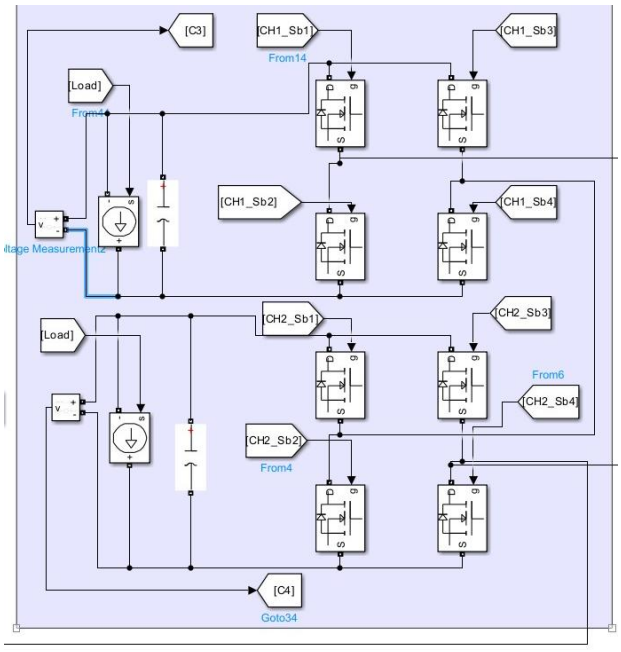


Fig 1: Two cell cascaded H Bridge

Fig 2: Two cell cascaded H Bridge Simulink implementation

In the Simulink implementation, controlled current source is connected, it acts as a load during active rectifier operation. During STATCOM operation controlled current source is not activated.

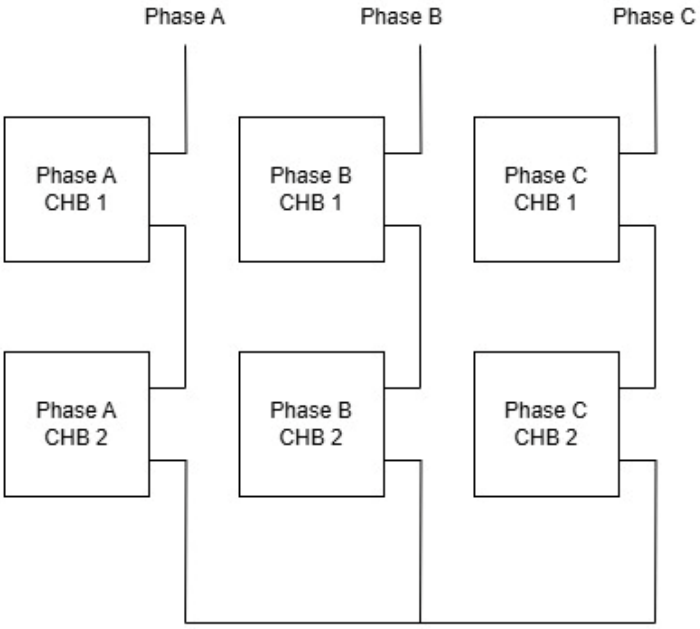


Fig 3: Cascaded H Bridge

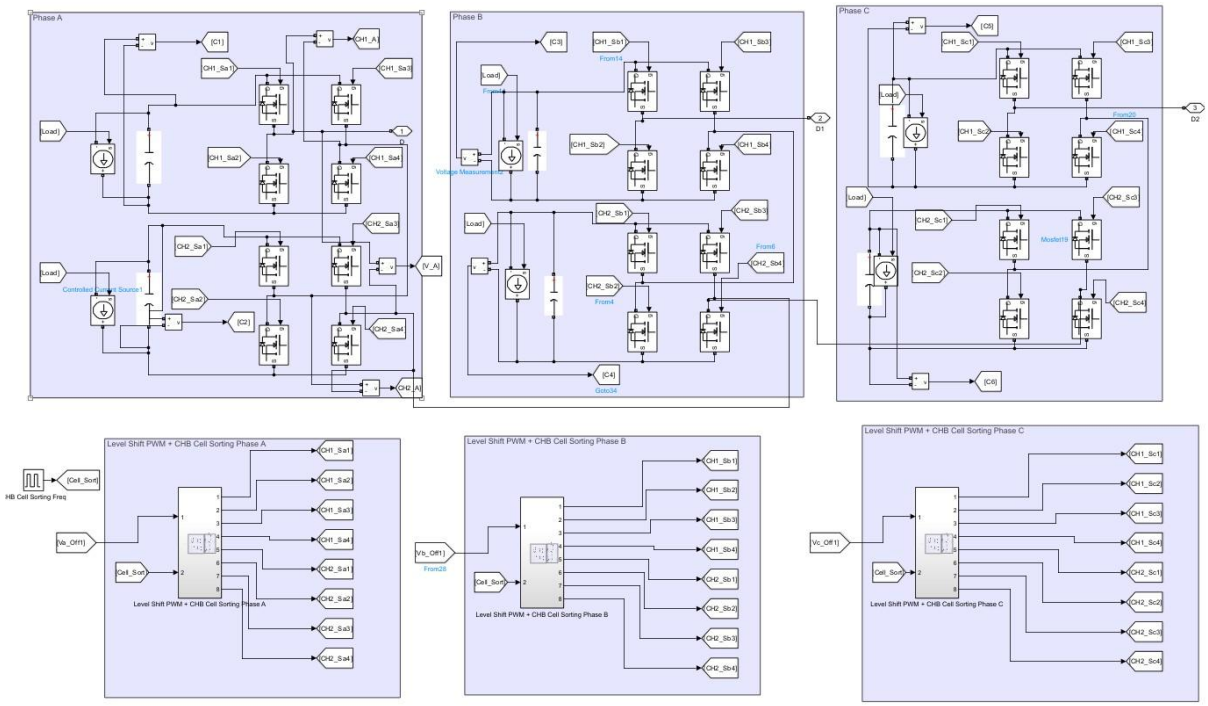


Fig 4: Three phase Cascaded H Bridge Simulink Implementation

In fig (4), the subsystem on the below shows the level shift PWM and cell sorting block.

Simulation Setup:

The converter is connected to the grid as shown in the fig (5). The grid is also connected to the AC load. The active load is supplied by the grid. The reactive load is supplied by the CHB converter.

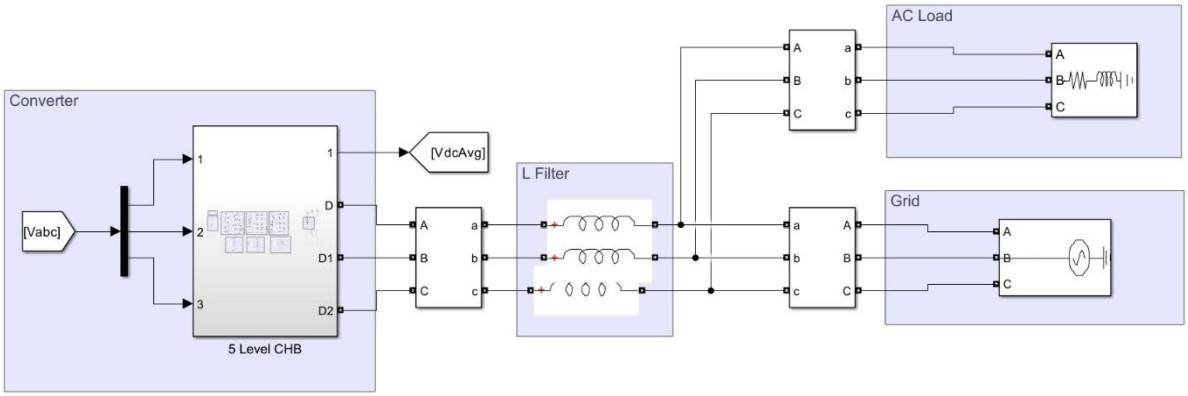


Fig. 6: Connecting Converter to the grid

The block diagram is shown in the Fig.7

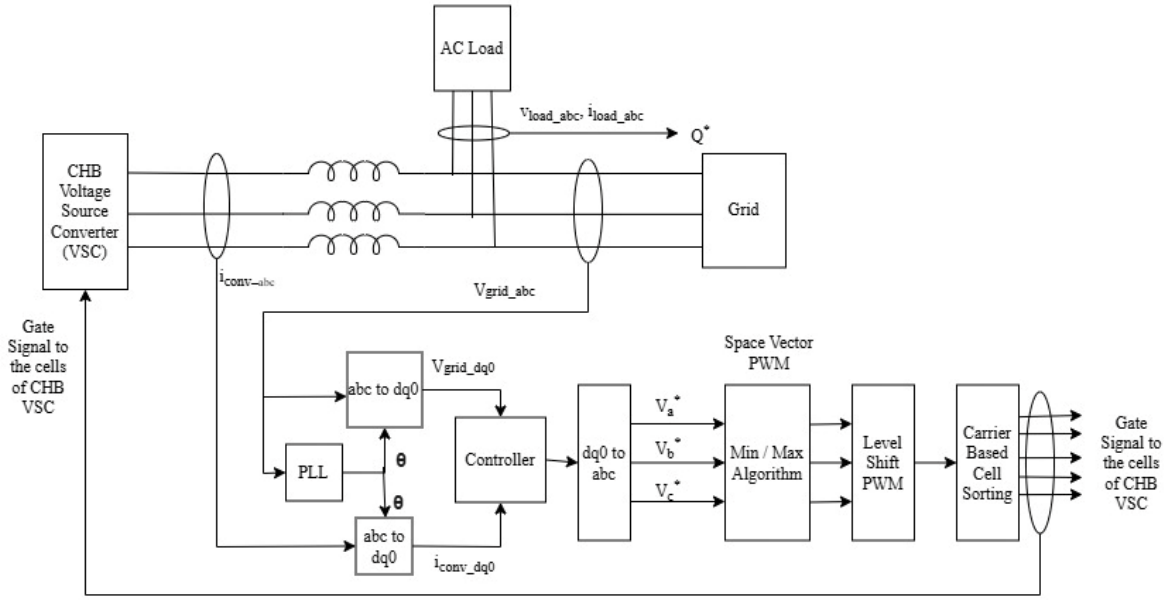


Fig. 7: Connecting Converter to the grid Block Diagram

Phase Locked Loop:

The Fig. 7 shows the overall structure for the control of the grid connected CHB. The grid voltage is measured and the synchronous reference frame is aligned to the voltage space vector. Therefore, making magnitude of the V_{grid_q} to be zero. The magnitude of the V_{grid_d} is equal to the magnitude of the grid peak voltage. This alignment of synchronous reference frame with the grid voltage space vector is achieved by taking the "θ" from the Phase Locked Loop (PLL) block. The θ is the angle at which the synchronous reference frame rotates.

Controller Implementation:

The controller block is shown in detail in Fig. 8. The reactive power to be compensated is measured from the load voltage and current. Based on the reactive power reference $i^*_{conv\_q}$ is generated. It is compared with the actual i_{conv_q}, and the error signal is given to the PI controller. When CHB VSC is acting as a STATCOM Or Active Rectifier it does not require separate dc voltage source in the dc side, dc link capacitor is enough. However, to maintain constant voltage source, active power is taken from the grid. This is achieved by comparing dc voltage reference V_{dc} with the average of all the cell voltage and the error signal is given to the PI controller. This gives the reference d-axis current for the converter ($i^*_{conv\_d}$).

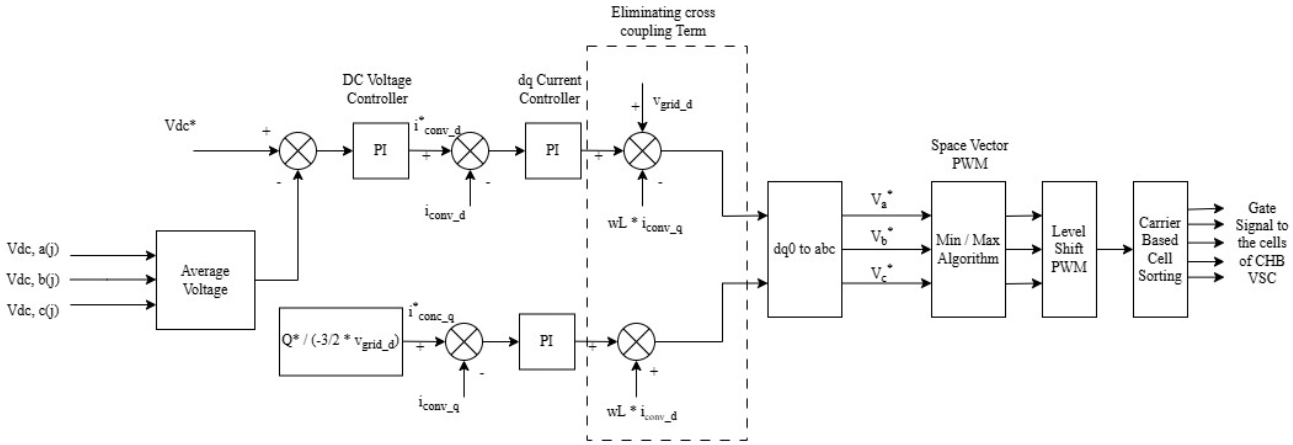


Fig. 8: Connecting Converter to the grid

The output of the dq axis current controller is add with feedforward term to nullify the cross-coupling terms in the voltage equation of the converter. The cross coupling is the inherent nature of the converter, it the effect of i_{conv_d} current on the reactive power flow and the effect of i_{conv_q} on the active power flow. It is nullified by adding the term "- $\omega L^* i_{conv\_q} + v_d$" for the d-axis current controller output. And "+ $\omega L^* i_{conv\_d}$" to the q axis current controller output. Now active power is controlled only by the d-axis current and the reactive power is controlled only by the q-axis current.

$$P_{conv} = \frac{3}{2}\left[\, v_d i_d + v_q i_q \right]$$

$$Q_{conv} = \frac{3}{2}\left[-\, v_d i_q + v_q i_d \right]$$

But, by the choice of "θ" for the synchronous reference frame, the v_q is made zero. Therefore, the voltage becomes,

$$P_{conv} = \frac{3}{2}\left[\, v_d i_d \right]$$

$$Q_{conv} = \frac{3}{2}\left[-\, v_d i_q \right]$$

The controller implementation in Simulink is shown in the Fig. 9.

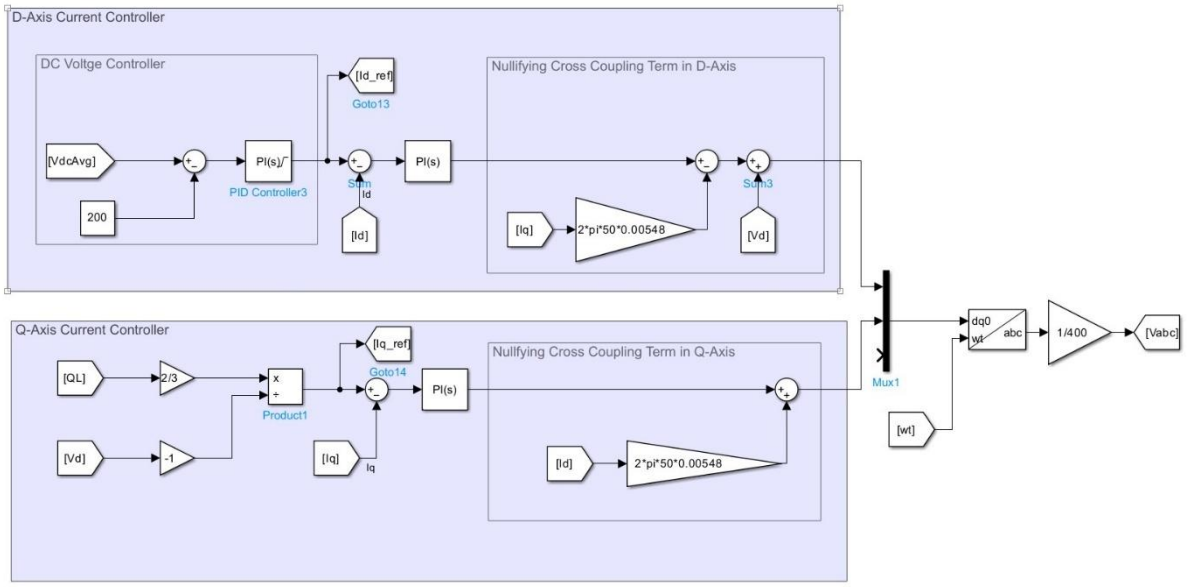


Fig. 9: Simulink Implementation of the controller Block

The obtained reference voltages in dq0 domain are converted to abc domain by reverse transformation. The obtained sinusoidal waveform is converter to Space Vector PWM by voltage Minimum and Maximum Algorithm. This done to increase the dc bus utilization by 15% more than the Sinusoidal PWM. The reference waveform developed by the controller, the Space Vector Reference PWM derived form the Min Max Algorithm and the Level shift PWM is shown in the Fig. (10).

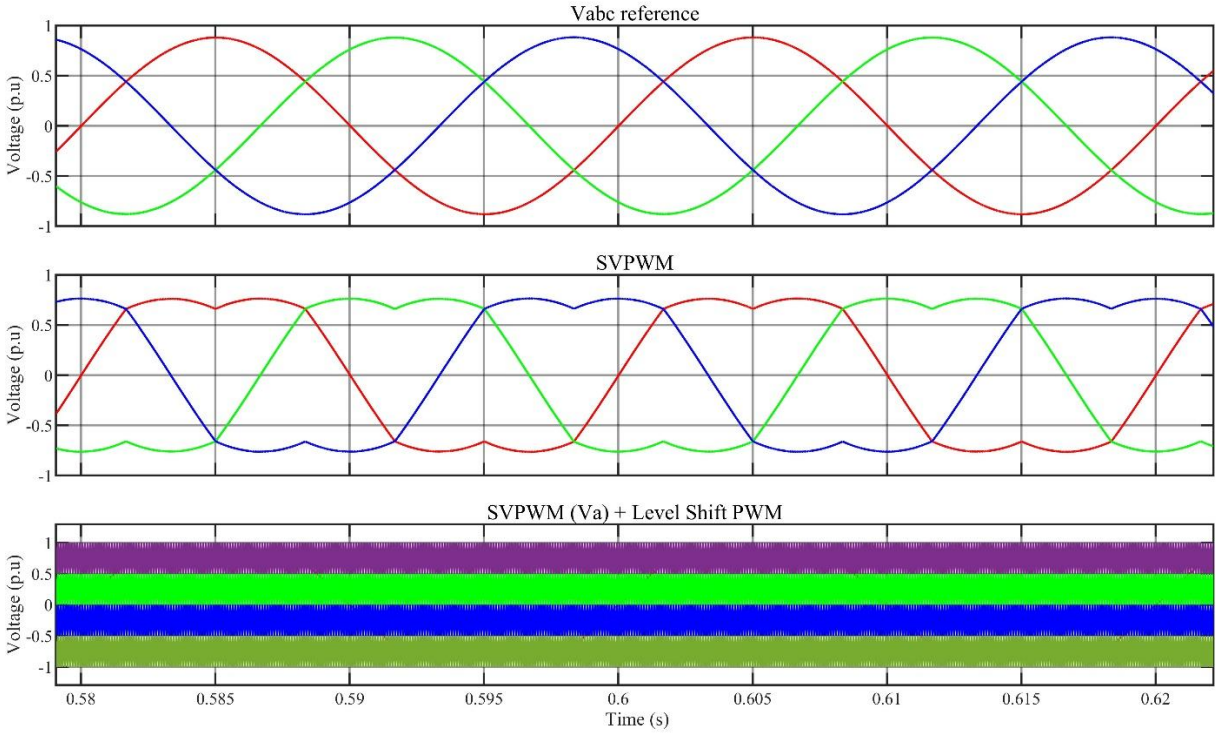


Fig. 10: (a) Sinusoidal Ref, (b) SV PWM Ref, (c) Level Shifted PWM

The gate signal generated by the Level Shifted PWM for the CHB cell 1 and cell 2 of phase is shown in the Fig. (11). The switching signal for CHB S1 and S3 switches only shown, the switches S2 and S4 is just the complement of S1 and S3 respectively.

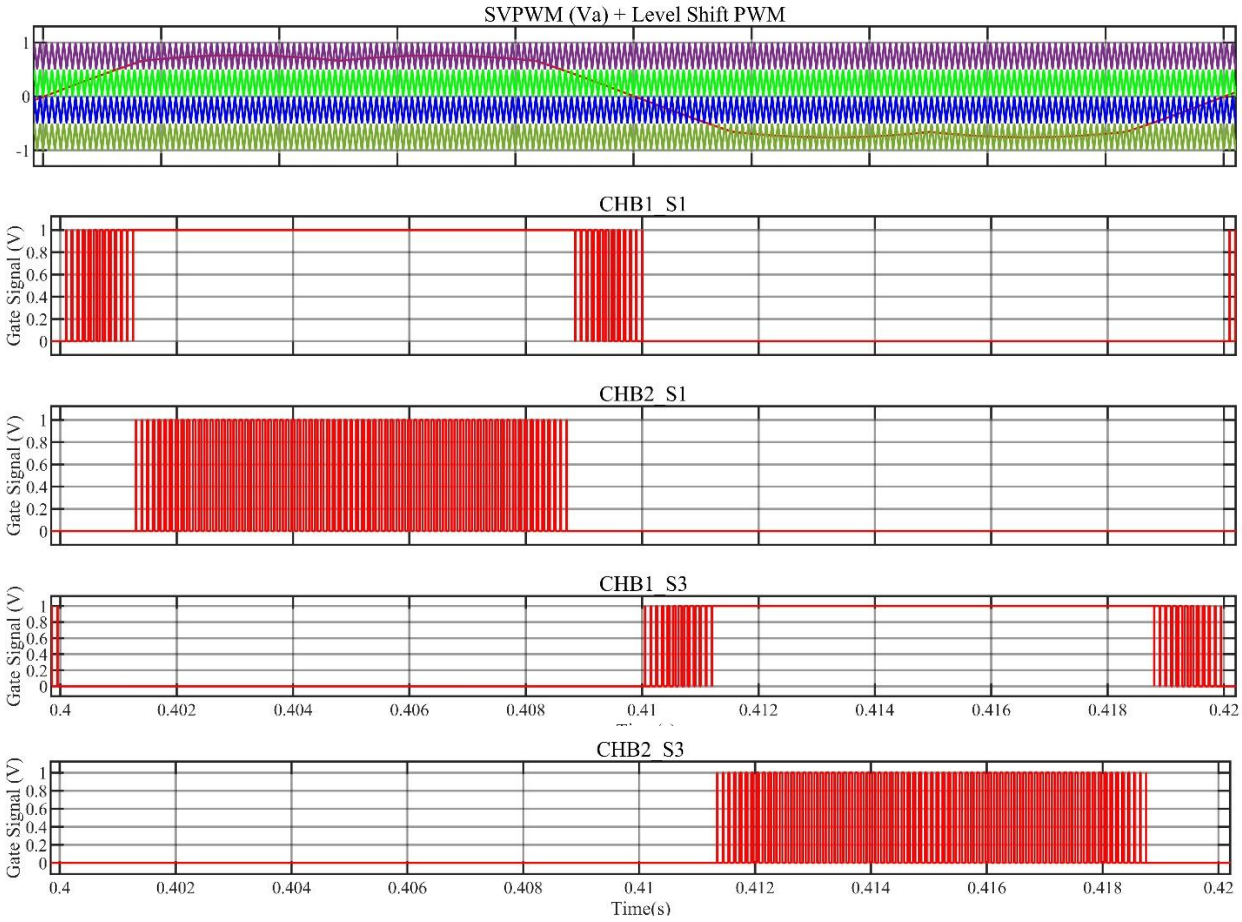


Fig. 11: (a) Level Shifted PWM, (b - e) Switching Signal of CHB1_S1, CHB2_S1, CHB1_S3, CHB2_S3

In this this type of switching the losses in the CHB cell 1 and CHB cell 2 is different. The modularity of the converter is affected and one cell may lose functionality faster than the other cell. The capacitor voltage will also get drifted due to unsymmetrical switching frequency.

The drift of capacitor voltage is shown in the Fig. (12). Here, the reference capacitor voltage is set as 200 V dc. All the cell capacitor voltage is measured and the average of 6 capacitor voltge is used to compare with the reference capacitor voltage to obtain refered d-axis current. But it cannot detect drift of voltage within each cell in the phase (One capacitor voltage increaces and the other decreases therefore the average remains constant, it can be seen from the Fig. 12). To eliminate this carrier based cell sorting Algorithm is used.

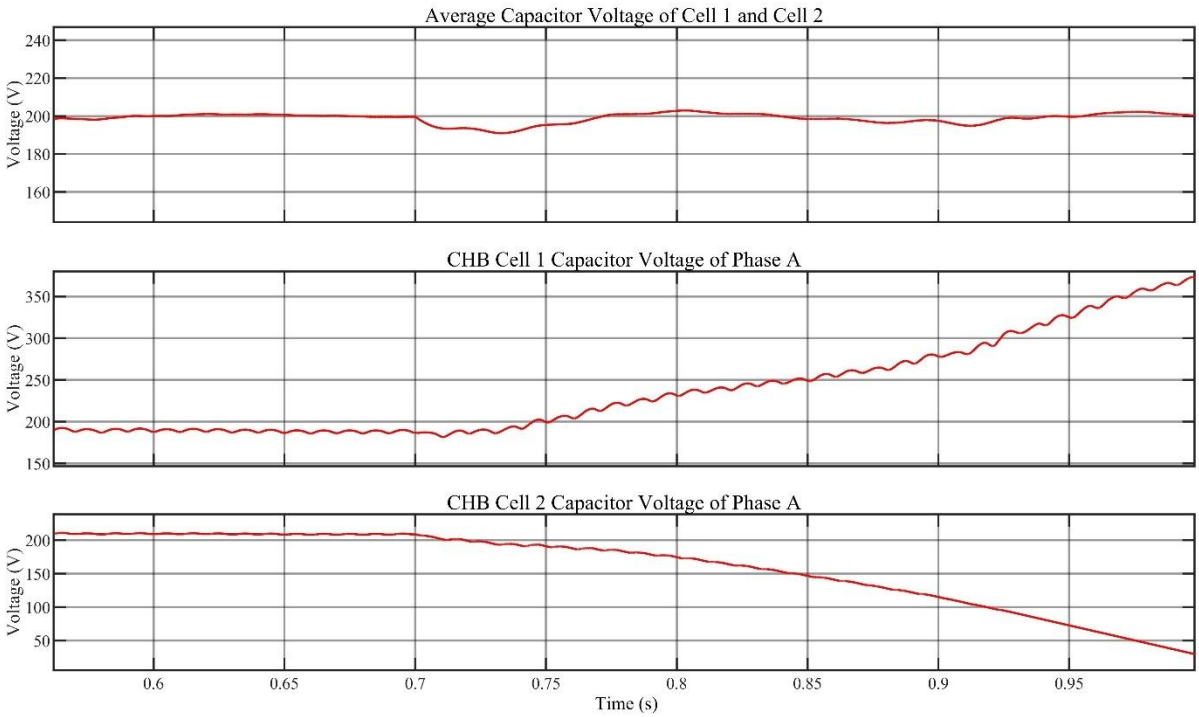


Fig. 12: (a) Average of all Cell Capacitor vol, (b) Capacitor voltage of CHB Cell1 of Phase A,

(c) Capacitor voltage of CHB Cell2 of Phase A.

Carrier Rotation Based Sorting Algorithm:

To ensure balanced switching stress across H-bridge cells in the cascaded converter, a carrier rotation-based sorting algorithm was implemented. In this method, switching conditions of individual cells are periodically varied by reassigning carrier signals.

For a converter leg with four carrier signals:

- The middle two carriers are assigned to one H-bridge cell,
- While the outer two carriers are assigned to the other.
- After a set interval, these assignments are interchanged, rotating switching stress among the cells.

Such a dynamic carrier assignment is essential in multilevel converters like CHB, where uniform thermal distribution significantly affects performance and device lifespan. The Switching signal after the Cell sorting algorithm is shown in the Fig. (14). The Simulink implementation of Level Shift PWM and Carrier Rotation Based Sorting Algorithm is shown in the Fig. (13).

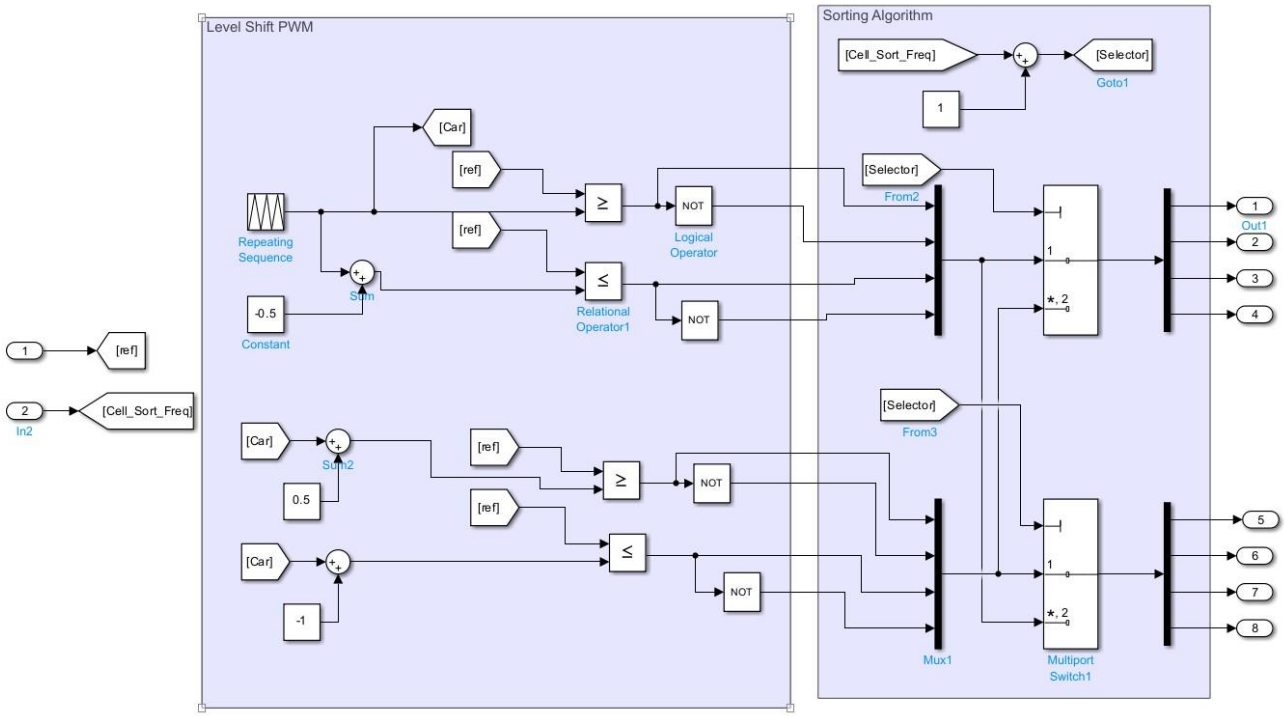


Fig. 13: Simulink Implementation of Level Shifted PWM & Carrier Rotation based sorting Algorithm in Simulink

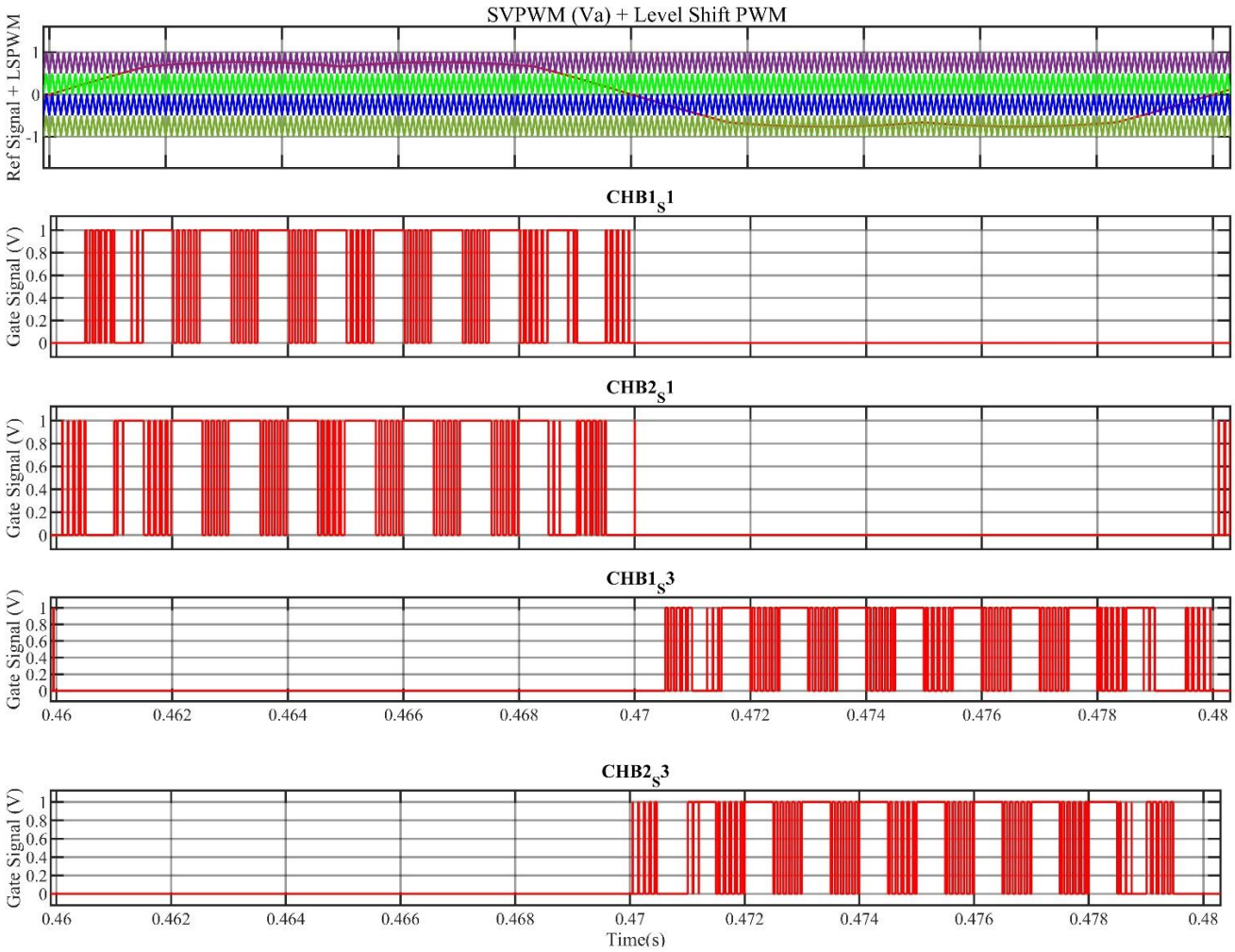


Fig. 14: (a) Level Shifted PWM, (b - e) Switching Signal of Carrier Rotation based sorter CHB1_S1, CHB2_S1, CHB1_S3, CHB2_S3

The capacitor voltage is not drifting after implementing the Carrier Rotation Based Sorting Algorithm. It is shown in the Fig. (15).

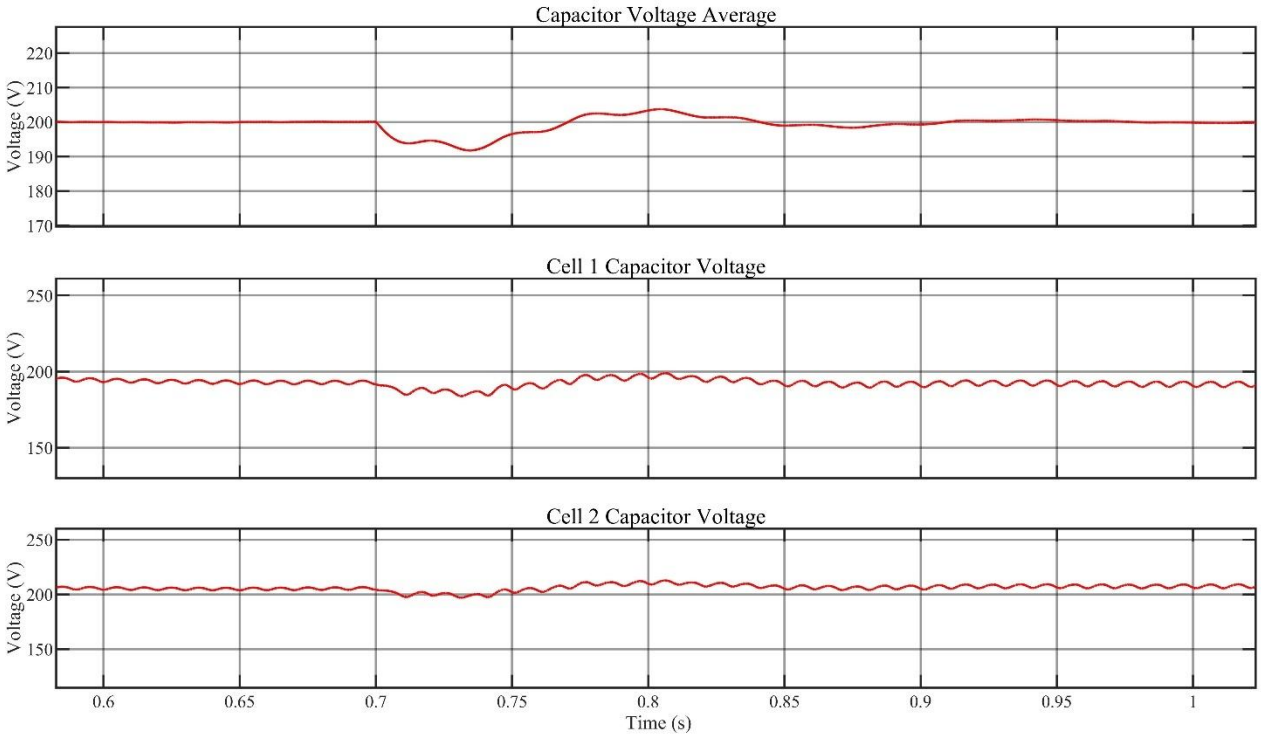


Fig. 15: (a) Average of all Cell Capacitor vol after cell Sorting,

(b) Capacitor voltage of CHB Cell1 of Phase A after cell sorting algorithm,

(c) Capacitor voltage of CHB Cell2 of Phase A after cell sorting algorithm.

Implementation of this sorting algorithm will not affect the output voltage of the converter. This can be observed for the Fig. (16 – 17). It shown each cell voltage and the phase voltage during normal implementation Fig. (16) and the Carrier Rotation Based Sorting Algorithm Implementation Fig. (17).

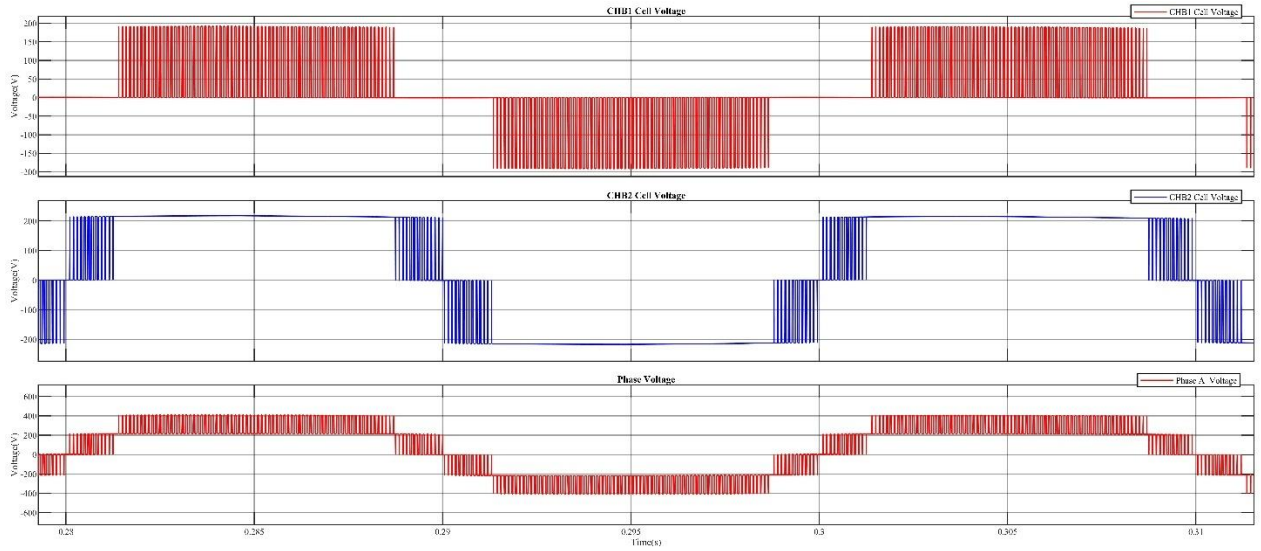


Fig. 16: (a) CHB cell 1 Voltage of Phase A, (b) CHB cell 2 Voltage of Phase A, (c) Phase A Voltage (V_{an})

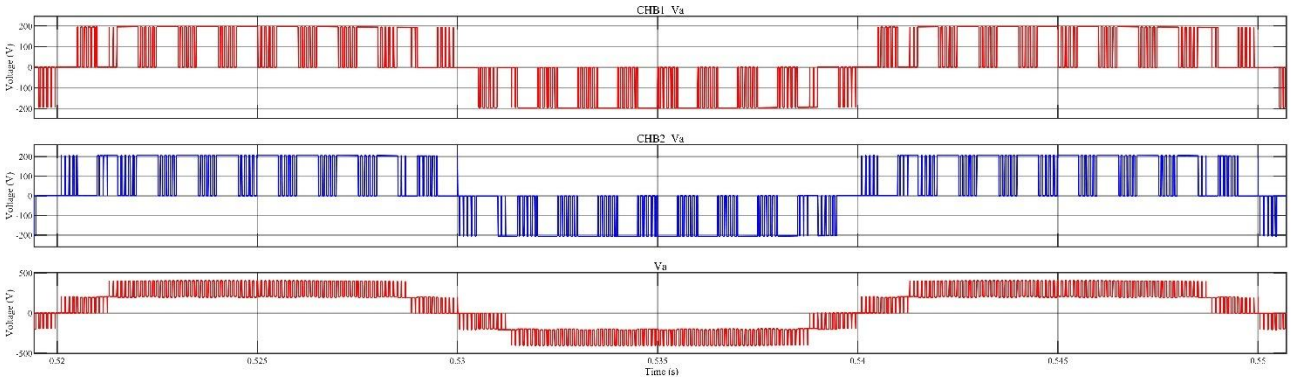


Fig. 17: After Carrier Rotation Based Sorting

(a) CHB cell 1 Voltage of Phase A, (b) CHB cell 2 Voltage of Phase A, (c) Phase A Voltage (V_{an})

STATCOM Operation:

For the STATCOM operation the reactive power required by the load is supplied by the CHB Voltage Source Converter (VSC). The Active power required by the load only is supplied by the grid. Therefore, improving the power factor of the system. During the STATCOM operation a small amount of active power is absorbed by the VSC to maintain constant DC voltage in the dc link capacitor, it is achieved by controlling the d-axis current. The Grid Phase voltage & current, the Load Phase currents, Converter Currents, Converter active and reactive power is shown in the Fig. (18).

For this simulation, the load Absorbs 4 KW active power and 4 KVar of lagging reactive power. It can be observed the grid voltages and currents are in phase therefore power factor is 1 (Unity Power factor). The Load phase current lag the grid voltage by some angle (Lagging Power factor). The converter phase current is lagging the grid voltage by the angle of 90 degree. This shows that the converter is suppling only the reactive power and the active power absorbed or supplied by the converter is negligible. The grid supplies only the active power, therefore the efficiency of the system is improved.

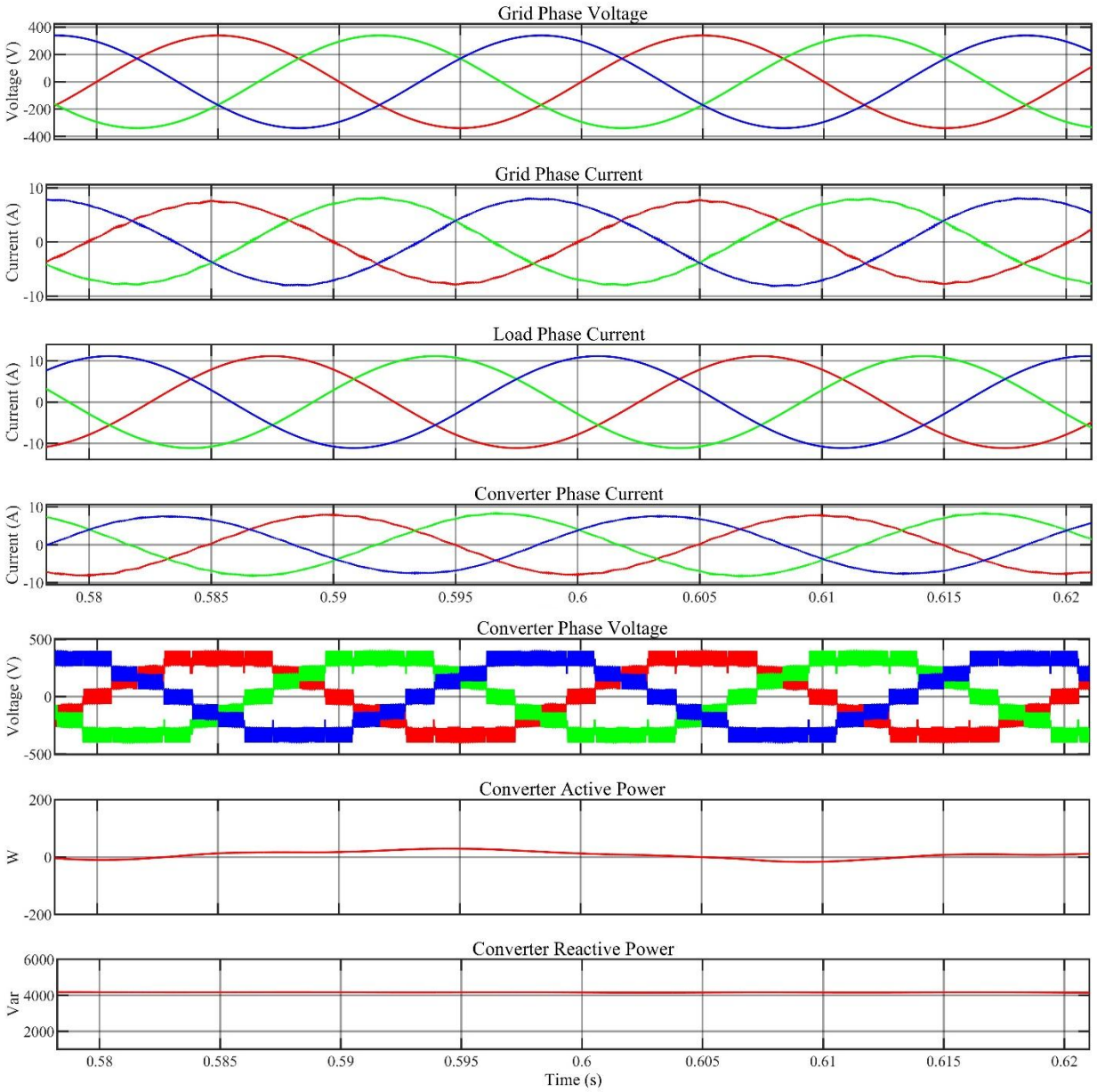


Fig. 18: (a) Grid Phase Voltage, (b) Grid Phase Current, (c) Load Phase Current, (d) Converter Phase Current, (e) Converter Phase Voltage, (f) Converter Active Power, (g) Converter Reactive Power

Active Rectifier Operation:

In Rectifier operation, the dc power is taken form the dc side of the capacitor. This is achieved by connecting the constant dc current source in reverse direction in all the six capacitors. The capacitor voltage is maintained at 200 V DC. Now the DC current taken from each capacitor is 5 A. This is shown in the Fig. (19). The power taken from single capacitor is 1 kW. Therefore, the total power taken from the dc side is 1kW * 6 = 6 kW. Due to the discharge of the capacitor the capacitor voltage will decrease, to maintain the capacitor voltage more active power will be absorbed from the grid. Therefore, achieving the Active Rectification operation.

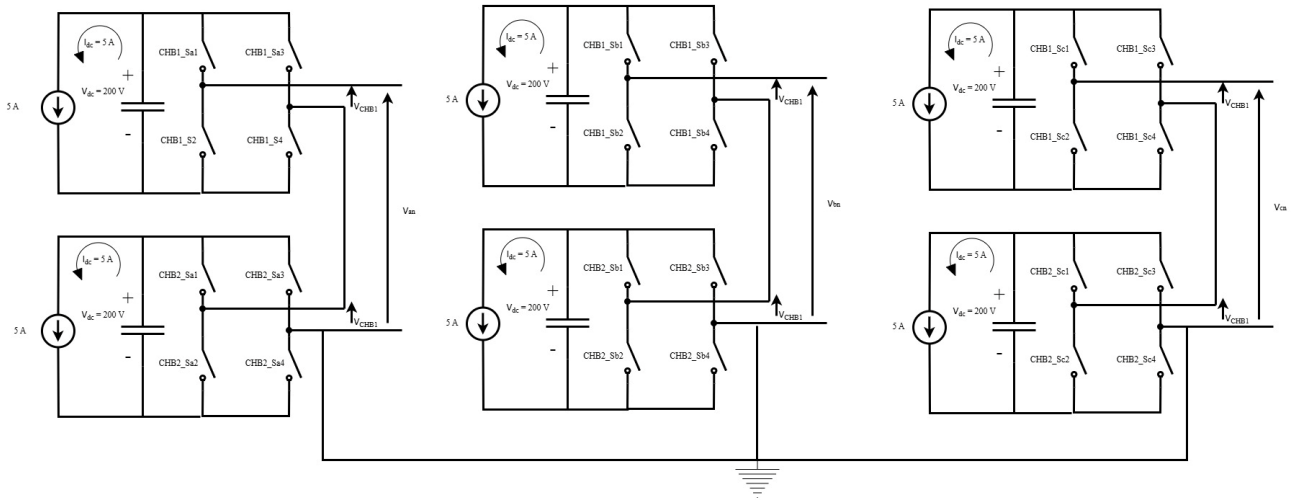


Fig. 19: Active Rectification operation Setup

During this operation the lagging load is still connected to the grid, the converter can supply reactive power and absorb active power at the same time. This is shown in the Fig. (20). The grid phase voltages and grid currents are in phase therefore unity power factor at grid. The load is absorbing the active and lagging reactive power, therefore lagging power factor. The CHB VSC additional to supplying lagging power to the grid, now it is also absorbing active power from the grid to supply the load in the dc side.

The power taken from the dc side is 6 kW, the converter is absorbing the active power of 6 kW from the grid, shown in Fig. (20). It can be observed that the reactive power of the converter is positive indicating it is supplying the reactive lagging power and the active power of the converter is negative indicating it is absorbing the active power from the grid. It is also possible to make the converter to absorb only the active power from the grid by making the $i^*_{conv\_q}$ as zero. And the converter will act as Active rectifier only.

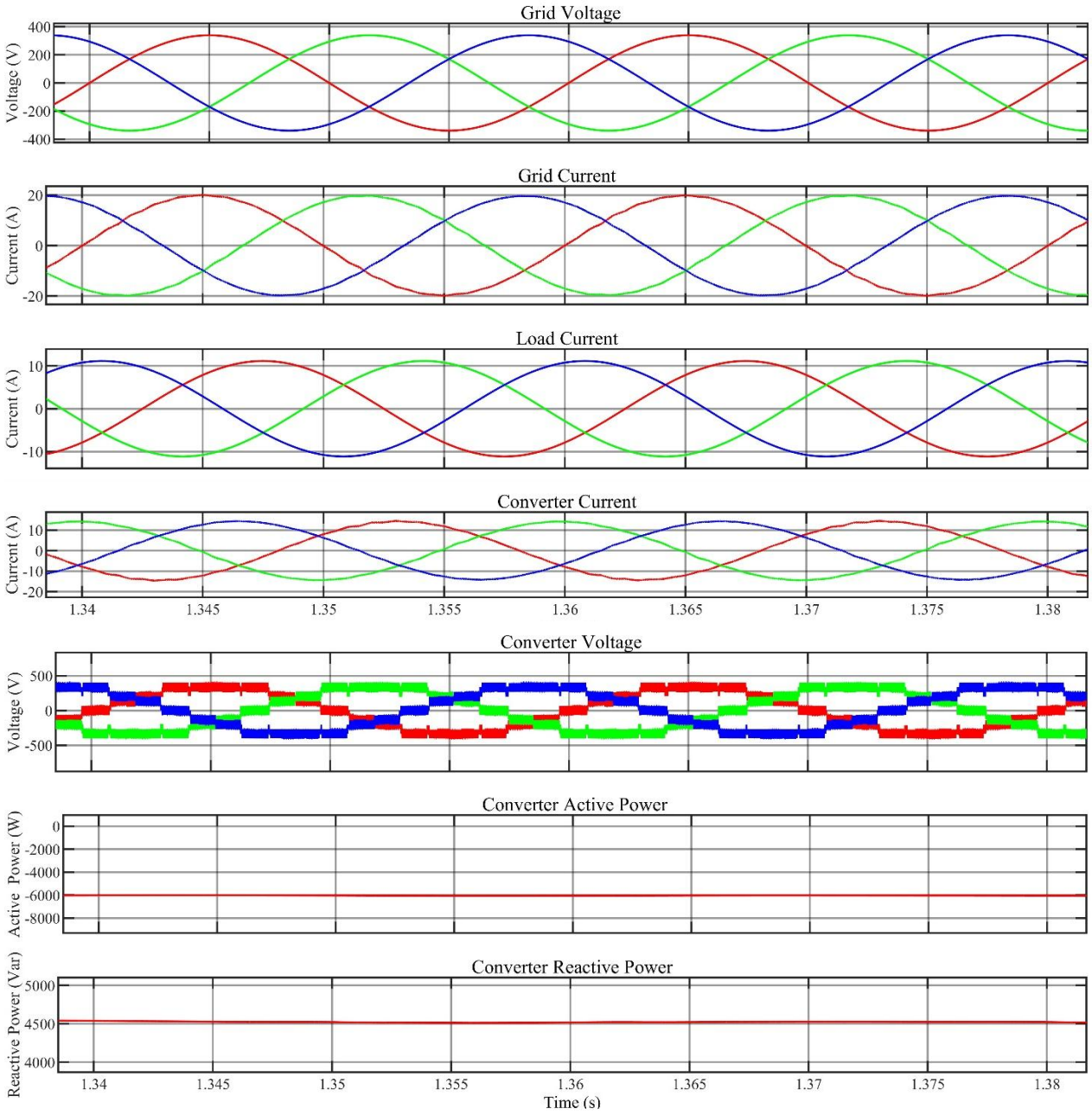


Fig. 20: STATCOM + Active Rectification operation

(a) Grid Phase Voltage, (b) Grid Phase Current, (c) Load Phase Current, (d) Converter Phase Current, (e) Converter Phase Voltage, (f) Converter Active Power, (g) Converter Reactive Power

Dynamic Performance of the VSC:

To observe the dynamic performance of the converter, up to 0.7 sec the converter is operated as a STATCOM. After 0.7 sec the power is taken form the dc side of the converter. The active and reactive power of the Grid, AC Load, Converter and Average of dc link capacitor voltages is shown in the Fig. (21). It is observed the grid is initially supplying 4 kW active power to the load, at 0.7 sec when power is taken form the dc side of the converter, the average of capacitor voltage starts

decreasing. To maintain the constant capacitor voltage active power is taken from the grid. Therefore, the active power absorbed by the converter increases and active power supplied by the grid increases. In steady state the active power required by the converter (6 kW) is supplied by the grid. Now the total active power supplied by the grid is (10 kW). Still the reactive power supplied by the grid is zero. VSC is still supplying the reactive power required by the AC load. Therefore, through the **Grid Voltage-Oriented Control** the grid connected converter is operated as both the STATCOM and Active rectifier.

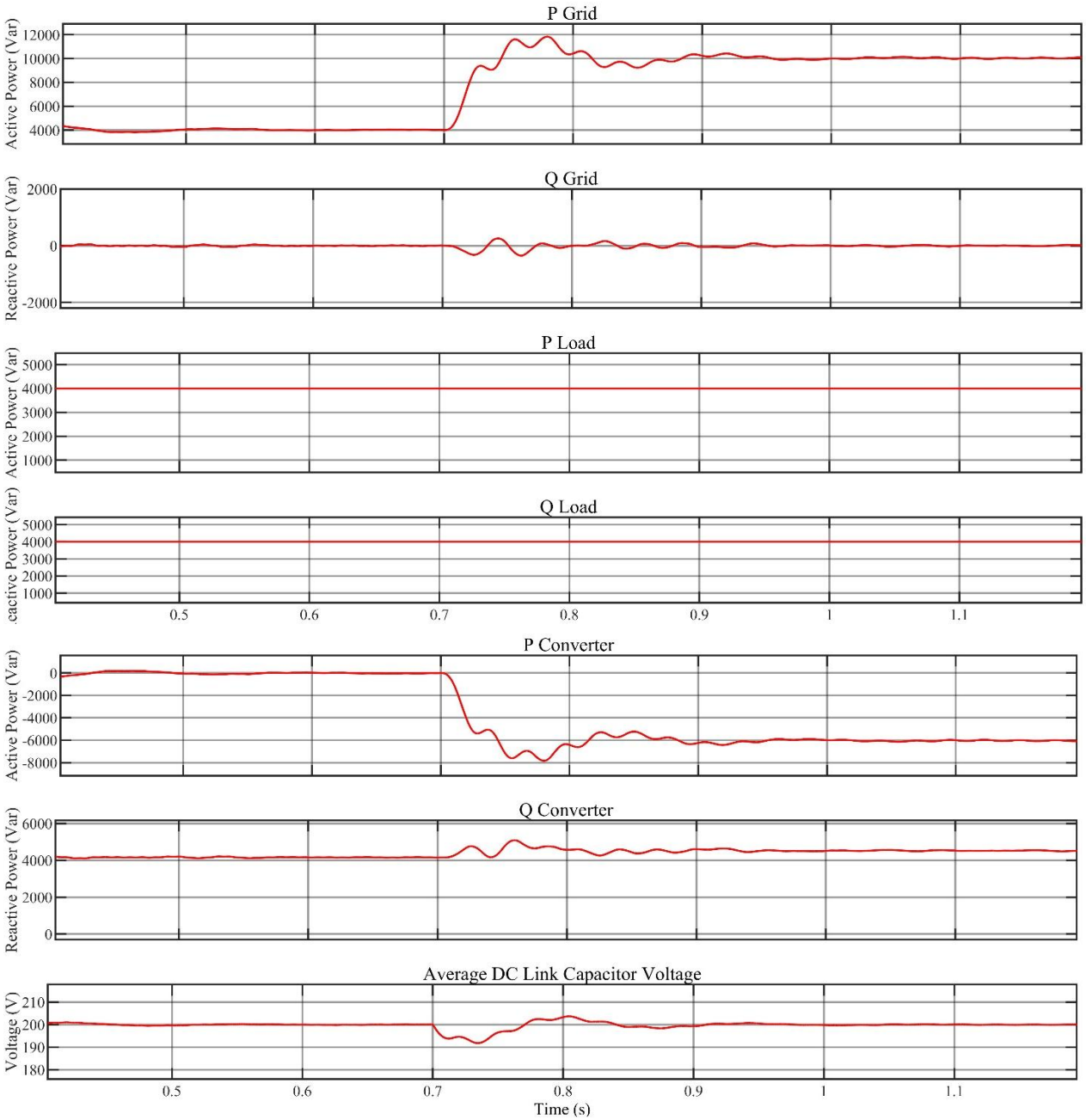


Fig. 21: (a) Active Power of Grid, (b) Reactive Power of Grid, (c) Active Power of Load, (d) Reactive Power of Load, (e) Active Power of Converter, (f) Reactive Power of Converter, (g) Average of DC Link Capacitor Voltages

Conclusion:

This project successfully demonstrated the voltage-oriented vector control of a grid-connected Cascaded H-Bridge (CHB) Voltage Source Converter (VSC) operating in both STATCOM and active rectifier modes. A five-level CHB converter was developed using two H-bridge cells per leg, offering enhanced waveform quality and reduced harmonic distortion.

The control strategy, based on abc–dq0 transformation, enabled independent regulation of active (Id) and reactive (Iq) power. A DC-link voltage controller ensured voltage stability during power transfer from the DC side, while a carrier rotation-based sorting algorithm effectively balanced the switching stress across cells, improving thermal reliability and efficiency.

Dynamic performance analysis confirmed that the converter could seamlessly transition from STATCOM to active rectifier mode, maintaining grid power quality and supplying or absorbing power as required. The system consistently met control objectives such as DC-link voltage regulation, zero reactive power draw from the grid, and reactive power compensation for the AC load.

Thus, the implemented VSC configuration and control strategy demonstrate the viability of CHB converters for flexible and reliable grid-interfaced applications such as FACTS devices, active front-ends, and renewable energy integration.