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# **Zipper and Myriad-RF 1 Development Kit Manual**

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# 1

## Introduction

The combination of the Zipper and Myriad-RF 1 boards provides a low-cost universal radio development platform, based on the flexible, multi-standard Field Programmable Radio Frequency (FPRF) LMS6002D device. It enables developers to implement their products for a wide variety of wireless communication applications efficiently. The main ideas are to:

- Make use of a ready-made design and implementation to accelerate the development time.
- Experiment and evaluate new modulation schemes and wireless systems, operating over a wide frequency range.
- Easily modify and manufacture the platform for new designs using the Open Source database for the complete Kit.

This document provides the following information:

- Detailed description of the hardware platform including setup.
- Software installation, setup and programming of the LMS6002D.
- Example files for running the complete platform.

For more details about the Myriad-RF 1 board, including where to purchase, please visit  
<http://myriadrf.org/>

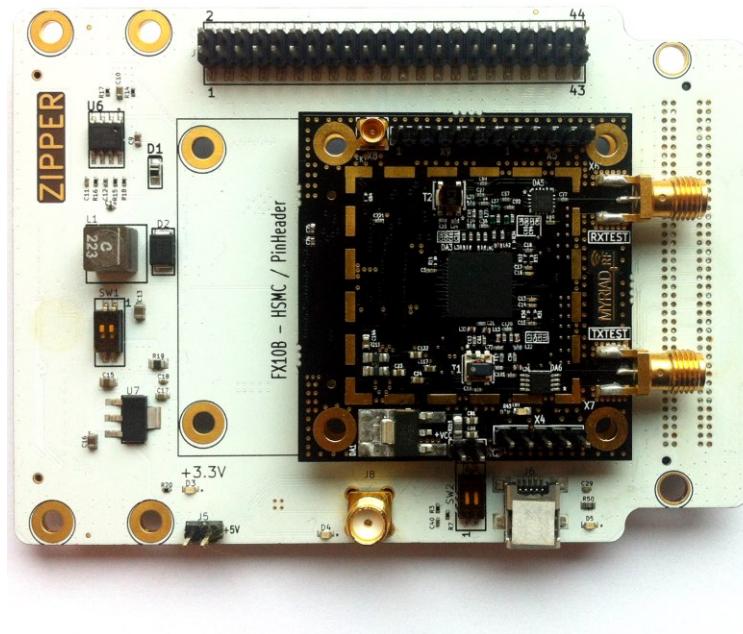
The Zipper board can be purchased from AZIO Electronics, please visit <http://www.aziotw.com/?p=1555>

More information on the LMS6002D device can be found on <http://www.limemicro.com/>

# 2

## Development System Contents

Fully operational development system contains Myriad-RF 1 board, Zipper board and Zipper software. See Figure 1. Zipper and Myriad-RF 1 board development system below.



**Figure 1. Zipper and Myriad-RF 1 board development system**

The universal interface board (Zipper board) allows the user to connect every available baseband to the Myriad-RF 1 board and start developing new applications for RF communication see Figure 2. In addition, the board provides the flexibility to select the desired digital interface frequency, and synchronize to reduce frequency error.

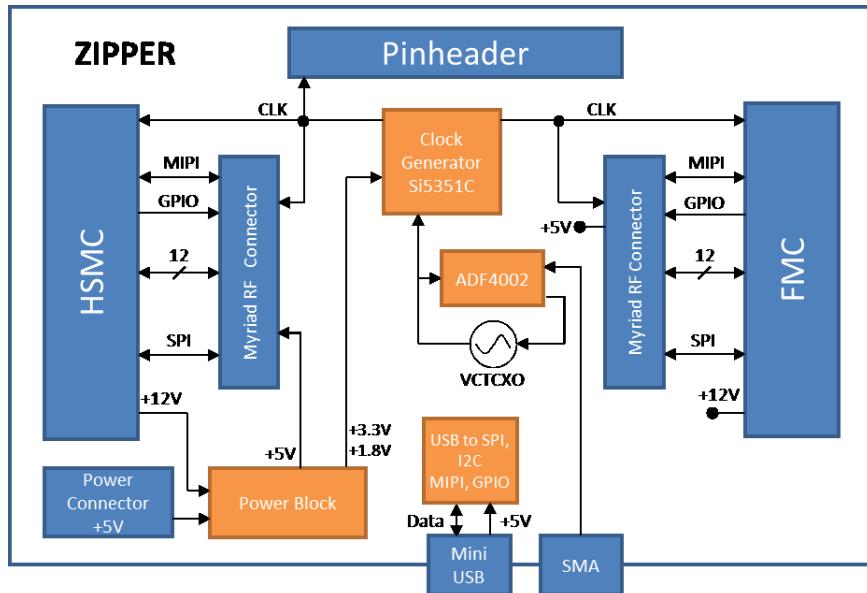


Figure 2. Zipper board block diagram.

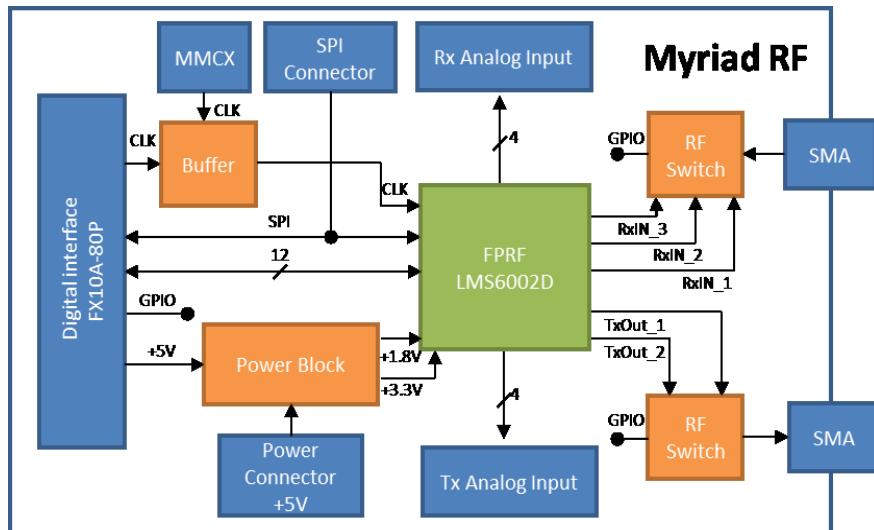


Figure 3. Myriad RF board block diagram

# 3

## **Installing and Running the Software Application**

### **3.1 Windows XP Operating System**

Communications through the USB port has become a standard feature on almost every new personal computer. The Zipper board contains the USB to SPI interface converter and together with the PC software application allows the user simplified control of the Myriad-RF 1 board.

The supplied USB driver software needs to be loaded onto the PC so that it can control the Zipper board via the USB. Before plugging the USB cable into the USB port, make sure that you are logged in as an Administrator.

When the device is plugged into the USB connector the following Wizard window comes up.



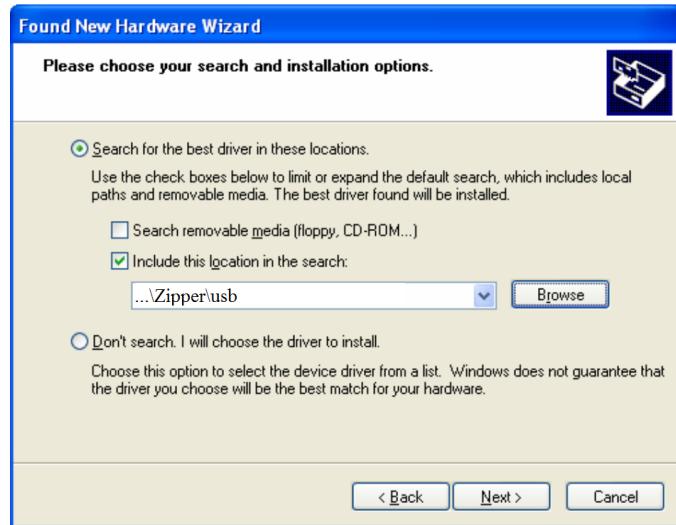
**Figure 4. Hardware wizard**

Select “No, not this time” option and click on Next



**Figure 5. Install driver manually**

Select “Install from a list or specific location (Advanced)” option and click on Next.



**Figure 6. Choose the USBDriver.inf from the folder**

Select “Search for the best driver in these locations” option, then select “Include this location in the search” and check if the following path is correctly setup : <your\_HDD>:\<your\_path>\ Zipper\usb.

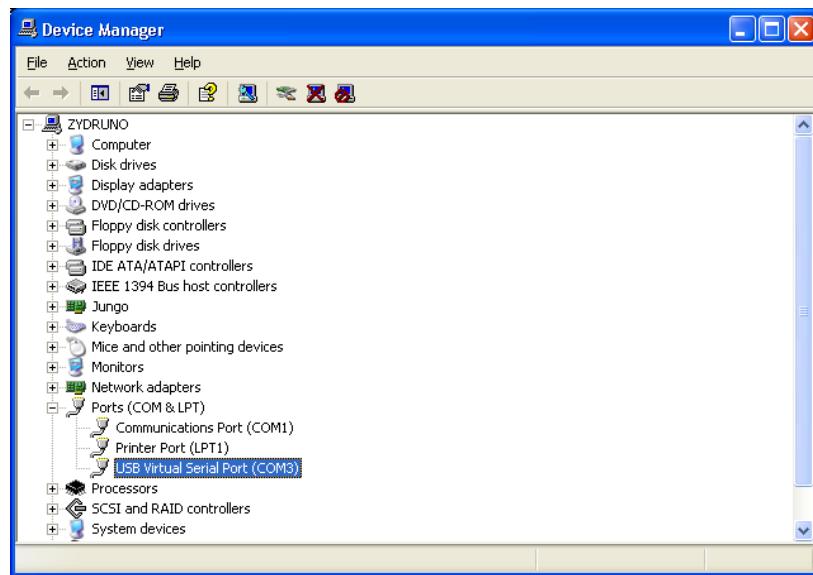
Windows should proceed to install the drivers. The enumeration process (USB term meaning *“connect and establish communication with”*) should start now. If everything is successful, unplug and then plug in your device again to be able to use it.

## 3.2 Determining Serial Ports

After installation, Windows will assign to your USB Virtual Serial device a serial port.

To check the serial port number, please use the following procedure:

1. Right-Click on **My Computer**.
2. Click **Properties** and select the **Hardware** tab.
3. Select **Device Manager**. New widow has to open. Find **USB Virtual Serial Port** under "Ports (COM & LPT)". Note that in this system example it has enumerated as COM3.



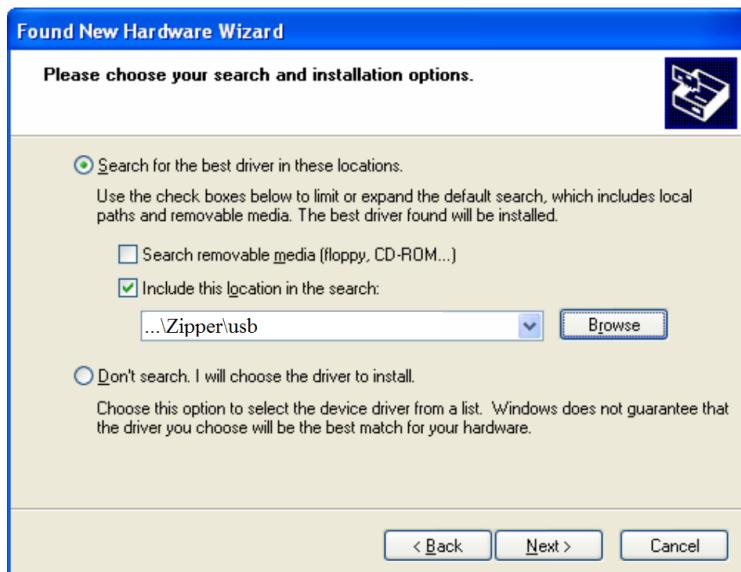
**Figure 7. Check in device manager the new communication port**

### 3.3 Windows 7 Operating System

Plug the USB cable into the USB port of the interface board. No external power connection is required.

After plugging in the board, the USB driver needs to be installed. To install the USB driver do the following:

1. Click on Control Panel → System and Security → System.
2. Click on Device Manager → other devices.
3. Right click on “LUFA USB-RS232 Demo” icon.
4. Click on Update Driver Software and select 2<sup>nd</sup> option: Browse my computer for driver software. Locate and install the driver software manually as shown below.



**Figure 8. Choose the USBDriver.inf from the folder.**

5. The folder should point to the **USBDriver.inf** file, which can be found in the **Zipper** folder. Use the browse function to find this file.
6. Windows should proceed to install drivers. The enumeration process (USB term meaning "*connect and establish communication with*") should start now. If everything is successful unplug and then plug in your device again to be able to use it.

To determine the assign port number you should follow the procedure described in section “3.2 Determining serial ports”.

## 3.4 Using Zipper Software

This section describes how to set up the Zipper software tool and communication with the Zipper board. The Zipper software is shown below.

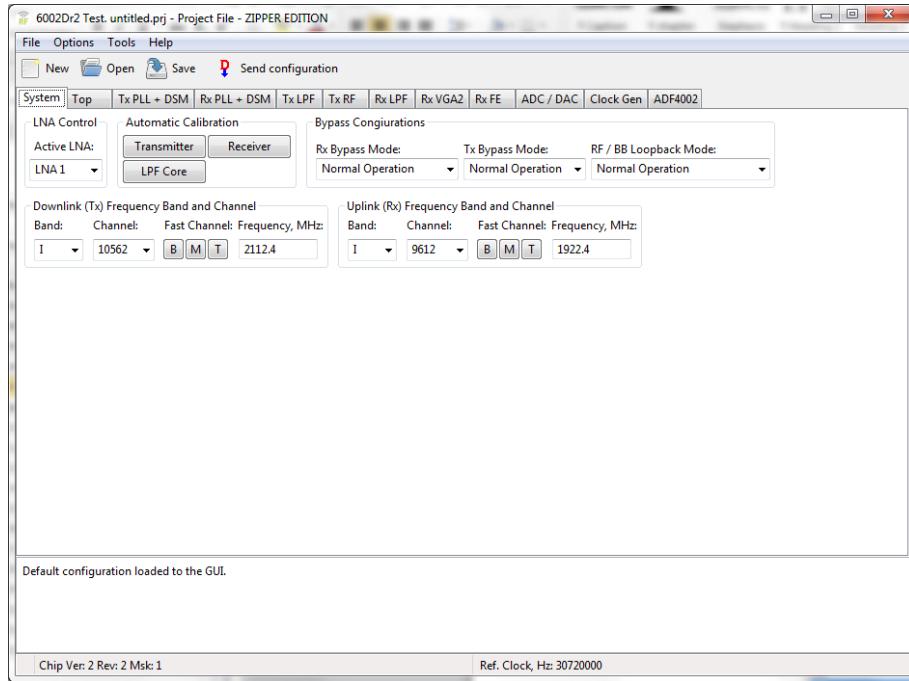


Figure 9. Zipper software main window.

### 3.4.1. Assign COM port and perform register test

Connect the board to your PC and start the application. Go to menu “Options->Communication Settings”. The following window appears

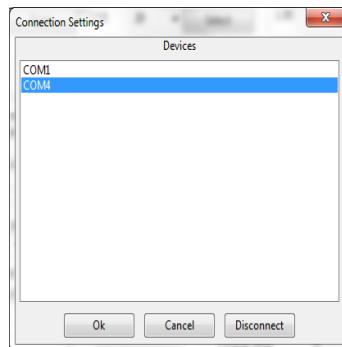
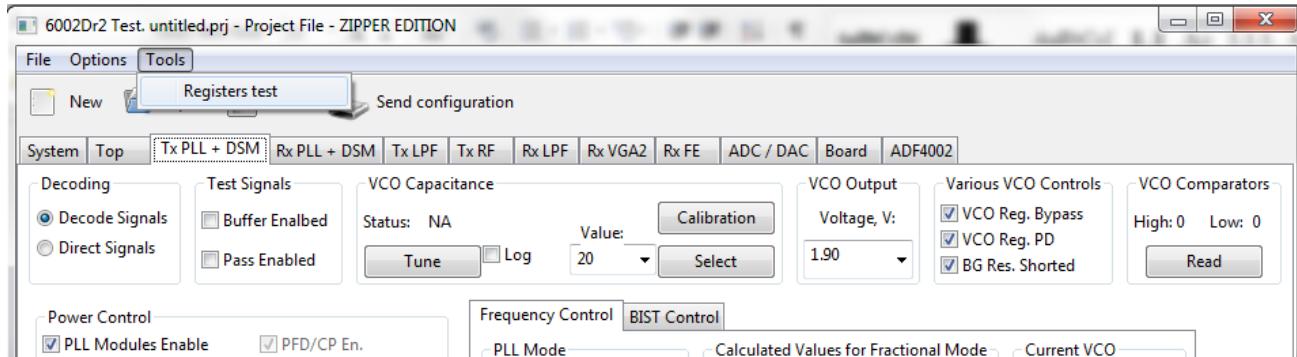


Figure 10. Zipper software Communication settings.

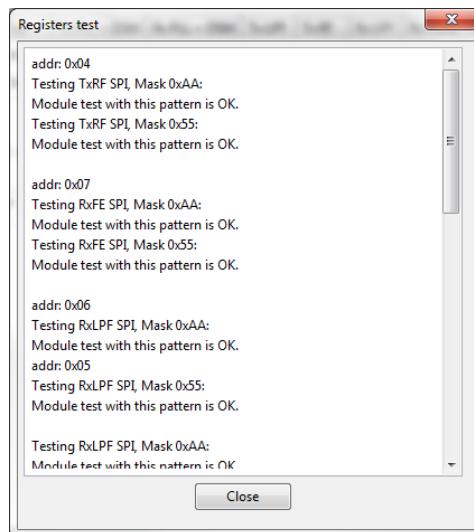
Select enumerated port under USB board. In this example COM port number is 4, but the port number can be different in another case.

To check if the communication with Myriad-RF 1 board is functioning, select the register test sequence by going to menu “Tools->Register Test”.



**Figure 11. Zipper software Register Test.**

The system will then return a full register log indicating OK for correct operation as shown below.



**Figure 12. Zipper software Register Test Log.**

When the system returns an OK message you are now ready to commence testing. If the system returns 00 or FF instead of the OK this means there is a communication problem with the Myriad-RF 1 board.

Here are hints when the software communication check fails:

- If the system test has returned 00 or FF instead of OK then shut down the Zipper software and disconnect the Zipper board. Leave for a few seconds before connecting the board and opening the Zipper software again. Start the registers test process again.
- If the system returns 00 then there is a problem with the connection between the PC and the board USB port. You will need to check the connection and start the process again.
- If the system test returns FF then you know the PC and the USB port are communicating properly. Connect the Zipper board to +5V supply and start the process again. If you now get an OK for the register test map results then the system is ready for testing. If the system still returns 00 or FF instead of an OK, reboot the entire connected system starting with the PC.

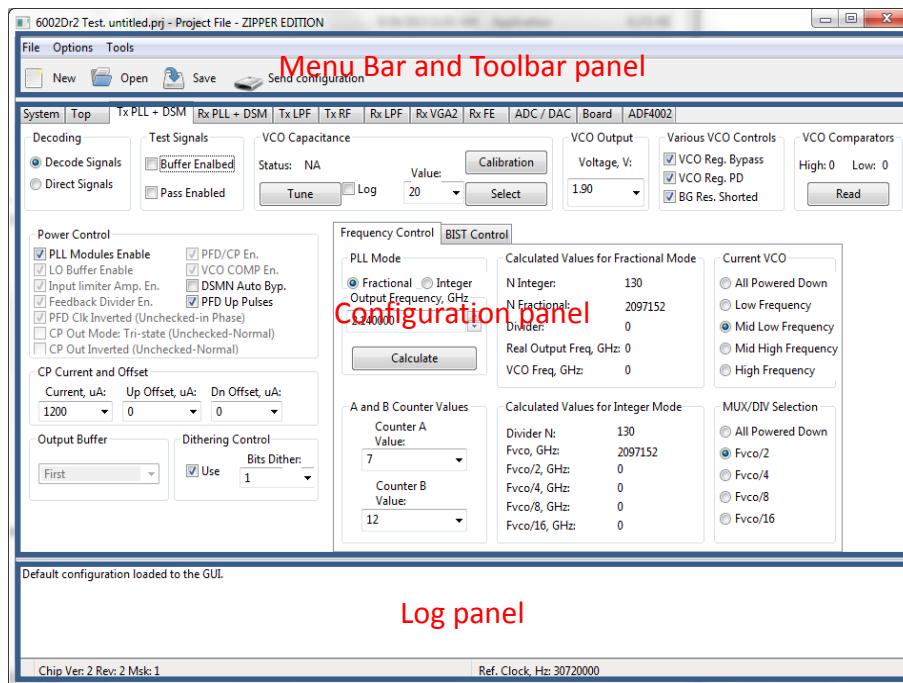
After the PC has finished rebooting apply power to the Zipper board and restart registers testing.

You should now see the correct OK message and the LMS6002D chip version will be displayed at the bottom left corner of the main window. The system is now ready to commence testing.

### 3.5 Zipper software description

This section describes the Zipper software tool and each of the buttons and embedded controls. Most of the pages in the tool can be read across to the top level sections of the SPI programming map, with the exception of the ‘System page’ and the ‘ADF4002’ page.

The Zipper software consists of several parts: menu bar and toolbar panel, configuration panel, log panel. See Figure 13.



**Figure 13. Zipper software window sections.**

The **Menu Bar and Toolbar panel** includes basic application configurations. The user can start new projects or save the current project with all register settings for LMS6002D chip. The same project file can be loaded using “Open project” command in the File menu. Register settings can be saved in HEX format using “Save to HEX” command.

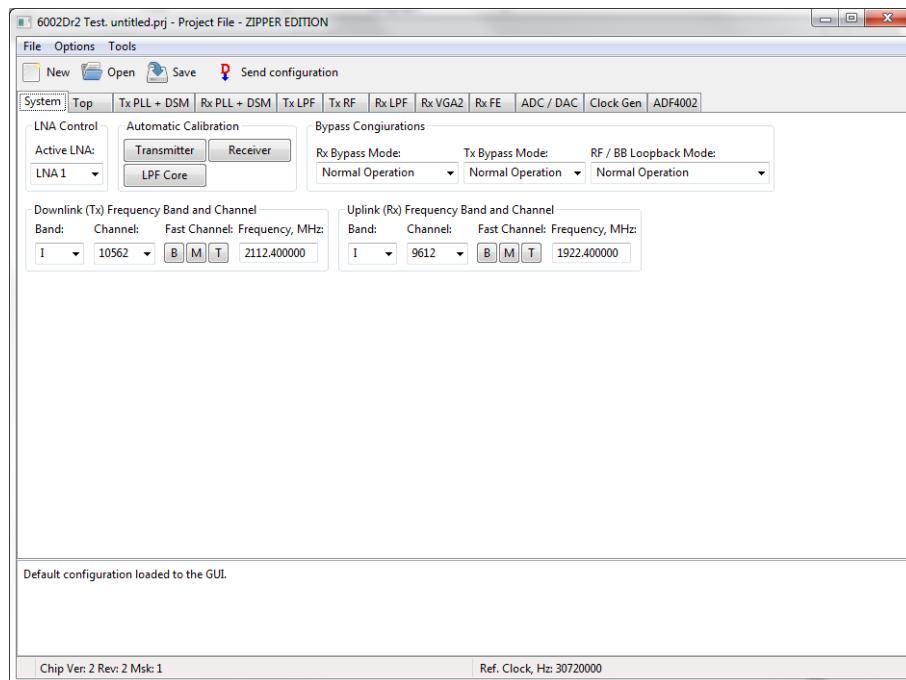
**Configuration panel** controls the LMS6002D registers depending on the selected tab.

**The Log panel** section logs data of all executed application commands. In the lower left corner it shows the LMS6002D chip version.

### 3.5.1. System Interface

The System interface page allows configuring the synthesizers to the 3GPP bands by channel number and has buttons for bottom, middle and top frequencies for each. This makes changing frequency for the commonly used test channels simpler. For applications other than 3GPP testing please see section 3.5..

Automatic calibration (see below) is also controlled from this page (the device carries out the calibrations itself under SPI prompting).



**Figure 14. Zipper software System Interface window.**

#### Downlink and Uplink Frequency setting by band/channel number.

The synthesizers can be configured by channel number to the correct frequency in each 3GPP band. Buttons are provided for bottom, middle and top frequencies for each band. This makes changing frequency for the commonly used test channels easier.

#### Bypass configurations

The various bypass test modes and loop back test modes can be implemented by selecting from the drop down boxes, default is Normal operation.

### **Automatic Calibration**

The Automatic calibration buttons can be used to run through the series of SPI commands required to implement the various self-calibration routines provided on the chip. Use of these macros is implemented as part of a calibration procedure and each button does not carry out a full calibration. Care should be exercised in using Automatic Calibration because use of the buttons in the wrong context could make the calibration state worse rather than better.

Automatic calibration should be done in the following order:

#### **a. LPF Core – Press LPF core button**

This executes the internal LMS6002D process related resistor capacitor (RC) calibration. LPF Core calibration is performed once per device to ensure that the corner frequencies of the LPFs are optimized. The calibration selects the LPF response which is closest and above the required bandwidth. This ensures modulation quality is not adversely impacted but, at the same time, sufficient rejection is provided for adjacent and alternate channel attenuation.

This should be done first, as the optimum DC calibration values for LPF's will change if this is done after the filter DC calibration.

#### **b. Transmitter**

The transmitter calibration executes a DC calibration on the TX LPF (I and Q) circuit. This zeros the DC contribution at the output of the filters so that the DC level at the mixer input does not change when the TX VGA1 gain is changed.

When executing this calibration make sure that no signal is applied to the transmit path via the analog input. For better DC calibration, set LMS6002D DAC's to all zeros from the baseband or power down DACs using the Graphical User Interface (GUI) via the ADC/DAC tab.

When the chip is powered, any not programmed DAC's may produce a high level DC which will affect the internal DC calibration.

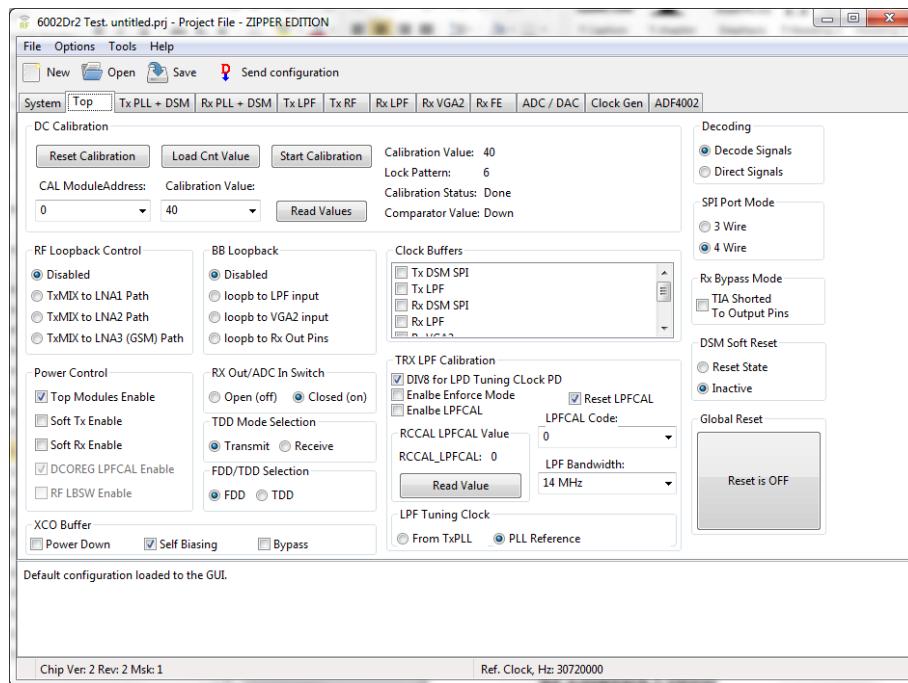
#### **c. Receiver**

This executes a DC calibration on the Rx LPF (I and Q), and Rx VGA2 (I and Q). This minimizes the DC contribution at the output of the filters and Rx VGA2.

When executing this calibration make sure that there is no signal applied to the Rx input.

### 3.5.2. Top

Various loop back and calibrations are also controlled on this page. They are not needed for basic operation. Automatic calibrations should all be done from the ‘System’ page where macros have been written to apply the calibration routines automatically.



**Figure 15. Zipper software Top window**

Description of each function available from this page is as follows:

#### DC Calibration

This carries out the top level DC calibration for the device. This is the R component of the RC cal value which is used in each of the LPF (Tx and Rx) process calibration values. Only calibration module address 0 is used.

#### Decoding

Select ‘Decode Signals’ or ‘Direct Signals’ for control of different parts of the SPI memory map. Use ‘Decode Signals’ mode to control general purpose registers. Select ‘Direct Signal’ mode to access LMS6002D test registers.

#### RF Loopback Control

This is a test mode. The RF loopback control sets the path used for the loopback from Tx to Rx input. Please refer to the SPI programming and calibration document for further details.

### **BB (Baseband) Loopback**

Test modes, sets the BB loopback from Tx to Rx input.

### **Clock Buffers**

Enable pins turn the internal clock buffers on and off. These should be enabled when control of the device is needed; however, during operation, the SPI clocks which are not being used should be disabled to reduce the risk of SPI clock spurious signals.

### **SPI Port Mode**

Selects 3 or 4 wire SPI mode. 4 wire mode is used with the USB board solution.

### **Rx Bypass Mode**

Not used.

### **Power Control**

This controls turn on/off the Tx and Rx top level blocks of the LMS6002D via SPI. Select “Soft Tx Enable” to enable transmitter path and “Soft Rx Enable” to enable receiver path.

### **Rx Out/ADC In Switch**

Select “Closed” to monitor the receiver analog input. Select “Open” if you wish to route an external signal into the ADC.

### **TDD Mode Selection**

Use only if TDD mode is selected. Select “Transmit” when transmitter is in operation and select “Receive” when receiver is in operation.

### **FDD/TDD Selection**

Select FDD if in application the separate frequency bands are used for the transmitter and receiver. Select TDD if in application the duplex communication links are separated by the allocation of different time slots in the same frequency band.

### **TRX LPF Calibration**

This section is used to calibrate the internal LMS6002D capacitance of the device to ensure the LPF BWs are correct. To execute the calibration, check then uncheck the Reset LPFCAL box (to reset the calibration module). Then, check and uncheck the Enable LPFCAL box to execute the calibration. The result can be found in the DC calibration area when the read button is pressed.

Enable Enforce Mode and LPFCAL Code are not used. The LPF BW sets the bandwidth used for the calibration. If you are using WCDMA, it selects 2.5MHz. The result should be copied into the TXLPF and RXLPF from the ‘TRX\_LPF\_CAL’ drop down box.

### **DSM Soft Reset**

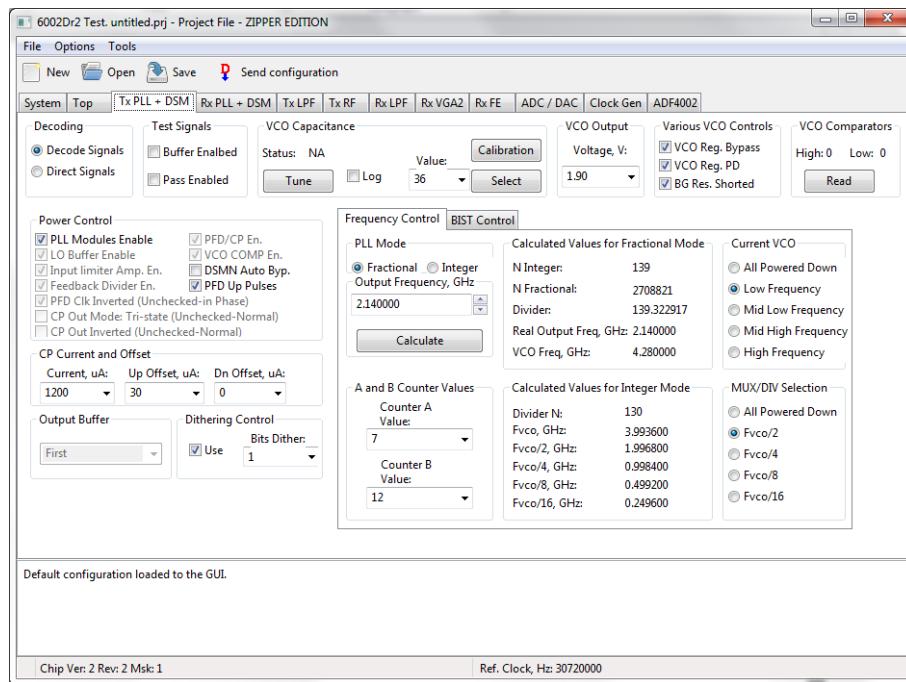
Keep on inactive.

**Global Reset**

This toggles the reset pin via the USB SPI interface. The LMS6002D should be reset after power up to put it into a known state.

### 3.5.3. Tx PLL + DSM (Digital Spectrum Modulation)

The Tx PLL is controlled from this page. If the frequency control on the ‘System’ page is used and the correct ‘setup files’ have been automatically downloaded, then this page should not be needed. However, a few points to check are that the tick boxes shown in the diagram below are enabled:



**Figure 16. Zipper software TxPLL + DSM window**

A description of each function available from this page is as follows:

#### Decoding

Select ‘Decode’ or ‘Direct’ signals for control of different parts of the SPI memory map. When swapping between the two options the available options are highlighted (and the unavailable ones grayed out). Use ‘Decode’ mode.

#### Test Signal

Design test signals – leave unchecked.

#### VCO Capacitance

Control for internal VCO frequency. Correct setting of VCO capacitance is described in LMS6002D Programming and Calibration Guide. Selections made when using the ‘Calculate’ button however are decided based on the calibration table used in this block.

To properly select the ‘VCO Capacitance’ click “Tune” after “Calculate”. If you want to observe the VCO capacitor selection algorithm results select “Log”.

### **VCO Output**

VCO output level control for test purpose only. Enabled through ‘Various VCO Controls’.

### **Various VCO Controls**

Various VCO controls for test purposes only.

### **VCO Comparators**

Reads the state of the VCO Comparators. The truth table is:

VTUNE_H	VTUNE_L	Status
0	0	OK
1	0	Vtune is high (> 2.5V) PLL lock not guaranteed.
0	1	Vtune is Low (< 0.5V) PLL lock not guaranteed.
1	1	Not possible, check SPI connections.

**Table 1 Comparator readings**

### **Power Control**

Individual parts of the PLL circuitry can be turned on and off – leave as default.

### **Charge Pump (CP) Current and Offset**

CP Current and Offset is set based on the selected loop filter and loop BW. For the recommended loop filter (implemented on the Myriad RF 1 board) the current should be 1200uA and Up Offset 30uA, as shown.

### **Output Buffer**

Control not used in TxPLL.

### **Dithering Control**

DSM dithering. Leave it set to 1.

### **Frequency Control**

This control sets the PLL divide ratios, VCO and output divider selection. The individual parts of this block are described in more detail below:

### **PLL Mode**

Selects fractional or integer mode. Use fractional mode.

**Output Frequency (GHz)** - set the desired Tx frequency in the text box.

‘Calculate’ button – calculates the required divide ratio based on the desired/operating LO frequency and reference frequency.

To properly select the ‘VCO Capacitance’ click “Tune” after “Calculate”. If you want to observe the VCO capacitor selection algorithm results select “Log”

The ‘Current VCO’ and the ‘MUX/DIV Selection’ show the choice made by the software by pressing “Calculate” or “Tune” buttons.

#### **PLL Calibration Data (displays following the “Calculate” function)**

The software is using a lookup table to select the correct register settings for TxPLL. To see the look up table, press the ‘Calibration’ button and a pop-up window will appear with the Frequency vs Capacitance calibration table data.

Vco1 Freq. GHz			Vco1 Cap		
1	3.76	0			
2	4.2	31			
3	4.84	63			

Vco2 Freq. GHz			Vco2 Cap		
1	4.68	0			
2	5.32	31			
3	6.04	63			

Vco3 Freq. GHz			Vco3 Cap		
1	5.72	0			
2	6.44	31			
3	7.36	63			

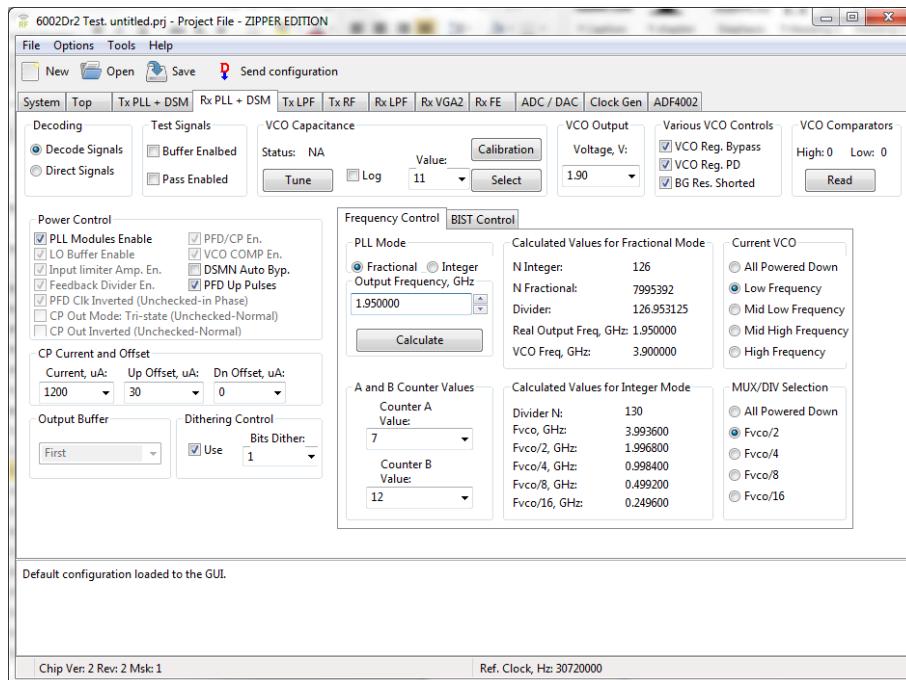
Vco4 Freq. GHz			Vco4 Cap		
1	6.92	0			
2	7.36	31			
3	8.398	63			

**Figure 17. Frequency versus capacitance calibration table data**

The calibration data consists of frequency versus capacitance value responses. The software automatically gives the optimum VCO data. The optimum calibration values are set as default, no need to change them.

### 3.5.4. Rx PLL + DSM

The Rx PLL is controlled from this page. If the frequency control on the ‘System’ page is used and the correct ‘setup files’ have been automatically downloaded, then this page should not be needed. However a few points to check are that the tick boxes shown in the diagram below are enabled.



**Figure 18. RX PLL + DSM window**

A description of each function available from this page is as follows:

#### Decoding

Select ‘Decode’ or ‘Direct’ signals for control of different parts of the SPI memory map. When swapping between the two options the available options are highlighted (and the unavailable ones grayed out). Use ‘Decode’ mode.

#### Test Signal

Design test signals – leave unchecked.

#### VCO Capacitance

Control for internal VCO frequency. Correct setting of VCO capacitance is described in LMS6002D Programming and Calibration Guide. Selections made when using the ‘Calculate’ button however are decided based on the calibration table used in this block.

To properly select the ‘VCO Capacitance’ click “Tune” after “Calculate”. If you want to observe the VCO capacitor selection algorithm results select “Log”.

### **VCO Output**

VCO output level control for test purpose only. Enabled through ‘Various VCO Controls’.

### **Various VCO Controls**

Various VCO controls for test purposes only.

### **VCO Comparators**

Reads the state of the VCO Comparators. The truth table is:

VTUNE_H	VTUNE_L	Status
0	0	OK
1	0	Vtune is high (> 2.5V), PLL lock not guaranteed.
0	1	Vtune is Low (< 0.5V), PLL lock not guaranteed.
1	1	Not possible, check SPI connections.

**Table 2 Comparator readings**

### **Power Control**

Individual parts of the PLL circuitry can be turned on and off – leave as default.

### **Charge Pump (CP) Current and Offset**

CP Current and Offset is set based on the selected loop filter and loop BW. The recommended loop filter is implemented on the evaluation board. The Current should be 1200uA and Up Offset 30uA, as shown.

### **Output Buffer**

Sets the correct PLL output buffer for the selected LNA:

LNA 1 = First

LNA 2 = Second

LNA 3 = Third and

Disable.

When Active LNA is selected in the “System” page the correct buffer is automatically selected on this page.

### **Dithering Control**

DSM dithering. Leave it set to 1.

### **Frequency Control**

This selects the PLL divide ratios, VCO and output divider. The individual parts of this block are described in more detail below.

#### **PLL Mode**

Selects fractional or integer mode. Use fractional mode.

**Output Frequency (GHz)** - set the desired Rx frequency in the text box. Activating the ‘Calculate’ button calculates the required divide ratio based on the required frequency and reference frequency.

To properly select the ‘VCO Capacitance’ return to this box and click “Tune” after “Calculate”. If you want to observe the VCO capacitor selection algorithm results select “Log”.

The ‘Current VCO’ and the ‘MUX/DIV Selection’ show the choice made by pressing “Calculate” or “Tune” buttons).

### **PLL Calibration Data**

The software is using a lookup table to select the correct register settings for RxPLL. To see the look up table, press the ‘Calibration’ button and a pop-up window will appear with the Frequency vs Capacitance calibration table data.

	Vco1 Freq. GHz	Vco1 Cap
1	3.76	0
2	4.2	31
3	4.84	63

	Vco2 Freq. GHz	Vco2 Cap
1	4.68	0
2	5.32	31
3	6.04	63

	Vco3 Freq. GHz	Vco3 Cap
1	5.72	0
2	6.44	31
3	7.36	63

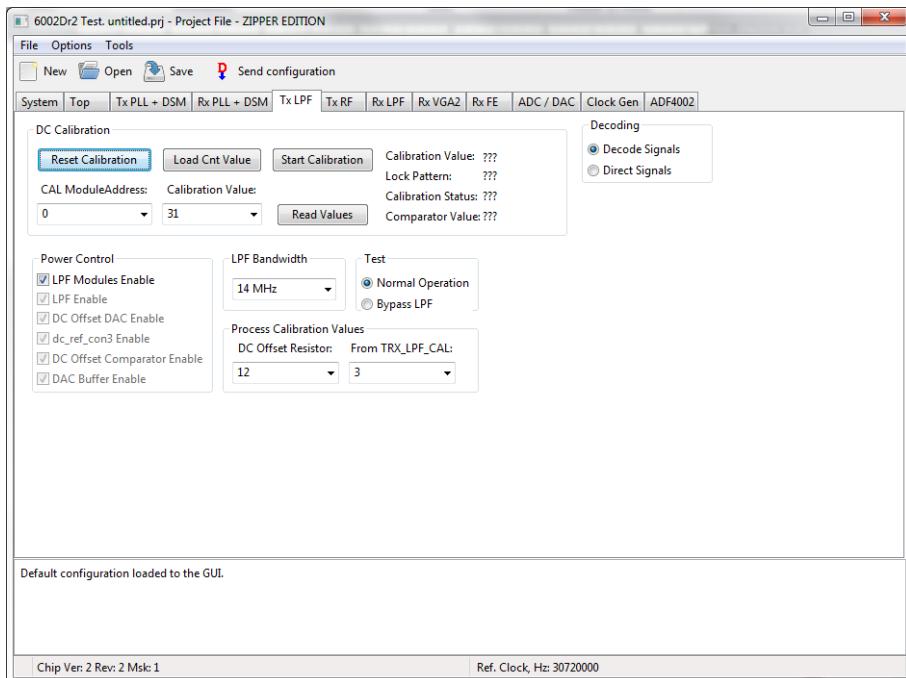
	Vco4 Freq. GHz	Vco4 Cap
1	6.92	0
2	7.36	31
3	8.398	63

**Figure 19. Frequency vs capacitance calibration table data**

The calibration data consists of frequency versus capacitance value responses. The software automatically gives the optimum VCO data. The optimum calibration values are set as default, no need to change them.

### 3.5.5. Tx LPF

The Tx LPF page contains the SPI controls for the transmitter low pass filters, notably the LPF BW and also the controls for the DC calibration.



**Figure 20. Tx LPF window**

The description of each function available from this page is as follows:

#### DC Calibration

These are the individual controls for the DC correction and auto-calibration routines for the TX LPF (controlled by the ‘Transmitter’ auto-calibration button on the ‘System’ page).

The Tx LPF DC calibration has 2 stages which can be calibrated:

- TXLPF(I) at Cal module address 0
- TXLPF(Q) at Cal module address 1

#### Decoding

Select ‘Decode’ or ‘Direct’ signals for control of different parts of the SPI memory map. When swapping between the two options the available selection is highlighted (and the unavailable one is grayed out). ‘Decode’ mode is recommended.

#### Power Control

This control powers down the LPF modules, grayed out controls can be accessed by using direct signals mode.

### **LPF Bandwidth**

Set the LPF BW in the drop down box, from 0.75MHz to 14MHz. Note RF system BW is twice this number, i.e. 0.75MHz LPF BW is 1.5MHz system BW.

### **Test**

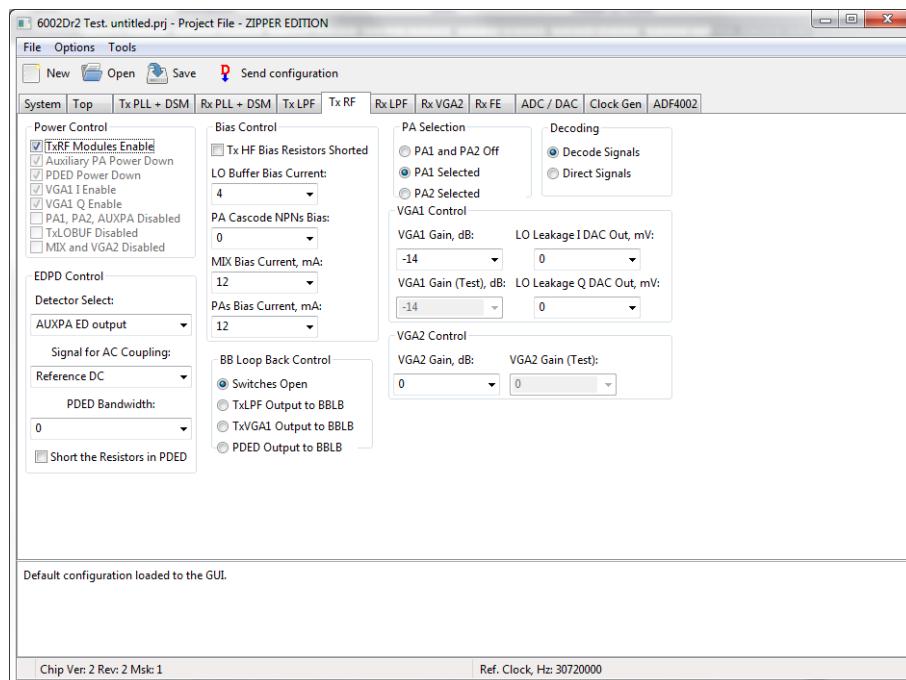
Enables LPF bypass for test purposes. Ensure ‘Normal Operation’ is enabled.

### **Process Calibration Values**

This displays the RC calibration values used to process trim the LPF BW. The values are calculated during top level calibration and written into these locations (carried out automatically by ‘LPF Core’ on ‘System’ page).

### **3.5.6. Tx RF**

The Tx RF page contains the SPI controls for the Tx RF stages, including all Tx gain control, LO correction and Tx output selection.



**Figure 21. Tx RF window**

The description of each function available from this page is as follows:

### **Power Control**

Powers down stages within the Tx RF block – grayed out controls are accessible via ‘Direct’ decoding mode.

### **Bias Control**

Settings for Bias Control are shown below, do not change:

- Tx HF Bias Resistor Shorted, leave not selected.
- LO Buffer Bias Current – ‘4’, leave it at default.
- PA Cascode NPNs Bias –‘0’, leave it at default.
- MIX Bias Current, mA – ‘12’, leave it at default.
- PAs Bias Current, mA –‘12’, leave it at default.

### **PA Selection**

Select Tx output stage PA1, PA2 or both off.

### **Decoding**

Select ‘Decode’ or ‘Direct’ signals for control of different parts of SPI memory map. When swapping between the two options the available selection is highlighted (and the unavailable one grayed out). ‘Decode’ mode is recommended.

### **VGA1 Control**

VGA1 Gain sets VGA1 gain (IF gain stage) from -4 to -36dB via the drop down box. ‘LO Leakage I DAC Out’ and ‘LO Leakage Q DAC Out’ set the DC level injected via the LO correction DACs for LO cancellation.

### **VGA2 Control**

VGA2 Gain sets VGA2 gain (RF gain stage) from 0 to 25dB via the drop down box.

### **EDPD Control**

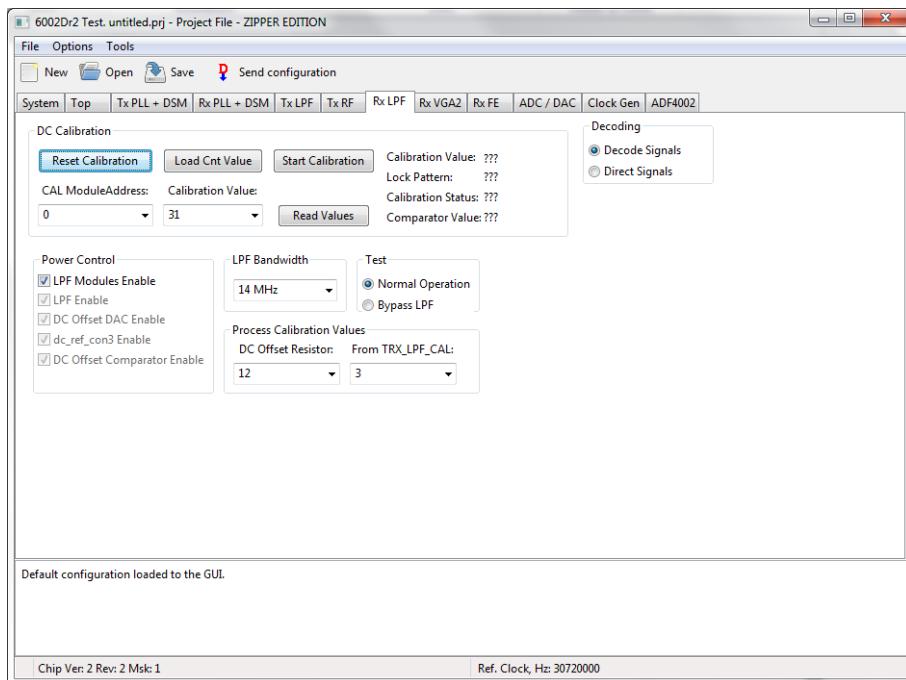
Envelope detector and power detector controls. Leave as defaults.

### **BB Loop Back Control**

Baseband loop back control options. BB loop back works in combination with the “Top” tab BB loopback selections. If no BB loop back is required, then select the “Switches Open” option.

### 3.5.7. Rx LPF

The Rx LPF page contains the SPI controls for the receiver low pass filters, notably the LPF BW and it also features the controls for the DC calibration.



**Figure 22. Rx LPF window**

The description of each function available from this page is as follows:

#### DC Calibration

These are the individual controls for the DC correction and auto-calibration routines for the RX LPF (controlled by the ‘Receiver’ auto-calibration button on the ‘System’ page).

The Rx LPF DC calibration has 2 stages which can be calibrated:

- RXLPF(I) at Cal module address 0
- RXLPF(Q) at Cal module address 1

#### Decoding

Select ‘Decode’ or ‘Direct’ signals for control of different parts of the SPI memory map. When swapping between the two options the available selection is highlighted (and the unavailable one grayed out).

#### Power Control

This powers down the LPF modules, grayed out controls can be accessed by using direct signals mode. Using ‘Decode’ mode is recommended.

### **LPF Bandwidth**

Set the LPF BW in the drop down box, from 0.75MHz to 14MHz. Note that RF system BW is twice this number, i.e. 0.75MHz LPF BW is 1.5MHz system BW.

### **Test**

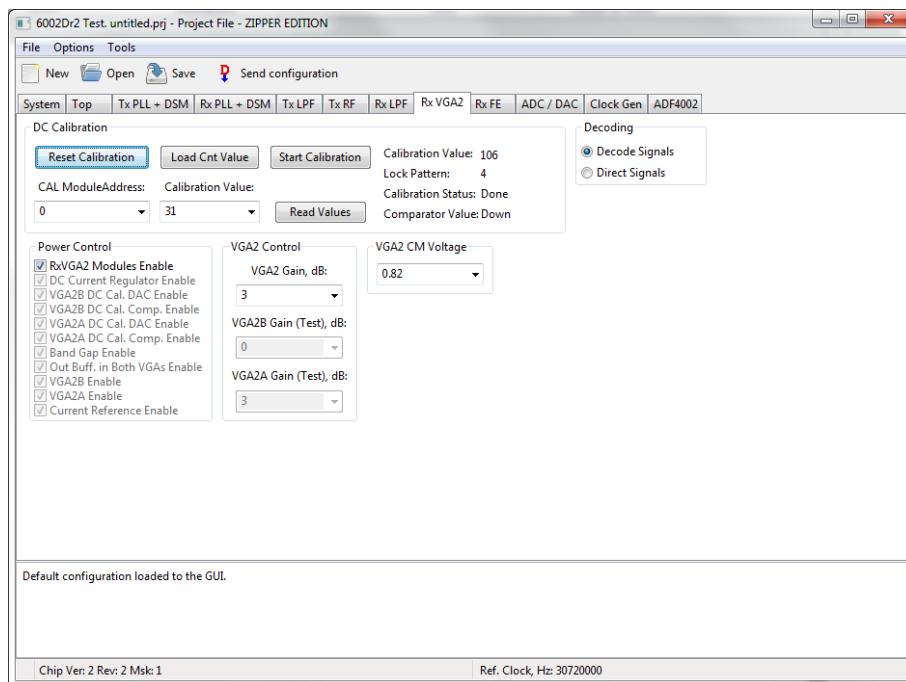
LPF bypass for test purposes. Ensure ‘Normal Operation’ is enabled.

### **Process Calibration Values**

These are the RC calibration values used to process trim the LPF BW, values are calculated in the top level calibration and written into these locations (carried out automatically by ‘LPF Cal’ on ‘System’ page).

### **3.5.8. Rx VGA2**

This page displays the SPI controls for the RX VGA2 stage settings.



**Figure 23. Rx VGA2 window**

The description of each function available from this page is as follows:

### **DC Calibration**

These are the individual controls for the DC correction and auto-calibration routines for the RX VGA2 (controlled by the ‘Receiver’ auto-calibration button on the ‘System’ page).

The Rx VGA2 DC calibration has 5 stages which can be calibrated:

- RXVGA2 Top at Cal module address 0
- RXVGA2a(I) at Cal module address 1
- RXVGA2a(Q) at Cal module address 2
- RXVGA2b(I) at Cal module address 3
- RXVGA2b(Q) at Cal module address 4

### **Decoding**

Select ‘Decode’ or ‘Direct’ signals for control of different parts of SPI memory map. When swapping between the two options the selected option is highlighted (and the unavailable one grayed out). Use ‘Decode’ mode.

### **Power Control**

Powers down the RXVGA2 modules, grayed out controls can be accessed by using direct signals mode.

### **VGA2 Control**

This sets the RXVGA2 Gain, where the available range is 0 to 30dB in 3dB steps. Decoding is set to ‘Decode Signals’ for normal use.

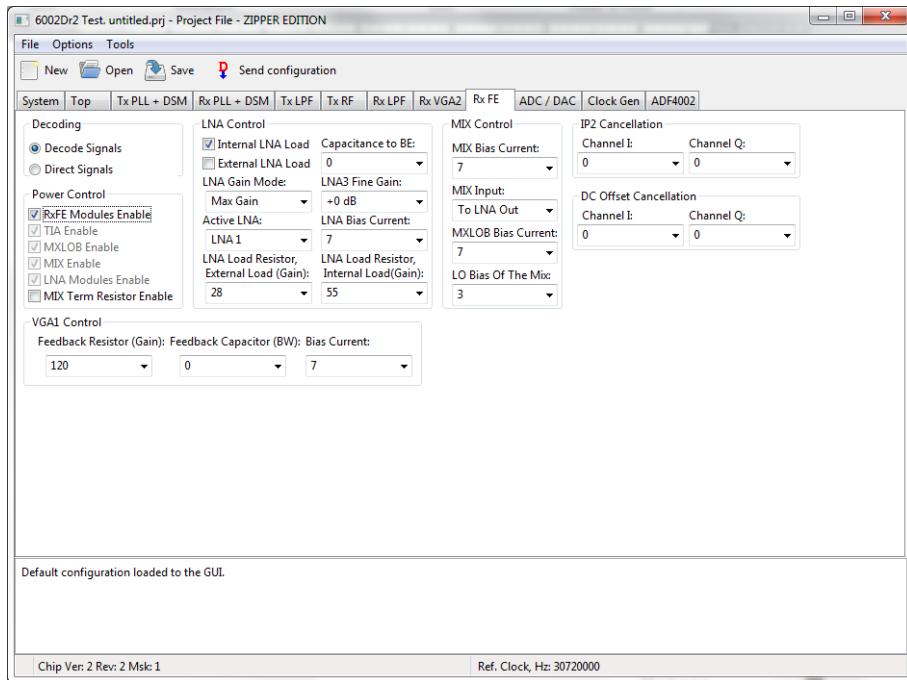
VGA2B Gain (Test) and VGA2A Gain (Test) are available in test mode to control A and B stages directly. Decoding is set to ‘Direct Signals’ to use this function. This feature is not used for normal operation.

### **VGA2 CM Voltage**

This control sets the RXVGA2 output common node voltage to interface to the ADCs. Code 12, which corresponds to 820mV, is recommended.

### 3.5.9. Rx FE

This page is used to set the SPI controls for the Rx Front End stages, including LNA selection, LNA gain, RXVGA1 gain and RX LO cancellation.



**Figure 24. Rx FE window**

The description of each function available from this page is as follows:

#### Decoding

Select ‘Decode’ or ‘Direct’ signals for control of different parts of the SPI memory map. When swapping between the two options the selected option is highlighted (and the unavailable one grayed out).

#### LNA Control

This is used for setting the LNA controls as follows:

- Internal/External LNA load tick boxes – use internal.
- Capacitance to BE – leave as default (0)
- LNA Gain Mode – selects LNA gain, Max, Mid and Bypass.
- LNA3 Fine Gain – fine gain setting for LNA3 which has no bypass mode, 0 to + 3dB.
- Active LNA – Select active LNA 1 to 3. Users also need to change the RX LO buffer in ‘RX PLL + DSM’ page when changing LNA. This control changes the RX LO buffer automatically.

- LNA bias current – leave at default (7).
- External load – not used when Internal load selected.
- Internal Load (0 to 63) sets LNA gain, max (0dB) = 55, min (-9.2dB) = 0. Do not set above 55.

### **MIX Control**

Settings for Mix control are shown below, do not change:

- MIX Bias current – ‘7’, leave it at default.
- MIX Input – ‘To LNA Out’, leave it at default.
- MXLOB Bias Current – ‘7’, leave it at default.
- LO Bias Of The MIX – ‘3’, leave it at default.

### **IP2 Cancellation**

IP2 Cancellation applies an offset to the mixer to improve IP2 performance. Not required.

### **Power Control**

This control powers down the RXFE modules, grayed out controls can be accessed by using direct signals mode.

### **DC Offset Cancellation**

The control applies a DC level to the mixer output to cancel any DC level from LO leakage.

### **VGA1 Control**

***Feedback Resistor (0 to 123)***. Only use settings up to 120

Sets VGA1 gain, max (0dB) = 120, min (-24dB) = 0, so do not set above 120. Gain control is not log-linear.

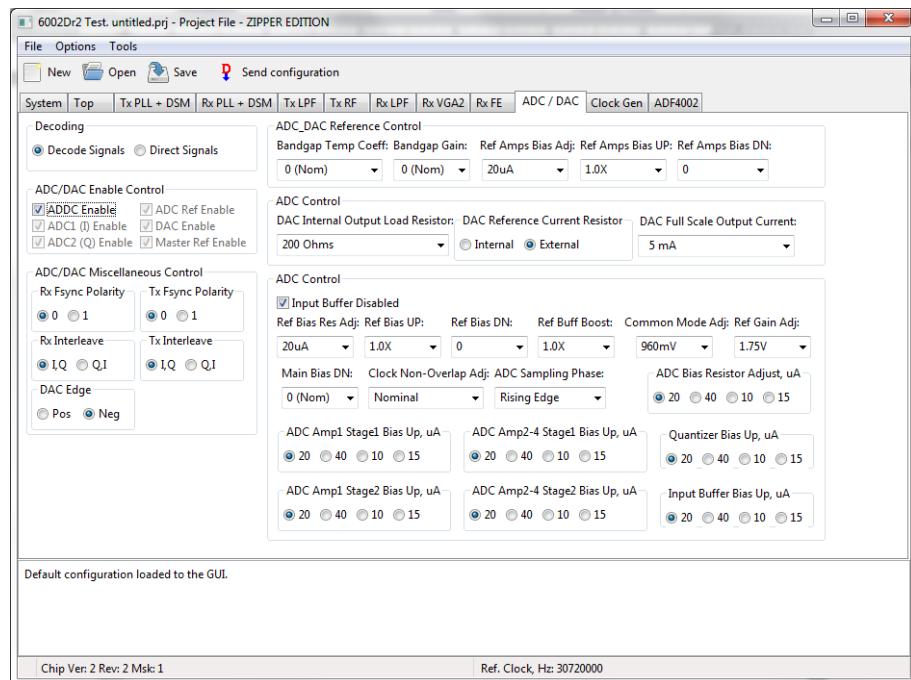
***Feedback capacitor (0 to 123)***

This introduces a single pole LPF at VGA1 output. The bandwidth is dependent on ‘Feedback resistor’ and ‘Feedback capacitor’. For no filtering, leave it at default (0).

***Bias Current*** - leave at default (7).

### 3.5.10. ADC/DAC

The ADC / DAC page sets all the controls for the data ADCs in the receive path and data DACs in the transmit path.



**Figure 25. ADC/DAC window**

The description of each function available from this page is as follows:

#### Decoding

Select ‘Decode’ or ‘Direct’ signals for control of different parts of the SPI memory map. When swapping between the two options, the available options are highlighted (and the unavailable ones are grayed out).

#### ADC/DAC Reference Control

Settings for the ADC/DAC reference control are shown below, do not change:

- Bandgap Temp Coeff – ‘0 (Nom)’, leave it at default.
- Bandgap Gain – ‘0 (nom)’, leave it at default.
- Ref Amps Bias Adj – ‘20uA’, leave it at default.
- Ref Amps Bias UP – ‘1.0X’, leave it at default.
- Ref Amps Bias DN – ‘0’, leave it at default.

### **ADC/DAC Enable Control**

Check ‘ADC Enable’ to enable ADCs and DACs. Sub-blocks are also independently controllable in ‘Direct Signals’ mode.

### **DAC Control**

- Internal output Load Resistor 50, 66, 100, 200 Ohms or Open Circuit setting (when using external load resistor).
- DAC Reference Current resistor – use External.
- DAC Full Scale Output Current (2.5, 5, 10mA). Use Load resistor and Full scale output current to control DAC output voltage swing.

### **ADC/DAC Miscellaneous Control**

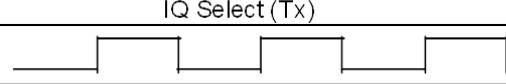
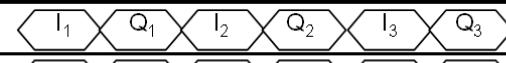
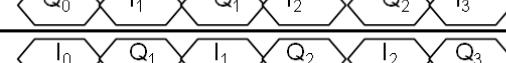
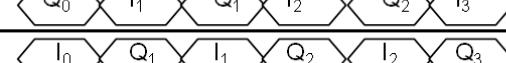
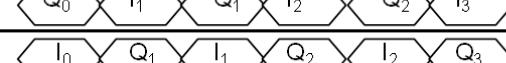
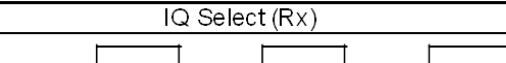
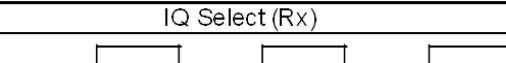
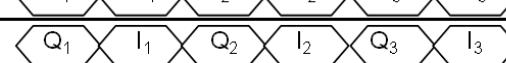
Rx Fsync Polarity – sets the polarity of the RX IQ SEL signal for the first sample of the Rx IQ pair.

Rx Interleave – sets the order of the RX IQ pair.

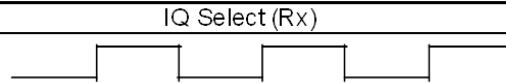
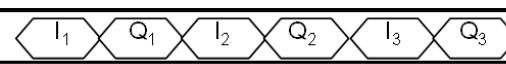
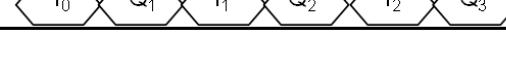
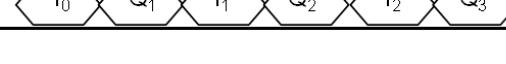
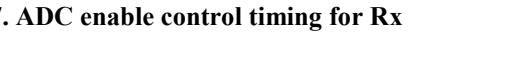
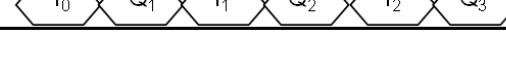
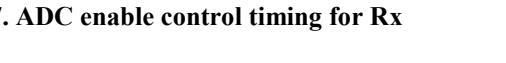
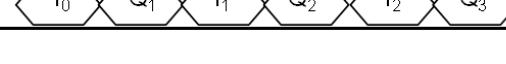
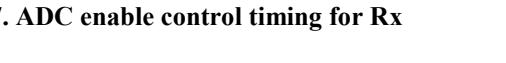
Tx Fsync Polarity – sets the polarity of the Tx IQ SEL signal for the first sample of the Tx IQ pair.

Tx Interleave – sets the order of the Tx IQ pair.

See diagram below for explanation:

Fsync Polarity	Interleave	IQ Select (Tx)					
							
0	I,Q						
0	Q,I						
1	I,Q						
1	Q,I						

**Figure 26. DAC enable control timing for Tx**

Fsync Polarity	Interleave	IQ Select (Rx)					
							
1	I,Q						
1	Q,I						
0	I,Q						
0	Q,I						

**Figure 27. ADC enable control timing for Rx**

### **DAC Edge**

DAC Edge – selects the active edge of the DAC clock. Negative is usually required.

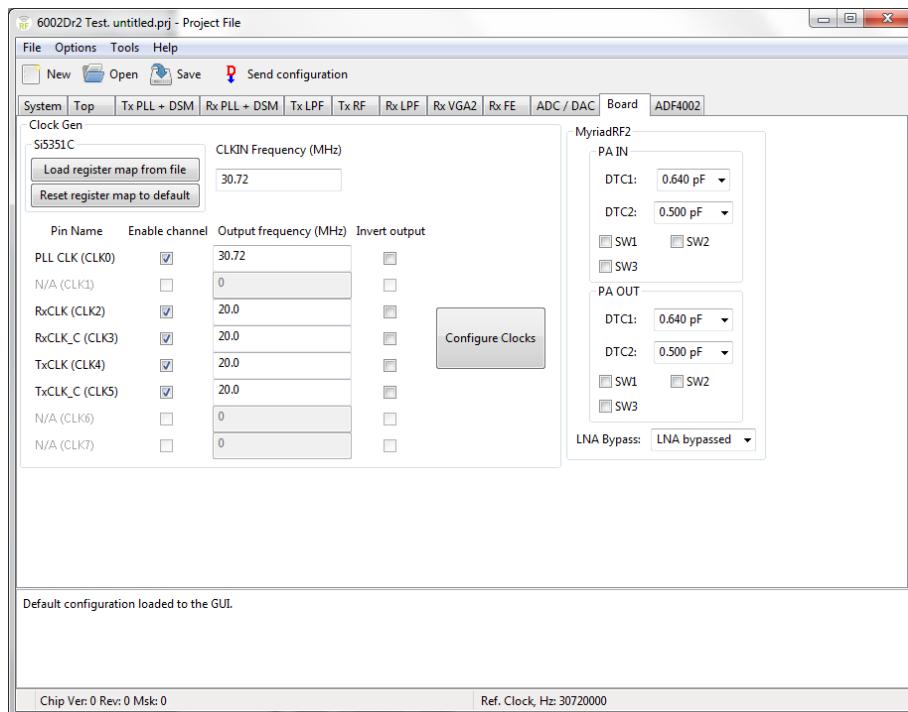
### **ADC Control**

Settings for ADC control are shown below, do not change:

- Input Buffer Disabled, leave as selected.
- Ref Bias Res Adj – ‘20uA’, leave it at default.
- Ref Bias UP –‘1.0X’, leave it at default.
- Ref Bias DN – ‘0’, leave it at default.
- Ref Buff Boost –‘1.0X’, leave it at default.
- Common Mode Adj , set to ‘960 mV’.
- Ref Gain Adj, set to ‘1.75V’.
- Main Bias DN – ‘0 (Nom)’, leave it at default.
- Clock Non-Overlap Adj –‘Nominal’, leave it at default.
- ADC Sampling Phase – ‘Rising Edge’, leave it at default.
- ADC Bias Resistor Adjust, uA –‘20’, leave it at default.
- ADC Amp1 Stage1 Bias Up, uA –‘20’, leave it at default.
- ADC Amp2-4 Stage1 Bias Up, uA –‘20’, leave it at default.
- ADC Amp1 Stage2 Bias Up, uA –‘20’, leave it at default.
- ADC Amp2-4 Stage2 Bias Up, uA –‘20’, leave it at default.
- Quantizer Bias Up, uA – ‘20’ , leave it at default.
- Input Buffer Bias Up, uA - ‘20’ , leave it at default.

### 3.5.11. Board

This page divided in two sections: Clock Gen and MyriadRF2. Clock Gen section provides control of the clock generator on the Zipper board, which generates the reference clock for the Myriad-RF board as well as for digital interface. MyriadRF2 section provides control of the tuners for external PA.



**Figure 28. Control window for on-board clock generator.**

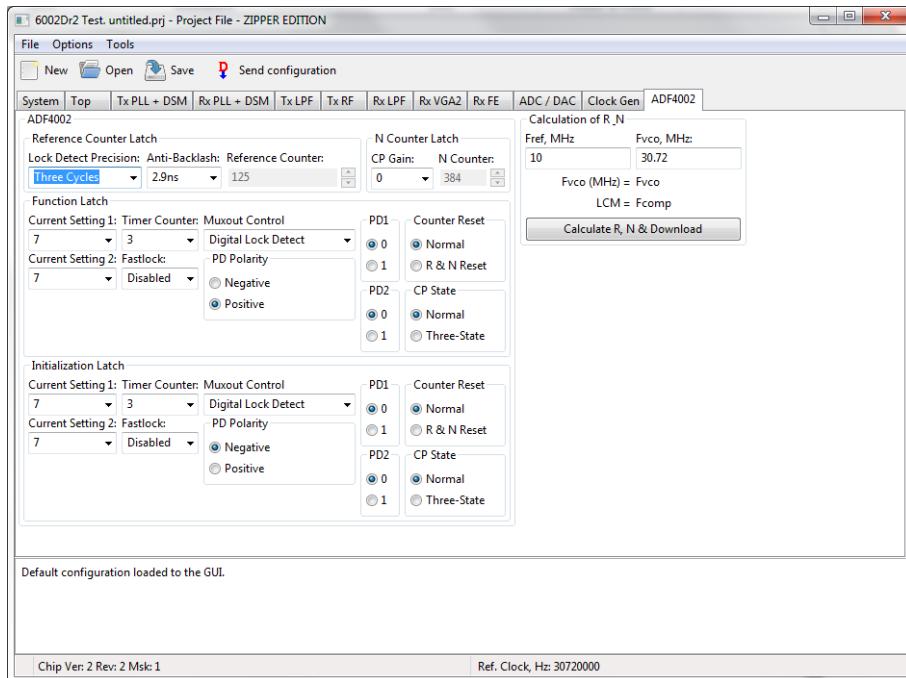
The default settings will program the standard board which is supplied with a 30.72MHz TCXO to output a PLL CLK of 30.72MHz and a digital interface running at 20 MHz. Please note that, with the default board configuration, the Myriad-RF 1 PLL CLK pin is supplied directly from TCXO. With a simple board modification PLL CLK can be supplied directly from the Si5351C clock generator. More information you can find in section 4.5.

Using this feature:

- Enable clock channel
- Enter the desired output frequency
- Press “Configure Clocks”
- Press “upload register map to Si5351C”

### 3.5.12. ADF4002

This page provides the SPI control via a second enable pin on the SPI interface for an external PLL chip. The purpose of this is so the interface TCXO can be locked to external test equipment if required.



**Figure 29. Control window for on-board ADF4002.**

The default settings will program the standard board with a 30.72MHz TCXO and a 10MHz reference. When the 10 MHz reference clock is connected to board J8 connector, press ‘Calculate R,N & Download’ button. If all is correct the green PLL locked LED (LD4) on the interface board should illuminate.

# 4

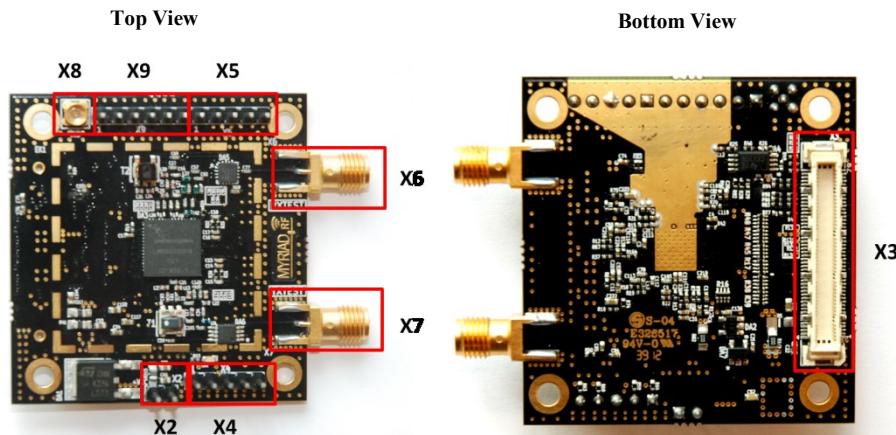
## Development Kit Connections

### 4.1 Basic Connections

The Myriad-RF 1 board can be used as a stand-alone board or in conjunction with the Zipper board. The Myriad-RF 1 board is connected to the Zipper board via the standard connector FX10A-80P. The following sections describe the connections on both boards as well as the overall functionality.

### 4.2 Myriad-RF 1 Board Connections

The analog differential IQ interface is also available on the Myriad-RF 1 board and provided via X4 and X5 connectors, see Figure 30. X6 and X7 are the RF connection for the receiver input and transmitter output respectively on the RF board, see Figure 30. The RF board is tuned to support band 1 (Tx 2140 MHz and Rx 1950 MHz) and broadband operation. The front end switches are configurable for the selected receiver input and transmitter output via GPIO's. The truth table for each selection mode (Rx and/or Tx) is shown in section 4.7.



**Figure 30. Myriad-RF 1 board connection descriptions.**

Myriad-RF 1 board connectors are described in the table below.

Connector	Name	Description
X2	+5 V supply	External +5 V supply.
X3	Digital I/O	The FX10A-80P is a standard connector used to interface the RF board directly to the interface board or any other baseband board.
X4	Tx Analog I/Q	Connector used to provide or get transmit analog I/Q signals.
X5	Rx Analog I/Q	Connector used to measure receiver analog I/Q signals.
X6	RXTEST	SMA connector provides connection to low band or high band Rx input. Requires preselected RF switch configuration.
X7	TXTEST	SMA connector that provides connection to low band or high band Tx output. Requires preselected RF switch configuration.
X8	Ext – CLK	Connector used to supply PLL clock externally.
X9	Ext – SPI	Connector used to control LMS6002D SPI registers externally. SPI registers are usually controlled via X3 connector.

**Table 3. Myriad-RF 1 Board Connector Assignments**

#### 4.2.1. X2 – +5V Supply Connector

The pin header type connector is used to supply +5 V (+/- 10%)-for the Myriad-RF 1 board in stand-alone mode.

#### 4.2.2. X3 – Digital I/O Connector

The Myriad-RF 1 board X3 connector (type FX10A-80P0) is pin compatible with the J1 connector on the interface board, see Figure 30. It provides the digital and SPI interface for the LMS6002D together with the supply voltage and GPIO control for the RF switches for the Myriad-RF 1 board. The pin descriptions on this connector are given in the table below:

Pin No	Pin Name	Type	Description
1	+5 V	in DC	+5 V power supply
2	+5 V	in DC	+5 V power supply
3	+5 V	in DC	+5 V power supply
4	+5 V	in DC	+5 V power supply
5	GND		Ground pin
6	GND		Ground pin
7	+3.3V +/- 5%	in DC	+3.3 V power supply optional
8	+3.3V	in DC	+3.3 V power supply optional
9	+3.3V	in DC	+3.3 V power supply optional
10	+3.3V	in DC	+3.3 V power supply optional
11	GND		Ground pin
12	GND		Ground pin
13	-		Not used
14	-		Not used
15	-		Not used
16	-		Not used
17	GND		Ground pin
18	GND		Ground pin
19	TXIQSEL	in cmos	TX digital interface IQ flag
20	-		Not used
21	-		Not used
22	-		Not used
23	TXD0	in cmos	DACs digital input, bit 0 (LSB)
24	TXD1	in cmos	DACs digital input, bit 1
25	TXD2	in cmos	DACs digital input, bit 2
26	TXD3	in cmos	DACs digital input, bit 3
27	GND		Ground pin
28	GND		Ground pin
29	TXD4	in cmos	DACs digital input, bit 4
30	TXD5	in cmos	DACs digital input, bit 5
31	TXD6	in cmos	DACs digital input, bit 6
32	TXD7	in cmos	DACs digital input, bit 7
33	TXD8	in cmos	DACs digital input, bit 8

34	TXD9	in cmos	DACs digital input, bit 9
35	TXD10	in cmos	DACs digital input, bit 10
36	TXD11	in cmos	DACs digital input, bit 11 (MSB)
37	GND		Ground pin
38	GND		Ground pin
39	RXIQSEL	out cmos	RX digital interface IQ flag
40	-		Not used
41	-		Not used
42	-		Not used
43	RXD0	out cmos	ADCs digital output, bit 0 (LSB)
44	RXD1	out cmos	ADCs digital output, bit 1
45	RXD2	out cmos	ADCs digital output, bit 2
46	RXD3	out cmos	ADCs digital output, bit 3
47	GND		Ground pin
48	GND		Ground pin
49	RXD4	out cmos	ADCs digital output, bit 4
50	RXD5	out cmos	ADCs digital output, bit 5
51	RXD6	out cmos	ADCs digital output, bit 6
52	RXD7	out cmos	ADCs digital output, bit 7
53	RXD8	out cmos	ADCs digital output, bit 8
54	RXD9	out cmos	ADCs digital output, bit 9
55	RXD10	out cmos	ADCs digital output, bit 10
56	RXD11	out cmos	ADCs digital output, bit 11 (MSB)
57	GND		Ground pin
58	GND		Ground pin
59	RXCLK	in cmos	RX digital interface clock
60	TXCLK	in cmos	TX digital interface clock
61	-		Not used
62	-		Not used
63	GND		Ground pin
64	GND		Ground pin
65	GPIO0		
66	RESET	in cmos	Hardware reset, active low
67	GPIO1		
68	SPI_MOSI	out cmos	Serial port data out
69	GPIO2		
70	SPI_MISO	in/out cmos	Serial port data in/out
71	-		Not used
72	SPI_CLK	in cmos	Serial port clock, positive edge sensitive
73	GND		Ground pin
74	SPI_NCSO	in cmos	Serial port enable, active low
75	CLK_IN	in cmos	PLL reference clock input

76	-		Not used
77	GND		Ground pin
78	-		Not used
79	TXEN	in cmos	Transmitter enable, active high
80	RXEN	in cmos	Receiver enable, active high
81	GND		Ground pin
82	GND		Ground pin
83	GND		Ground pin
84	GND		Ground pin
85	GND		Ground pin
86	GND		Ground pin
87	GND		Ground pin
88	GND		Ground pin

**Table 4. X3 connector pin description****4.2.3. X4 and X5 – Analog IQ Connectors**

Pin header type connectors on the Myriad-RF 1 board, provide analog IQ signals I/O.

**4.2.4. X6 and X7 – RF Input and Output**

The X6 and X7 are SMA type connectors which provide Receive input and Transmit output to the LMS6002D, respectively. These are generally used to connect to an antenna or test equipment.

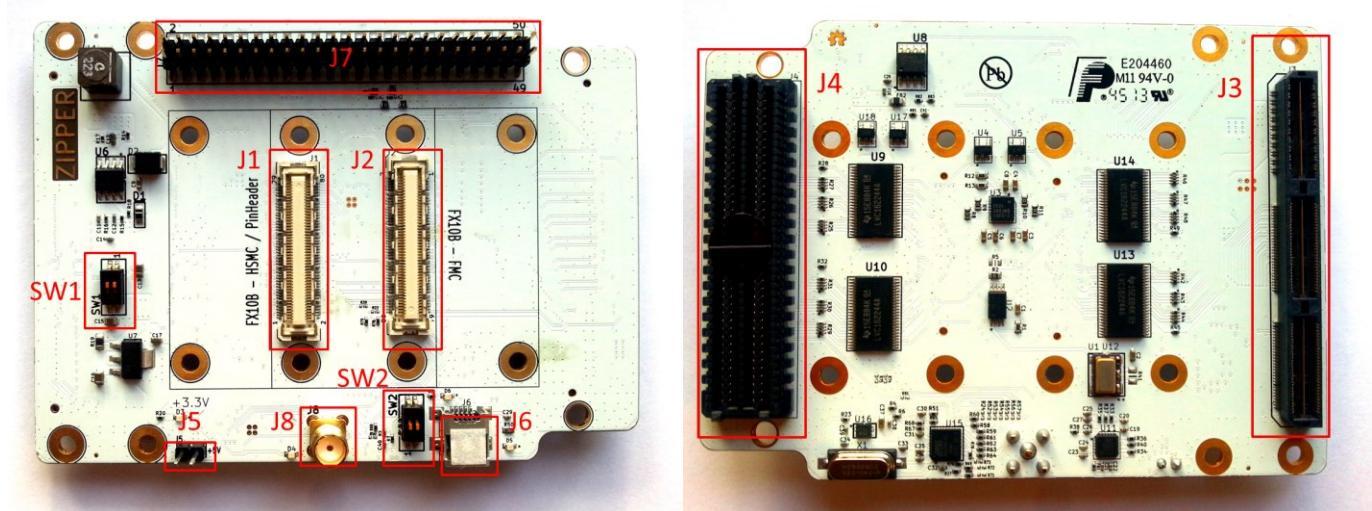
**4.2.5. X8 – External CLK Connector**

The X8 is a micro miniature coaxial connector (MMCX8400). It is optional and used to supply an external clock in stand-alone mode.

**4.2.6. X9 – External SPI Connector**

This is a pin header type connector used for the SPI interface to the LMS6002D. This is optional, if the board is used in stand-alone mode.

## 4.3 Zipper Board Connections



**Figure 31.** Zipper board connection descriptions.

The following table describes the Zipper board connectors.

Connector	Name	Description
J1	Myriad-RF 1 to HSMC and Pinheader	Connects the Myriad-RF 1 board with HSMC and the Pinheader via the FX10A-80P standard connector.
J2	Myriad-RF 1 to FMC and Pinheader	Connects the Myriad-RF 1 board with the FMC via the FX10A-80P standard connector.
J3	HSMC	HSMC standard Altera development kits connector, connected to all Myriad-RF 1 digital inputs/outputs.
J4	FMC	FMC standard Xilinx development kits connector, connected to all Myriad-RF 1 digital inputs/outputs.
J5	+5V	+5V input power connector.
J6	MiniUSB	USB connector. Provides +5 V supply for the Atmel microcontroller.
J7	Pinheader	All Myriad-RF 1 inputs/outputs are connected.
J8	SMA	Reference clock input for ADF4002 to lock the external clock from test equipment with DigiRED board clock.
SW1	+12V	When the switch is enabled, the Zipper board as well as Myriad-RF 1 board can be powered from +12V voltage supply via +5V regulator fitted on the board.
SW2	MCU	A hard reset switch for Atmel MCU

**Table 5** Zipper board connectors and switches.

#### 4.3.1. J1 and J2 – Digital I/O Connectors

The Myriad-RF 1 board is directly plugged into one of the FX10A-80P type connectors. The digital I/Q connector is a digital transmit (Tx) and receive (Rx) interface to the ADC/DAC of the LMS6002D. The SPI interface for the LMS6002D can also be established via the J1 and J2 connector.

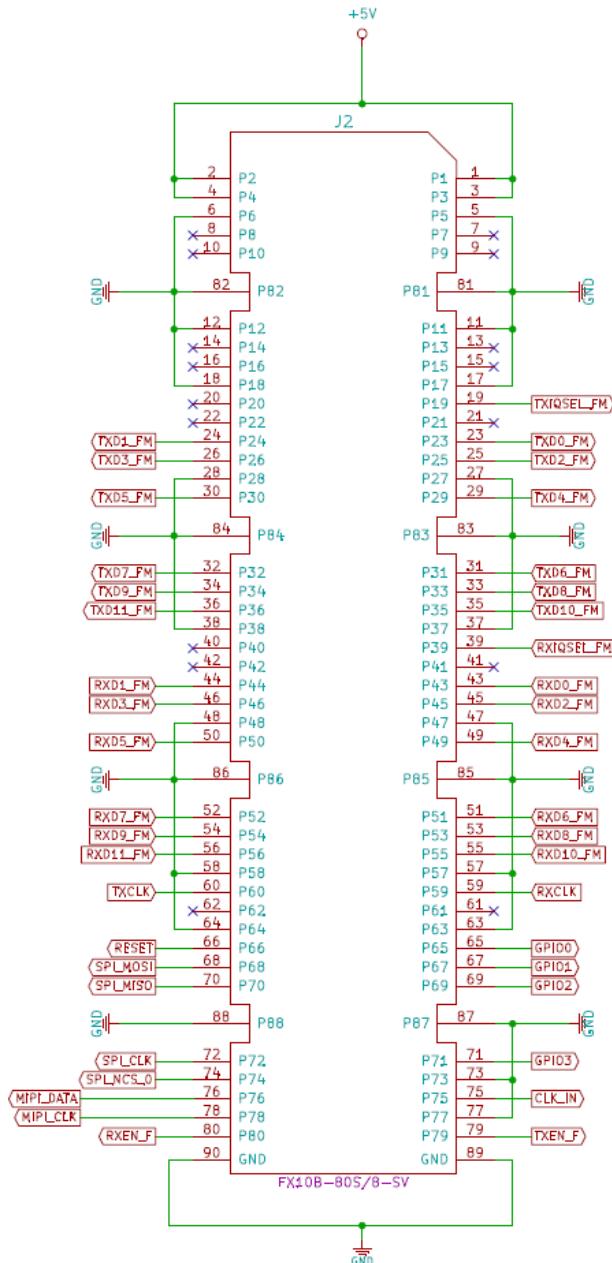


Figure 32. Digital I/O connector J2.

## 4.4 Hardware options: Clocking, SPI, GPIO truth table.

This section describes the configurations and setup procedures for:

- Reference frequency and data clocks distribution (Section 4.5).
- SPI interface configuration (Section 4.6).
- GPIO control truth table (Section 4.7).

The board is shipped in a default mode for basic operation. Various options are available depending on the system configuration required for testing or development work. The options are summarized below and the following sections describe the board modifications required to achieve these configurations.

## 4.5 Reference Frequency and Data Clocks Distribution

The Myriad-RF 1 provides a flexible clocking scheme which enables the PLL clock, Rx clock and Tx clock to be independently set.

The Zipper board is shipped with a default mode using the on-board 30.72MHz clock for the PLL clock only. The board can be reconfigured to allow users to provide a different clock frequency for the digital interface and the PLL clock using the programmable clock generator from Silicon Labs (Si5351C) which is capable of synthesizing four independent frequencies. The device outputs are connected independently to the LMS6002D PLL clock, Rx data interface clock and Tx data interface clock.

In order to reprogram the LMS6002D PLL frequency from the default setting of 30.72 MHz, please change the components on the Zipper board as given in the table below. Please note that NF denotes that the component is not fitted:

Reference clock options		
Component	Description Default mode. PLL clock set to 30.72 MHz	Programmable mode. PLL clock can be reprogrammed.
R2	0 Ohm	NF
R5	NF	0 Ohm

**Table 6. Reference clock configurations**

## 4.6 SPI Options

The Zipper board offers two options for the SPI, GPIO and MIPI RF communication with the Myriad-RF 1 board:

1. Communication established via USB interface (default configuration).
2. Communication established via J3, J4 or J7 connectors. In other words, from an external baseband.

In order to ensure stable communication for the desired option, the component changes on the Zipper board are given in the table below. Please note that NF denotes that the component is not fitted:

SPI Options				
SPI Line	Components	SPI via USB	SPI via J2, J4 or J7	Description
RESET	R60	0 Ohm	NF	
	R24	NF	0 Ohm	
SPI_MOSI	R62	0 Ohm	NF	
	R55	NF	0 Ohm	
SPI_MISO	R61	0 Ohm	NF	
	R54	NF	0 Ohm	
SPI_SCLK	R63	0 Ohm	NF	
	R56	NF	0 Ohm	
SPI_NCS0	R64	0 Ohm	NF	
	R57	NF	0 Ohm	
SPI_NCS_1	R59	0 Ohm	NF	Master enable for ADF4002 SPI interface
	R53	NF	0 Ohm	
SPI_NCS_2	R58	0 Ohm	NF	Master enable for Si5351 SPI interface
	R52	NF	0 Ohm	
GPIO 0	R68	0 Ohm	NF	GPIO for RF switch, controlled via GUI.
	R71	NF	0 Ohm	
GPIO 1	R69	0 Ohm	NF	GPIO for RF switch, controlled via GUI.
	R72	NF	0 Ohm	
GPIO 2	R70	0 Ohm	NF	GPIO for RF switch, controlled via GUI.
	R73	NF	0 Ohm	
GPIO 3	R80	0 Ohm	NF	GPIO for RF switch, controlled via GUI.
	R90	NF	0 Ohm	
MIPI_DATA	R79	0 Ohm	NF	MIPI RF devices controlled via GUI.
	R39	NF	0 Ohm	
MIPI_CLK	R78	0 Ohm	NF	MIPI RF devices controlled via GUI.
	R22	NF	0 Ohm	

Table 7. SPI configuration table

## 4.7 GPIO control truth table

The RF switches on the Myriad-RF 1 board are controlled via the GPIO 0-3 logic signals. This enables the user to choose RF input/output depending on the operational frequency. The truth table of the GPIO 0-2 settings is shown below.

LMS6002D RF Input/output	GPIO 0	GPIO 1	GPIO 2	GPIO 3	Description
Tx out 1	X	X	0	X	High band output (1500 – 3800 MHz)
Tx out 2	X	X	1	X	Broadband output
Rx in 1	1	1	X	0	Low band input (300 – 2200 MHz)
Rx in 2	0	1	X	0	High band input (1500-3800MHz)
Rx in 3	0	0	X	0	Broadband input

**Table 8. GPIO truth table**

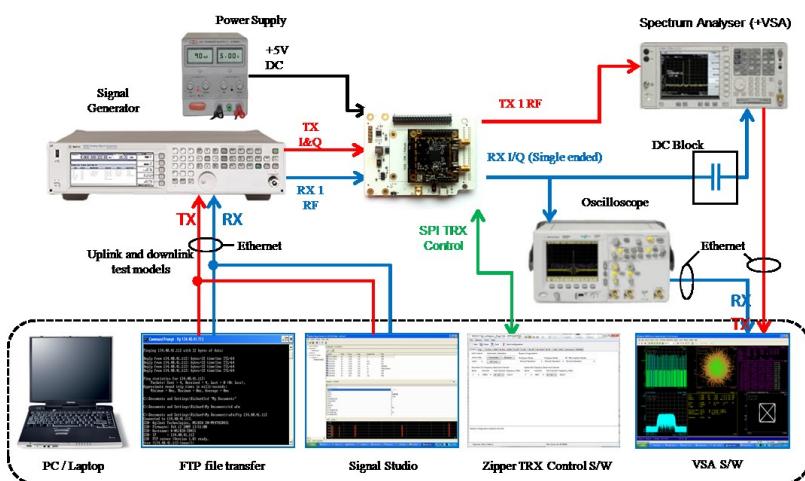
# 5

## Test System Connections

The combination of the Myriad RF 1 board and the Zipper board allows the user to select the following test system combinations: IQ signals applied/measured to the Myriad RF 1 board via the Analog Inputs/Outputs; IQ signals applied to the Myriad RF 1 board via the digital interface.

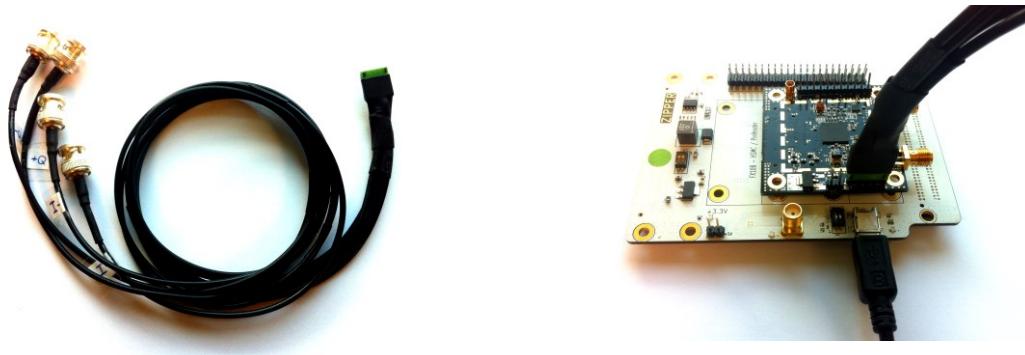
### 5.1 Test system using IQ Analog Inputs/Outputs

The system connections using IQ Analog inputs/outputs are used shown in the figure below.



**Figure 33. Test system connections to test receiver and transmitter via analog inputs/outputs.**

There is a specially made coaxial cable to connect the Tx IQ analog inputs with the signal generator IQ modulator outputs (standard BNC connection). The cable connects to the Myriad RF 1 X4 connector, see Figure 34.

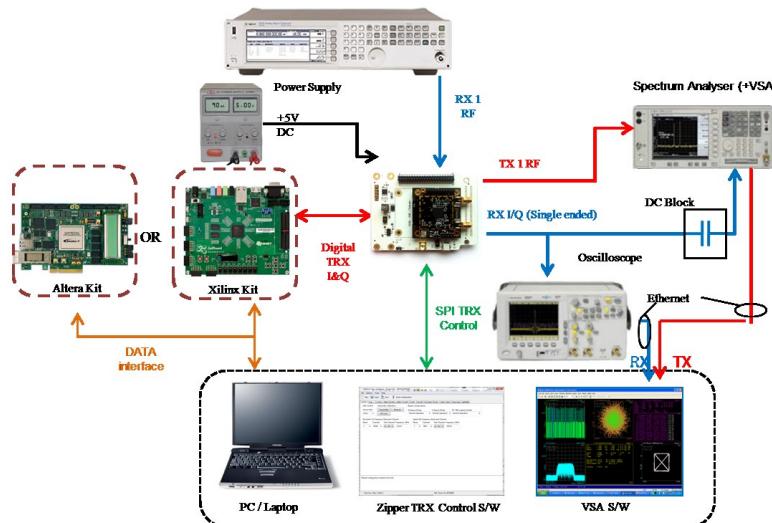


**Figure 34.** Tx IQ analog cable to connect to the MXG IQ modulator, on the left. The same cable connected to the Myriad RF 1 board X4 connector.

The signal generator setup to drive the Tx IQ Analog inputs is described in chapter 7.1.

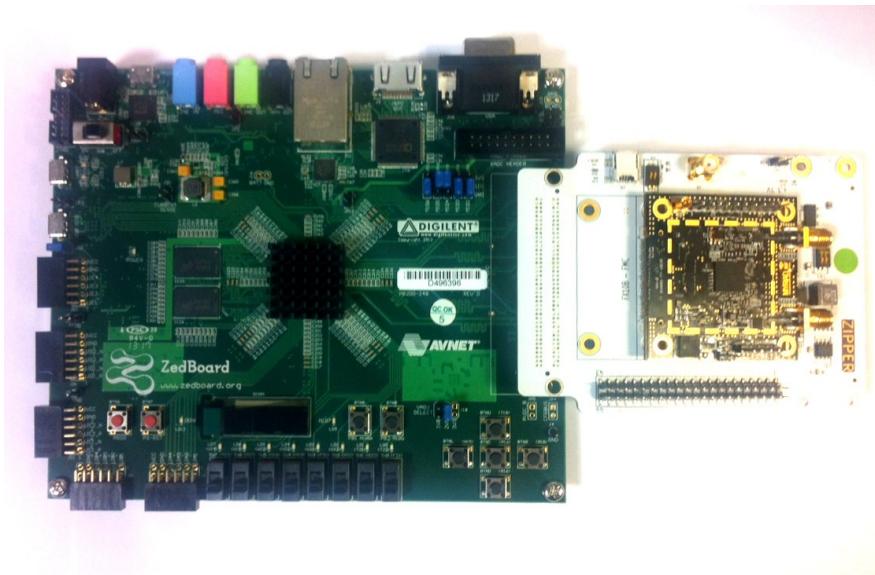
## 5.2 Test system using digital interface

The system connections to supply digital data to the Myriad RF 1 board are shown in the figure below.



**Figure 35.** Test system connections with digital interface.

The Zipper board can interface with the Myriad RF 1 and various baseband processing options such as Xilinx development kits or Altera development kits via the digital interface. The figure below shows the interconnection of the Zedboard (Xilinx development kit) with the Zipper and Myriad RF 1 boards via the FMC interface..



**Figure 36. Zipper and Myriad RF 1 board connected to a Zedboard.**

# 6

## Myriad RF 1 Calibration Procedures

### 6.1 Tx LO Leakage Calibration

This procedure assumes the transmitter has been turned on and initialized, it describes how to use the parameters within the LMS6002D to cancel any LO leakage from the IQ modulator.

It is intended that this will be a single point calibration per band, the example given uses 3GPP Band I with a centre frequency of 2140 MHz.

The transmitter should be set up with the following parameters:

Parameter	Page	Value
Transmitter Frequency	System Interface	2140
Soft Tx enable	Top Level	Tick box selected
Tx DSM SPI clock buffer	Top Level	Tick box selected
LPF bandwidth	Tx LPF	3.5MHz
PA1 selected	Tx RF	PA1 Selected
VGA1 gain	Tx RF	-10
VGA2 gain	Tx RF	15

**Table 9 Transmitter setup**

No signal should be applied to the DAC's. For a better result, all '0' can be generated by the BB and applied to the DACs.

**Note:** Set gain settings before calibration.

The output should be observed on a spectrum analyzer. The following measurements were taken using an Agilent N5181A MXG RF instrument. The signal on the screen represents the LO feedthrough from the transmit modulator. In this case the level is -45dBm, see figure below.

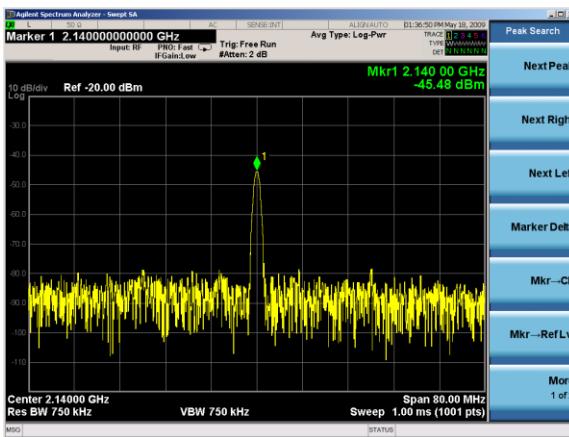


Figure 37. Transmit Output

Assuming that the LPF Core calibration has been carried out in the initialization, then press the ‘Transmitter’ button on the System tab in the Automatic Calibration area.

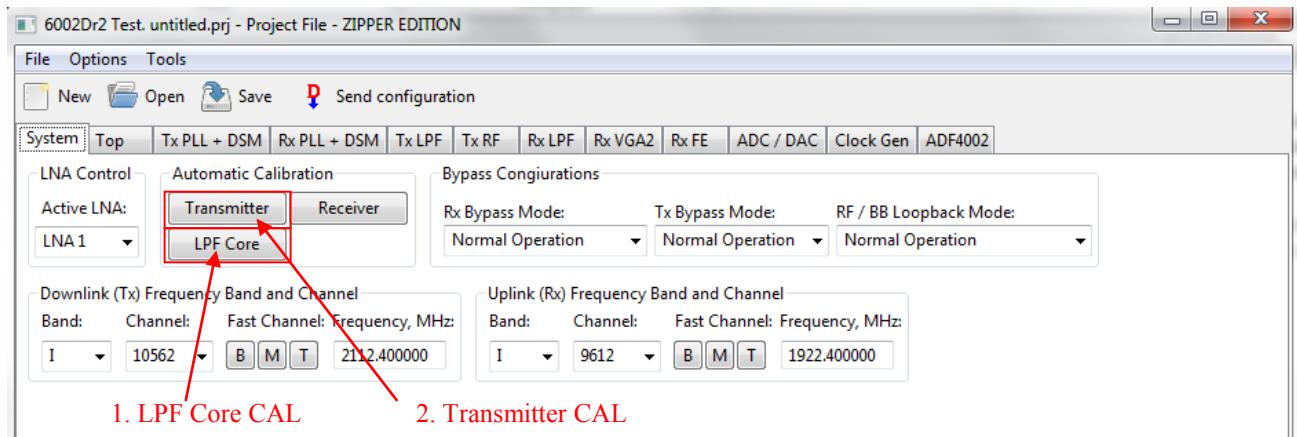


Figure 38. System Window. Use Automated Calibration

‘Tx Calibration Done’ should appear in the text box at the bottom of the display. In this case the LO level dropped after automatic calibration to -53dBm as shown in the figure below.

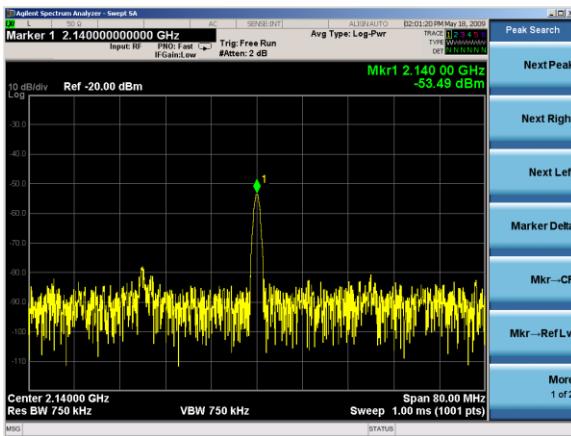


Figure 39. Transmit Output after calibration

Automatic calibration is intended to calibrate the DC offset at the output of the internal LPF. This is not the same as canceling the LO, it just makes the DC contribution from the IQ chain as low as possible. It may be the case that the level will go up after automatic calibration – do not worry if it does, this is due to the default values on power up canceling the LO at the selected frequency.

The next step is to calibrate the residual LO leakage using the ‘LO leakage DAC Out’ registers controlled via the GUI. Select the ‘Tx RF’ page in the Zipper software.

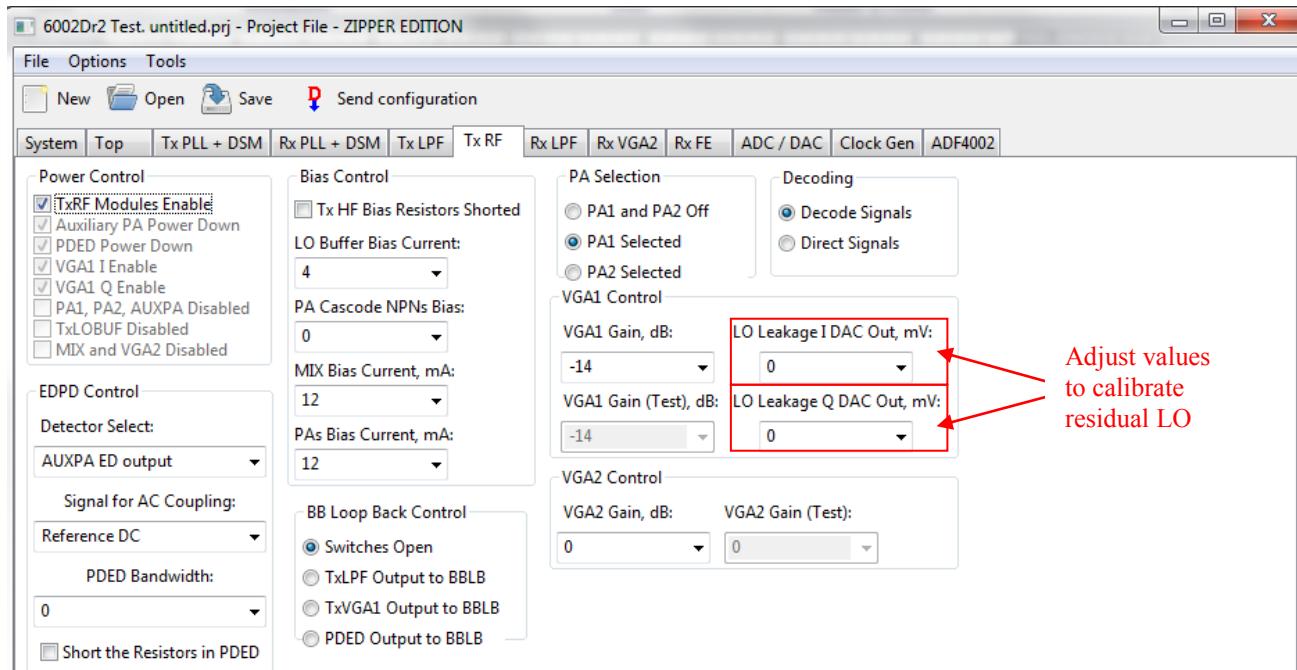


Figure 40. Tx RF window

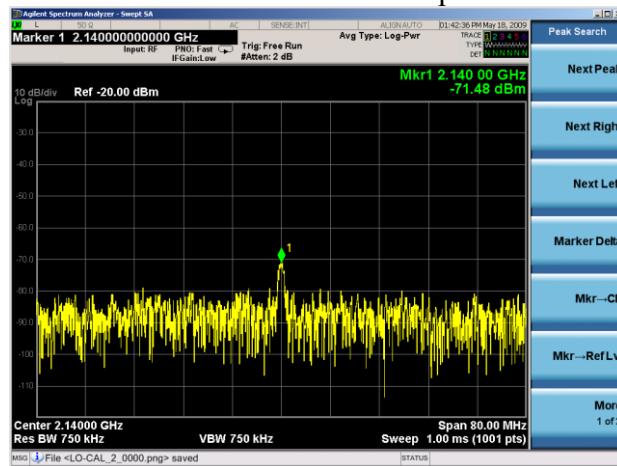
The LO cancellation levels for the DACs are displayed in the boxes marked ‘LO Leakage DAC I Out’ and ‘LO Leakage DAC Q Out’. The entry mechanism is different to the LPF DC offset and easier to tune.

The LO Leakage DAC I/Q Out boxes contain the value of the DC LO cancellation DAC in mV and the level ranges from -16 to 15.875.

Click on the LO Leakage DAC I/Q Out shift box to cause a drop down menu to appear. Click again and the drop down menu collapses leaving the entry box blue.

The value in the box can now be adjusted using the up and down arrows on the key board. Once the number has changed, the register in the LMS6002D is updated, allowing for a simpler search method as shown below:

- a. Select the I DAC box
- b. Increase/decrease until the minimum is found.
- c. Do the same for Q.
- d. It is possible that 0 is the best result for both as the optimum calibration value.



**Figure 41. Transmit output after calibration**

In the example, the LO cancellation has been improved to -71dBm as shown in this figure. The optimum values were:

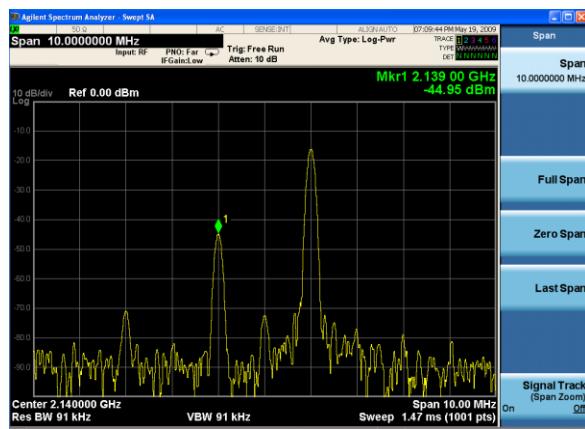
$$\begin{aligned}I &= 0 \\Q &= -0.125\end{aligned}$$

Each LMS6002D device will have its own optimum calibration values.

## 6.2 Transmit I/Q Balance Calibration

This procedure assumes the Tx LO calibration procedure in section 6.1 has been completed. The purpose of this calibration is to optimize the I/Q balance for optimum transmit Error Vector Magnitude (EVM) performance. Typically, this is done by applying a 1 MHz CW tone from a digital I/O card through the digital interface at J7. The 1 MHz CW tone could also be applied at the Myriad RF 1 X4 connector from a differential I/Q analog signal generator. For more information on the generator setup and calibration procedure can be found in section 7.1.

Initially, the user should observe a spectrum at the tuned frequency which is similar to the figure below Figure 42.



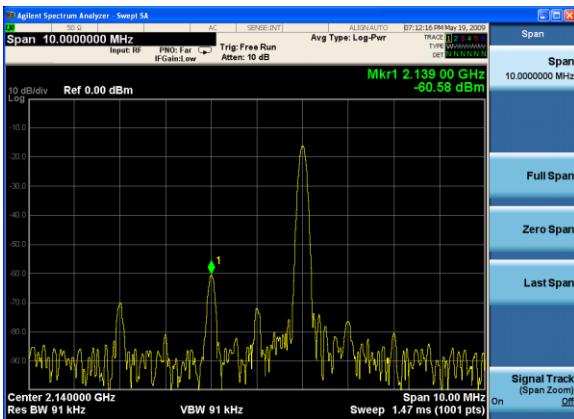
**Figure 42. Initial -1 MHz Image Spectrum**

The wanted signal can be seen at a 1MHz offset from the selected RF frequency (2140MHz), In this case at a level of approx. -16dBm.

The unwanted (lower) sideband can be seen at -1 MHz offset. With no correction, it is at a level of -45dBm (29dBc). The image or sideband rejection performance of the system depends upon the phase and gain match of the I and Q paths. This includes the test equipment, cables and, of course, the LMS6002D transmit path. Keep the cable lengths short between the signal generator and the test board.

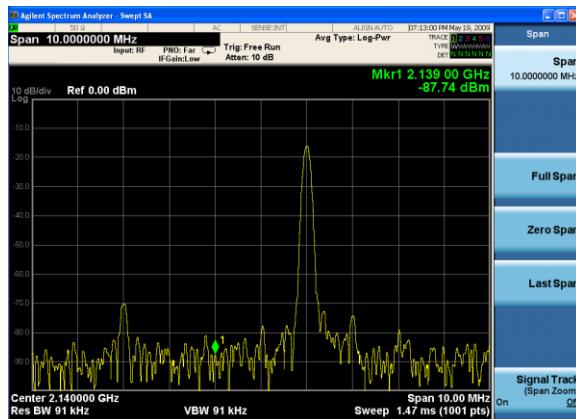
The phase match also depends on the accuracy of the sin/cosine split on the LO of the IQ modulator (inside the LMS6002D). The bulk of the phase correction is for this parameter – hence, any amplitude mismatch with frequency will be small, however the phase mismatch may differ for each band.

Following the phase angle calibration, the resultant spectrum is shown in the Figure 43. The unwanted sideband has been reduced to -60dBm (-44dBc). The optimum value found in this case was 4.1 deg.



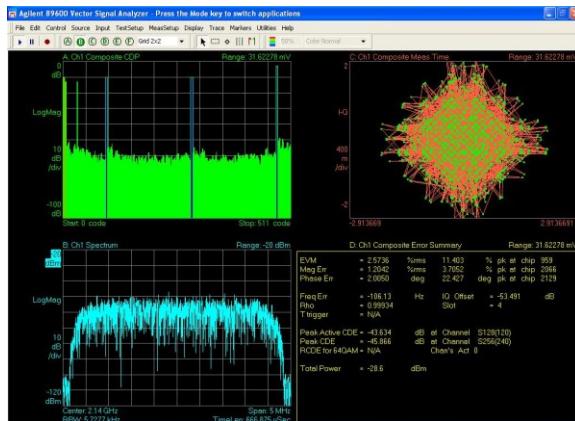
**Figure 43. Phase angle calibration**

The result of the amplitude balance calibration is shown in Figure 47. The unwanted sideband has been reduced to < -80dBm (-64dBc). The optimum value found in this case was 0.11 dB.



**Figure 44. Amplitude balance calibration**

If necessary, repeat the phase and amplitude adjustments until the optimum values are found and an  $EVM \leq 3.5\%$  is measured as shown below. The transmit I/Q balance calibration is valid on the flat part of the LPF bandwidth. As you approach the LPF corner frequency the lower sideband cancellation will begin to degrade. For example, with the 1 MHz tone used in this calibration the EVM will degrade as the filter bandwidth decreases below 1.92 MHz.



**Figure 45.** Transmit EVM performance after calibration

With a WCDMA TM2 waveform applied to the Myriad RF 1 analog input, and using the Vector Signal Analysis (VSA) analysis software, the performance results were recorded as:

EVM 2.5%

Peak Code Domain Error (CDE) -45 dB

**Note:** The EVM is dependent on a number of parameters being set up correctly. Phase noise performance of the LO is the dominant factor in the above measurement.

### 6.3 Receiver DC Calibration

The receiver has a number of self-calibration routines which are designed to cancel out DC offsets from the LPF's and the VGA's. It is similar to calibration in the transmit path where the low LO levels are easy to measure with the spectrum analyzer, but low DC levels are more difficult to measure.

In most cases the baseband (BB) processor is capable of adjusting the DC calibration (and also the IQ phase and amplitude match) based on measurements of the uplink signal. It is only necessary to ensure the calibration is good enough so that the ADC is not saturated.

However, for testing without the BB, the following procedure has been devised. This method uses the I and Q samples from the oscilloscope. The Agilent VSA software is used to sample the oscilloscope and display the spectrum. The oscilloscope used for this procedure must be supported by the Agilent VSA software. The spectrum analyzer cannot be used because it cannot display DC.

The receiver calibration procedure steps are:

1. Set the receiver up for the desired frequency at “TxPLL + DSM” window.
2. Set the receiver path for maximum gain (VGA1 120, VGA2 30 dB, LNA max gain). The uncalibrated Rx LO leakage is shown in Figure 46.

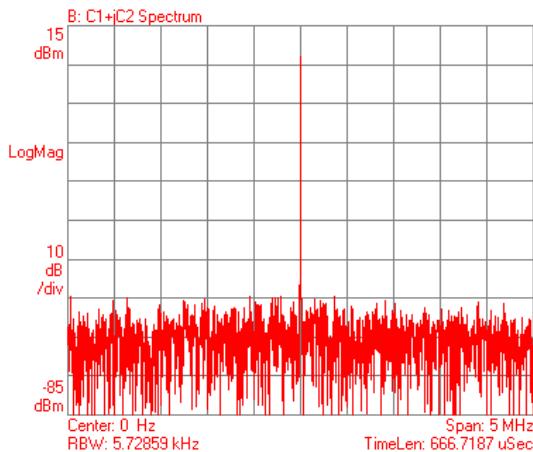


Figure 46. Receiver LO leakage

3. Execute automatic DC calibration routines for the receive path in the “System” interface.

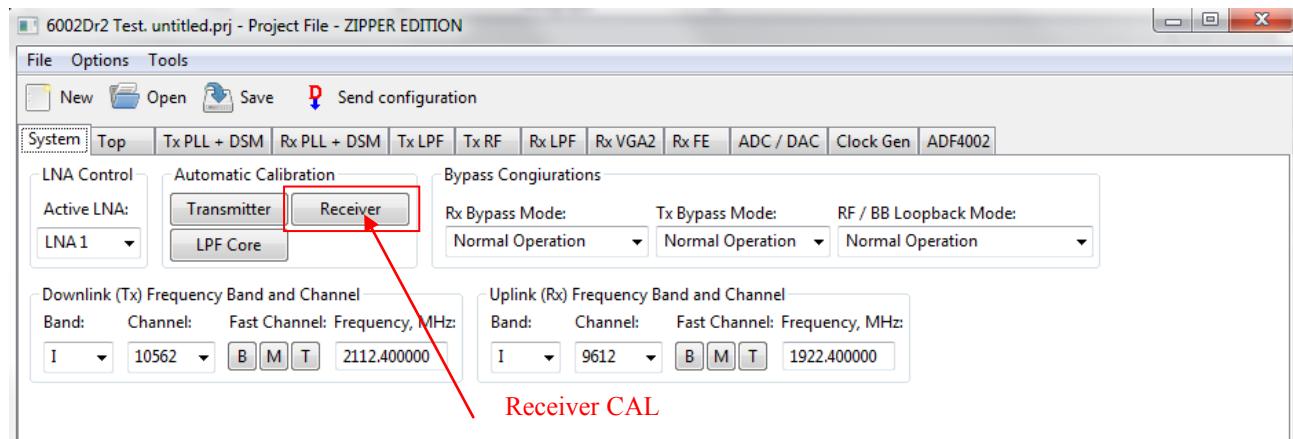
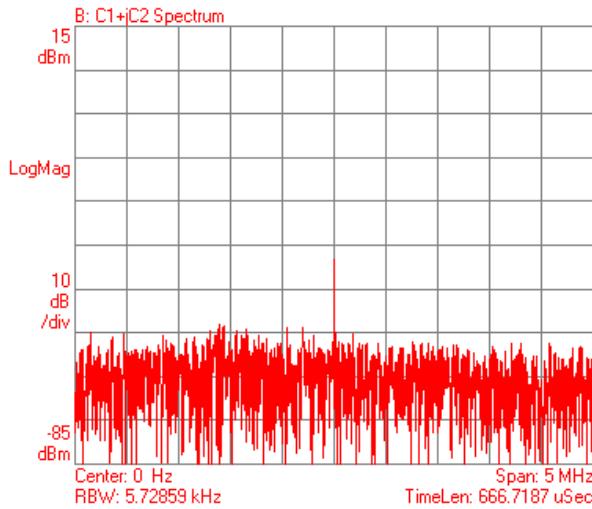


Figure 47. Execute receiver internal DC auto calibration routines

The DC offset level should drop as shown in Figure 48.



**Figure 48. Rx LO leakage after calibration**

For further DC offset improvement implement the DC cancellation filter in the baseband.

## 6.4 Calibration Process Summary

There are several similarities between the receive and transmit DC calibration processes but there is one fundamental difference. During the transmit calibration process no signal can be applied to the input of the transmitter. An automated DC calibration is performed to ensure the BB stages contribute no DC offset to the LO leakage calibration. Finally, an LO leakage calibration is performed to minimise LO leakage. The transmit input must be zero so that the automated DC calibration can find the correct minimum DC point. This DC calibration process provides optimum transmitter performance.

In the receiver a similar DC calibration process is applied but in reverse order. When no signal is applied at the input of the receiver, the resulting DC offsets at the receiver outputs are due to LO leakage (multiplied by the RX gain) and the DC offsets in the LPFs and VGAs. The DC offset calibration routines will remove the DC offset contribution from the LPFs and VGAs. This calibration process will result in minimum DC offset in the receiver and optimum sensitivity and dynamic range.

# 7

## Signal Generator Setup

This chapter uses the Agilent N5182A MXG signal generator with an arbitrary waveform generator and the differential I/Q outputs option (1EL). Other signal generators can be used. However, some issues may arise if the options available for IQ amplitude and phase manipulation, which comes with the MXG, are not supported.

### 7.1 Agilent MXG Setup

The front panel of the MXG is as follows:

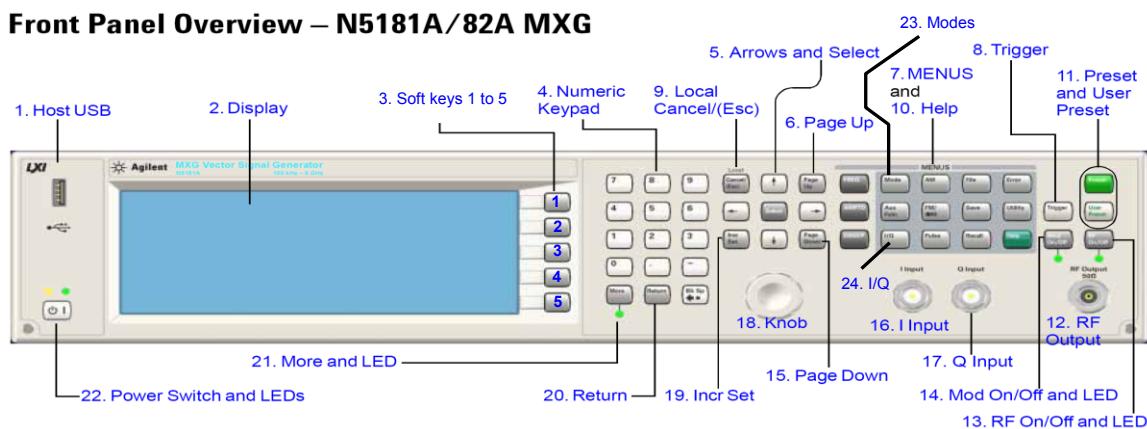


Figure 49. Agilent N5181A/82A MXG Front Panel

### 7.1.1. Apply 0.6V common mode offset on IQ outputs

The LMS6002D Analog inputs require a 0.6V common mode offset voltage with a 300 mVp-p voltage swing for optimum performance.

To apply the common mode offset voltage:

1. Press 'IQ' button (24)
2. Press 'IQ offsets (on/off)' softkey (3. softkey 4)
3. Press 'external output adjustments' softkey (3. softkey 4)
4. Press 'Common Mode I/Q offset' softkey (3. softkey 2)
5. type 0.6 on number pad (4), press 'V' softkey (3. softkey 1)
6. 0.6V should appear on the display next to the 'Common Mode I/Q offset' softkey
7. Press return
  - i. Check that the text next to 'I/Q Adjustments' softkey (3. softkey 1) highlights 'off/on'
  - ii. If not, press 'I/Q Adjustments' softkey (3. softkey 1), the highlighted section should toggle between on and off when pressed.
  - iii. press return
  - iv. Check that the text next to 'I/Q' softkey (3. softkey 1) highlights 'off/on'
  - v. If not, press 'I/Q' softkey (3. softkey 1), the highlighted section should alternate between on and off when pressed.

There should now be a 0.6V common mode voltage on the differential IQ connections on the signal generator. This can be verified by measuring the DC level of each of the 4 differential I/Q lines with a multimeter.

**Note:** Very small DC offset levels in the transmit IQ path can result in LO breakthrough levels changing in the transmit chain. To eliminate or minimize this effect the following practices should be followed:

- IQ cables should be of equal length.
- Once the I/Q gain and phase calibration is completed, the connections should not be modified.
- Cables and connections should not be moved once the I/Q gain and phase calibration is completed. Otherwise it might affect the calibration.

In practice the LMS6002D chip will be soldered to a PCB and connected to a baseband processor so this is purely a test issue.

### 7.1.2. Turn on the arbitrary waveform generator

The arbitrary waveform generator will run test vectors which are downloaded to it via either the ‘Signal Studio’ program from the Agilent equipment or test vectors which can be generated independently via ‘Matlab’ or C.

The MyriadRF website (<http://myriadrf.org/>) has a number of test vector files which are used for test and calibration of the LMS6002D as follows:

- DC.wfm - DC tone for Tx CW testing (clock 52MHz).
- onetone1.wfm - single tone at 1MHz offset for sideband suppression calibration/test (clock 52MHz).
- twotone.wfm - two tone signal for linearity testing for MXG and LMS6002D use MXG IQ scaling factor of 30% (clock 52MHz).
- wcdma31.wfm - TM2 WCDMA signal - use MXG IQ scaling factor of 30% (clock=15.36MHz).
- EDGE3.wfm - GSM EDGE modulated test signal - (clock=13MHz).

To download files to the signal generator follow the process described in 7.2 section.

To apply the correct file

1. Press ‘Mode’ button (23)
2. Press ‘Dual Arb’ softkey (3. softkey 1)
3. Press ‘Select waveform’ softkey (3. softkey 2)
4. Use up/down arrows (5) or spin knob (18) to select the wanted waveform from the list.
5. Press ‘Select waveform’ softkey (3. softkey 1)
6. The name of the selected waveform should now be present in the display window
7. The soft key list should have moved up one level back to ‘Arb’
8. Now change the Arb clock frequency
9. Press ‘Arb setup’ softkey (3. softkey 3)
10. Press ‘Arb sample clock’ softkey (3. softkey 1)
11. Type in the required frequency on the number pad e.g. for 13MHz type ‘13’ and press ‘MHz’ softkey (3. softkey 2)
12. The sample clock frequency should now be displayed on the screen.
13. Now scale the waveform data if necessary
14. Go to ‘Arb’ softkey menu
  - a. Either press ‘return’ button from ‘Arb setup’ menu or
  - b. Press ‘Mode’ button then ‘Dual Arb softkey (3. softkey 1)
15. Press ‘More’ button (21)

16. Press ‘Waveform Utilities’ softkey (3. softkey 2)
17. Use the up/down arrows (5) or spin the wheel to **highlight** the wanted waveform from the list.
18. Press the ‘scale waveform data’ softkey (3. softkey 2)
19. Type in the required scaling factor e.g. for 25%, type ’25’ on the number pad and press the ‘%’ softkey (3. softkey 1).  
**Note** – even if the text next to the ‘scaling’ softkey already states 25% (for example) this does not mean it has been applied to the waveform, so you should still follow process.
20. Press ‘Apply to waveform’ softkey (3. softkey 4)
21. The progress bar will show on the screen, and the soft menu will return to a level up (Arb utilities).
22. Now return to the main ‘Arb’ Menu
  - a. Press the ‘return’ button twice or
  - b. Press the ‘Mode’ button then ‘Dual Arb softkey (3. softkey 1)
23. Check that Arb is enabled
  - a. The ‘Arb on/off’ softkey (3. softkey 1) text should have highlighted ‘Off / **On**’
  - b. If not press the ‘Arb on/off’ softkey (3. softkey 1) to toggle between on and off.
24. The modulation can be also be toggled on and off by the ‘Mod on/off’ button (just above the RF o/p connector). This must also be on – and the green LED must be illuminated.
  - a. Press the ‘Mod on/off’ button to toggle the modulation on and off.  
**Note** – The Mod on/off button turns the modulation onto the RF and IQ outputs simultaneously. The RF does not need to be on for the IQ outputs to work

## 7.2 Downloading \*.wfm Files to the Signal Generator

The following process should allow you to download files to the Agilent signal generator. The same process works for MXG and ESG.

This can be done via a network, however these instructions assume a direct connection between a PC running windows XP and the signal generator.

- Connect a cable between the PC network port and the signal generator LAN port.
- Check that the LEDs are illuminated on both ends to indicate that the HW is connected.
- Find the IP address of the Signal generator
  - Press the ‘Utility’ button
  - Press the ‘I/O config’ softkey (3. softkey 1)
  - Press the ‘LAN setup’ softkey (3. softkey 2)
  - The IP address should now be displayed on the screen
  - e.g.  
IP Address : 134.40.41.112  
Subnet Mask : 255.255.255.0
- On the PC, open the ‘Local Area Connection Properties’ box
  - Select Internet Protocol (TCP/IP)

- Press the ‘Properties’ button
- Select ‘Use the following IP address’ tick box
- Set the IP address to one close to the sig gen, in this case: 134.40.41.122
- Set the subnet mask to the same as sig gen, in this case 255.255.255.0
- Press ok on both of the open dialog boxes.
- Open a Command Prompt window
  - Start
  - All programs
  - Accessories
  - Command Prompt
- To check the connection to the signal generator attempt to ‘ping’ it
  - Type ‘ping 134.40.41.112’ (or use your sig gen IP address)
- A successful ping result should be returned as shown below.

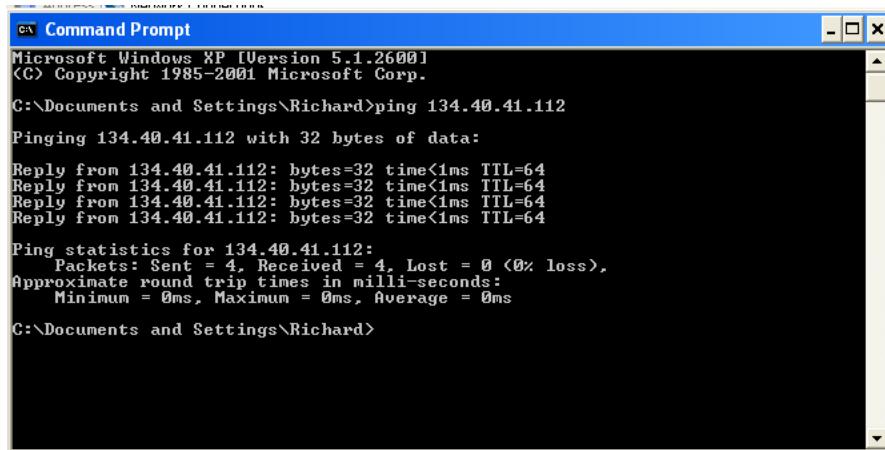
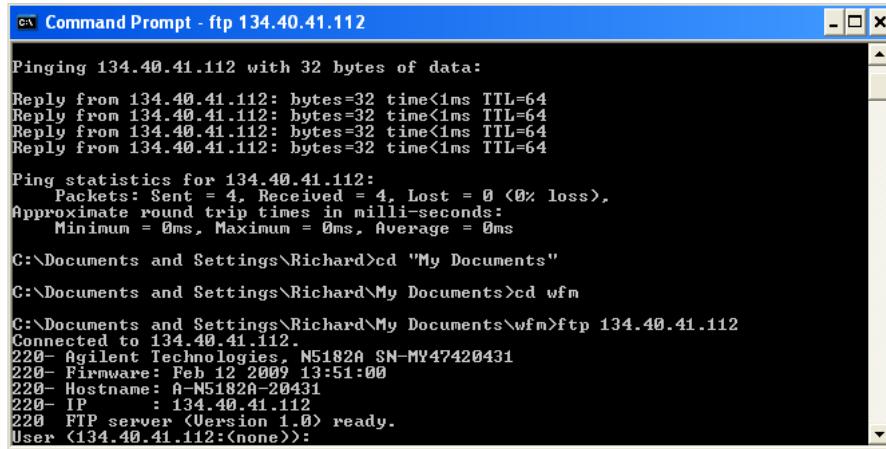


Figure 50. Command Prompt window. Connection check.

To send wfm files to the signal generator, the following procedure should be followed.

- Ensure that the wfm files are in a known directory e.g. ‘C:\Documents and Settings\User\My Documents\wfm’.
- In the ‘Command Prompt’ window set the directory to the one where the wfm files are located.
- Use FTP to send files to the signal generator
- Type ‘ftp 134.40.41.112’



```

Command Prompt - ftp 134.40.41.112
Ping statistics for 134.40.41.112 with 32 bytes of data:
Reply from 134.40.41.112: bytes=32 time<1ms TTL=64

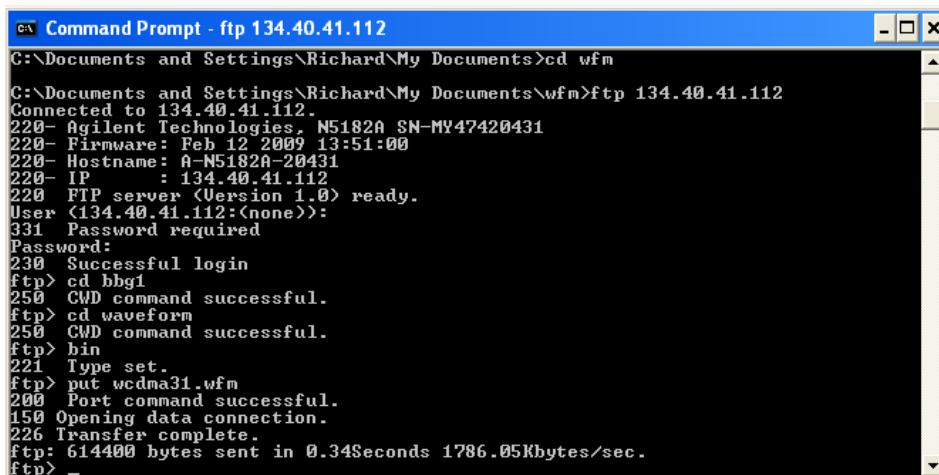
Ping statistics for 134.40.41.112:
    Packets: Sent = 4, Received = 4, Lost = 0 (0% loss),
Approximate round trip times in milli-seconds:
    Minimum = 0ms, Maximum = 0ms, Average = 0ms

C:\Documents and Settings\Richard>cd "My Documents"
C:\Documents and Settings\Richard>cd wfm

C:\Documents and Settings\Richard>My Documents>ftp 134.40.41.112
Connected to 134.40.41.112.
220- Agilent Technologies, N5182A SN-MY47420431
220- Firmware: Feb 12 2009 13:51:00
220- Hostname: A-N5182A-20431
220- IP      : 134.40.41.112
220- FTP server <Version 1.0> ready.
User <134.40.41.112:<none>>:
```

**Figure 51. Command Prompt window. Establish FTP connection.**

- If you are correctly connected, then the above should be returned.
- Press ‘return’ twice (for user name and password – none needed)
- Type ‘cd bbg1’
- Type ‘cd waveform’
- Type ‘bin’
- Type ‘put wcdma31.wfm’
- The command copies the files to the signal generator – repeat the ‘put’ command for all files needed.



```

Command Prompt - ftp 134.40.41.112
C:\Documents and Settings\Richard>cd wfm
C:\Documents and Settings\Richard>My Documents>ftp 134.40.41.112
Connected to 134.40.41.112.
220- Agilent Technologies, N5182A SN-MY47420431
220- Firmware: Feb 12 2009 13:51:00
220- Hostname: A-N5182A-20431
220- IP      : 134.40.41.112
220- FTP server <Version 1.0> ready.
User <134.40.41.112:<none>>:
331 Password required
Password:
230 Successful login
ftp> cd bbg1
250 CWD command successful.
ftp> cd waveform
250 CWD command successful.
ftp> bin
221 Type set.
ftp> put wcdma31.wfm
200 Port command successful.
150 Opening data connection.
226 Transfer complete.
ftp: 614400 bytes sent in 0.34Seconds 1786.05Kbytes/sec.
ftp>
```

**Figure 52. Command Prompt window. Send waveform to generator.**

- To exit the ftp program type “bye”.
- To close the ‘Command Prompt’ window type exit.
- The wfm files should now be visible in the list of Arb files.