1. Screenshot of Modelsim/Questa output (last page of transcript/console).

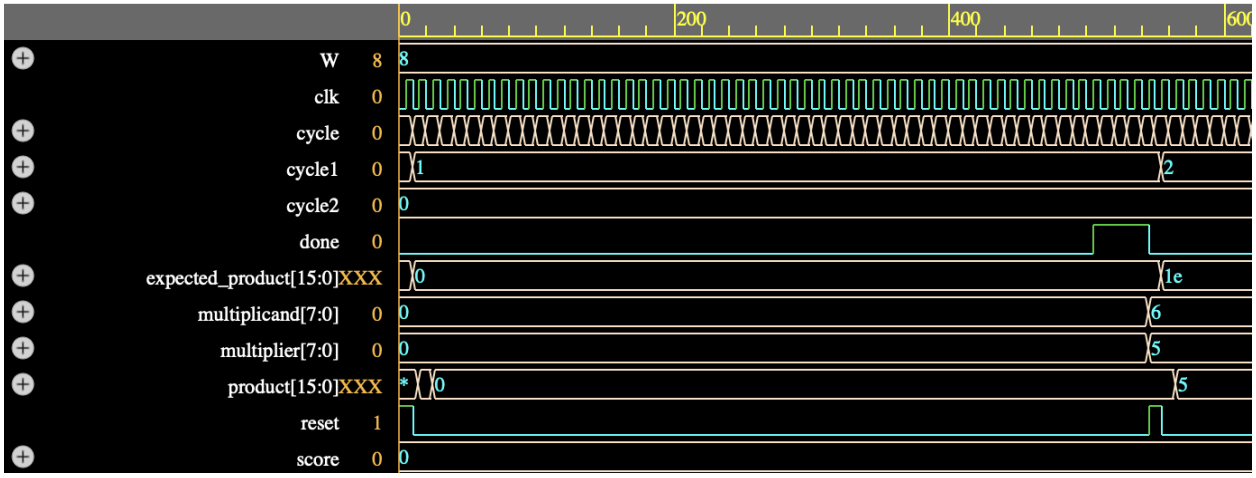
The screenshot should show your output vs the expected output. It should also show the score.

```
# run -all
# Simulation succeeded 0000 = 0000 = 00 * 00
# Simulation succeeded      0 =      0 =    0 *    0
# Simulation succeeded 001e = 001e = 05 * 06
# Simulation succeeded     30 =     30 =    5 *    6
# Simulation succeeded ffdd = ffdd = 07 * fb
# Simulation succeeded    -35 =    -35 =    7 *   -5
# Simulation succeeded ffe2 = ffe2 = fb * 06
# Simulation succeeded    -30 =    -30 =   -5 *    6
# Simulation succeeded ffc8 = ffc8 = f9 * 08
# Simulation succeeded    -56 =    -56 =   -7 *    8
# Simulation succeeded 001e = 001e = fb * fa
# Simulation succeeded     30 =     30 =   -5 *   -6
# Simulation succeeded 0024 = 0024 = f7 * fc
# Simulation succeeded     36 =     36 =   -9 *   -4
# ** Note: $stop    : robertsonstest.sv(72)
#    Time: 4315 ns  Iteration: 0  Instance: /robertsonstest
# Break in Module robertsonstest at robertsonstest.sv line 72
# exit
# End time: 18:47:18 on Apr 24,2024, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
# *** Summary ********************************************
#     qrun: Errors:   0, Warnings:   0
#     vlog: Errors:   0, Warnings:   0
#     vopt: Errors:   0, Warnings:   0
#     vsim: Errors:   0, Warnings:   0
#   Totals: Errors:   0, Warnings:   0
Finding VCD file...
```

2. Be sure to upload all of your source code (.sv files), including any associated .txt files for $readmem statements.

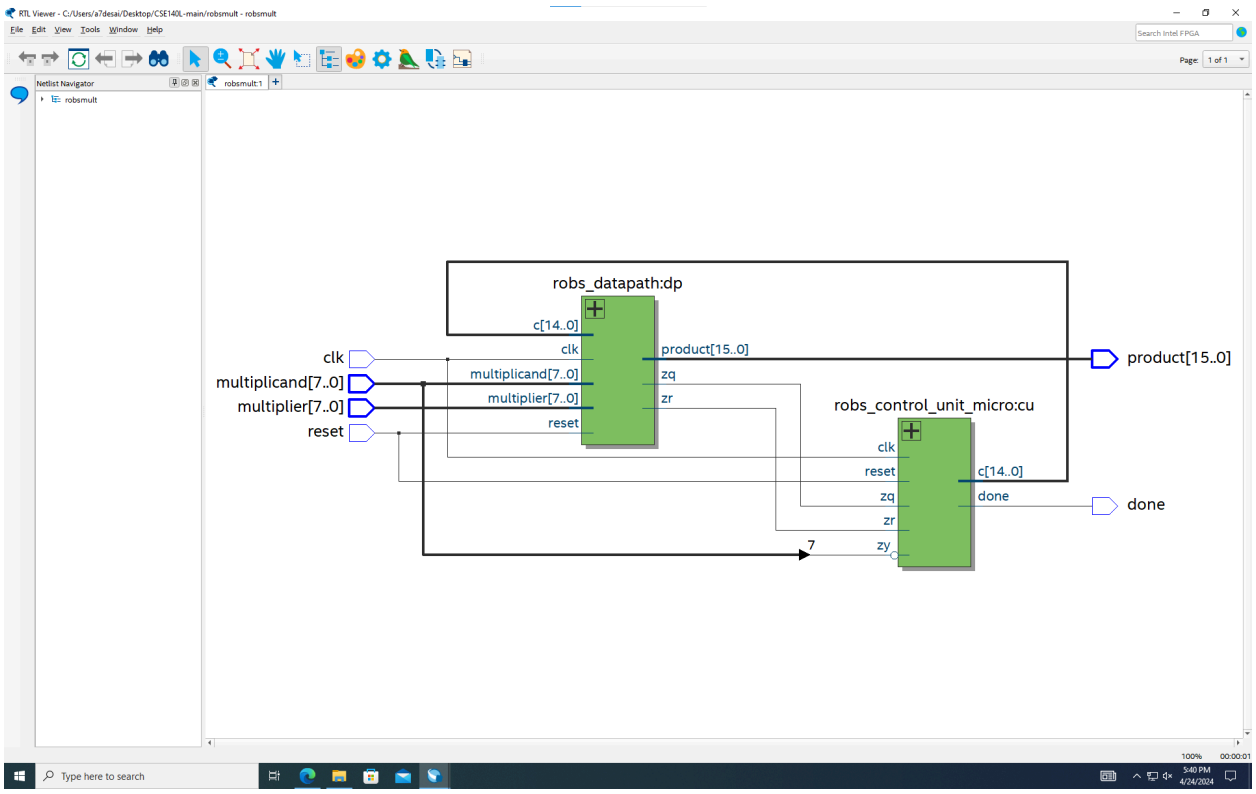
3. Waveforms.

Include screenshot of waveform for one entire multiplication cycle (i.e. the waveform should include the portion where reset is 1 until the portion where the done flag is 1)

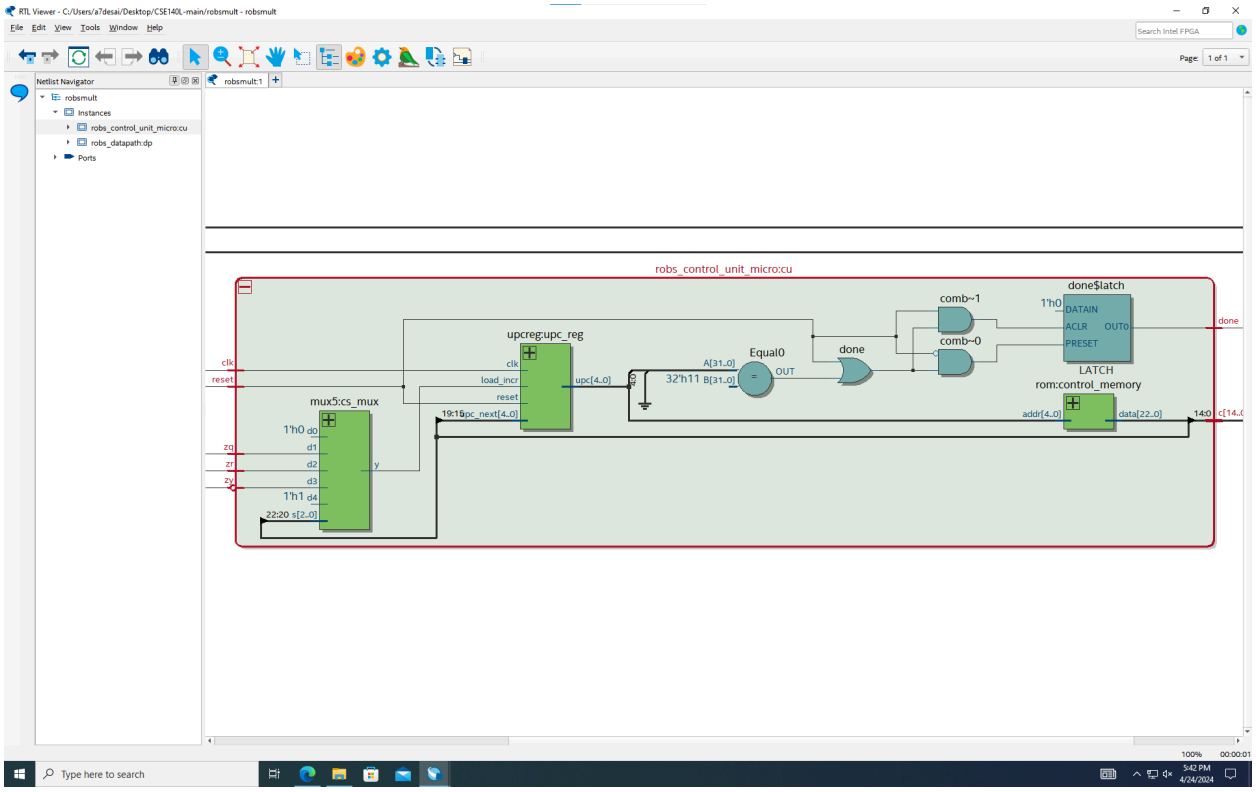



4. RTL diagrams of the following

a. Quartus RTL view of top level of the multiplier (it should show the connections between data path and control path).



b. Quartus RTL view of the control unit.



c. Quartus RTL view of the data path.