A 0.5V 36nW 10-transistor power-on-reset circuit with high accuracy

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***Abstract*—In this paper, a low voltage high accuracy 10-transistor power-on-reset circuit with brown-out-reset function is proposed. A native NMOS current reference based architecture is proposed to get high accuracy trip-voltage with a small area and power consumption. By adjusting the number of native NMOS transistors, a stable hysteresis window is obtained. Post-layout simulation results based on SMIC 55nm CMOS process show that the trip-voltage deviation of the proposed power-on-reset circuit is only 34mV under different temperature and process corners. Also, the trip-voltage of the proposed power-on-reset circuit shows great robustness to supply ramp time. The power consumption of the proposed circuit is as low as 36nW at 0.5V. Since the proposed power-on-reset circuit consists of only 10 transistors, the area is as low as 67.5μm².**

Keywords—power-on-reset, brown-out-reset, low-power, high accuracy, area efficient.

I. INTRODUCTION

In digital systems, a power-on-reset (POR) circuit with brown-out-reset (BOR) is necessary to set the memory elements to a certain state during the power supply ramp-up and ramp-down [1]. Fig.1 shows the functional diagram of a POR circuit. As shown in Fig.1, before the power supply voltage reaches the POR trip-voltage (VPOR), the reset signal (RSTN) remains low and the system is in a reset state. When the supply voltage exceeds the trip voltage, the reset signal is released. Once the power supply voltage drops below the BOR trip-voltage (VBOR), the reset signal is set to low to reset the system. VBOR is usually lower than VPOR. The difference between VPOR and VBOR is called hysteresis, which is used to avoid glitches in RSTN due to power supply ripples. Since the trip-voltage directly affects the stability of the systems, a high-accuracy POR circuit is preferred. Moreover, the POR circuit is always-on in the system, so the power consumption of the POR circuit needs to be as low as possible to meet the requirements of low power systems.

Several POR circuits have been displayed in previous works [1-9]. These POR circuits can be divided into voltage-reference-based POR circuits and delay-based POR circuits. The voltage-reference-based POR circuits [1-5] employ a bandgap and a voltage comparator to get high accuracy trip-voltage, which is robust to PVT variations. But this kind of POR circuits have large quiescent current, usually several μA. The large quiescent current greatly limits the applications in low-power systems. The delay-based POR circuits [6-9] employ a current source and a capacitor to generate the reset signal. This kind of POR circuits can get low leakage current. The main drawback of this kind of POR circuits is the low accuracy of the trip-voltage. The trip-voltage is very sensitive to PVT variations, and the trip-voltage deviation can be as large as several hundreds of mV under different corners. Also, the trip-voltage is sensitive to supply ramp time, which further limits the application of this kind of POR circuits. Moreover,

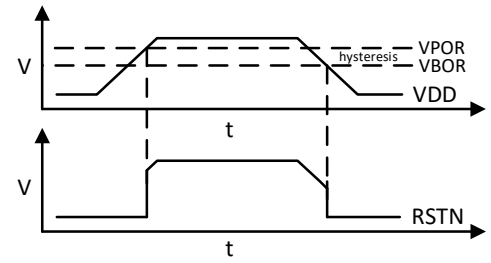

Fig. 1. Functional diagram of a POR circuit with BOR function.

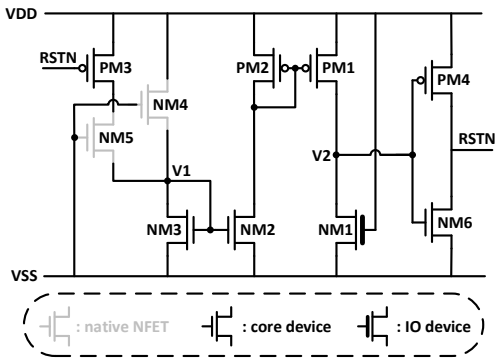

Fig. 2. Schematic of the proposed POR circuit.

the bipolar cells and resistors in the voltage-reference-based POR circuits and the capacitors (or transistors connect as capacitors) in the delay-based POR circuits greatly increase the area of these two kinds of POR circuits.

In this paper, a low voltage 10-transistor POR circuit is proposed. Different from previous voltage-reference-based POR circuits and delay-based POR circuits, the proposed POR circuit employs a native NMOS based current reference and a current comparator to generate accurate reset signal with a small area and power consumption. The trip-voltage of the proposed POR circuit is robust to PVT variations as well as supply ramp time, and the quiescent current is as low as 72.44nA. Since the proposed POR circuit consists of only 10 transistors, the area is as low as 67.5μm².

II. ARCHITECTURE OF THE PROPOSED POR CIRCUIT

In this Section, the architecture of the proposed POR circuit is analyzed in detail. As shown in Fig.2, the native NMOS transistors NM4 and NM5 work as a current reference generator. PM3 works as a digital switch to control the state of NM5. Two current mirrors composed of NM2, NM3, PM2 and PM1 are used to replicate the current of the native NMOS based current reference. The voltage of V2 is determined by the current of the current reference and the current of NM1. When the current of NM1 is larger than that of the current reference, V2 is discharged to low. On the contrary, when the current of NM1 is smaller than that of the current reference, V2 is charged to high.

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When the power supply starts to ramp up, the current of the current reference is much larger than that of NM1 since the threshold of native NMOS is much lower than that of IO NMOS. The voltage of V2 is charged to high and the output RSTN keeps low. With the increase of VDD, the current of NM1 increases gradually. When the current of NM1 increases to greater than the reference current, V2 is discharged to low and the output RSTN changes to high. When RSTN is high, the transistor NM5 is totally cut off by PM3 and the current of the current reference is only provided by NM4. When the power supply starts to ramp down, the current of NM1 decreases gradually. When the current drops to less than the current reference, V2 is charged to high and RSTN changes to low. Since the current of the current reference is larger when RSTN is low (PM3 is on), VPOR is larger than VBOR, and a hysteresis window is obtained.

Since NM4, NM5, NM3 and NM1 are in sub-threshold region, the drain current of these transistors can be calculated by the following formula [10]:

$$I_d = \mu C_{ox} \frac{W}{L}(m-1)V_T^2 \exp\left(\frac{V_{gs}-V_{th}}{mV_T}\right)\left(1-\exp\left(-\frac{V_{ds}}{V_T}\right)\right) \quad (1)$$

Where μ is mobility, C_{ox} is oxide capacitance, m is sub-threshold slope factor, and V_T is the thermal voltage (T=25°C, $V_T \approx$26mV). When we assume $V_{ds} >> V_T$, the factor $\left(1-\exp\left(-\frac{V_{ds}}{V_T}\right)\right)$ can be omitted and the formula can be simplified as follows:

$$I_d = \mu C_{ox} \frac{W}{L}(m-1)V_T^2 \exp\left(\frac{V_{gs}-V_{th}}{mV_T}\right) \quad (2)$$

When the supply voltage ramps to near the trip-voltage, the voltage of V2 is much larger than V_T, and the drain current of NM1 can be calculated as follows:

$$I_{NM1} = \mu_1 C_{ox1} \frac{W_1}{L_1}(m_1-1)V_T^2 \exp\left(\frac{VDD-V_{th1}}{m_1 V_T}\right) \quad (3)$$

Similarly, the current of the native NMOS based current reference can be expressed as follows:

$$I_{NN2} = N\mu_2 C_{ox2} \frac{W_2}{L_2}(m_2-1)V_T^2 \exp\left(\frac{-V_1-V_{th2}}{m_2 V_T}\right) \quad (4)$$

Where N is the count of native NMOS transistors that are weakly on. Since the sizes of NM4 and NM5 are the same in this design, N=1 when PM3 is off and N=2 when PM3 is on.

The current of NM3 can be expressed as follows:

$$I_{NM3} = \mu_3 C_{ox3} \frac{W_3}{L_3}(m_3-1)V_T^2 \exp\left(\frac{V_1-V_{th3}}{m_3 V_T}\right) \quad (5)$$

We assume that the current mirror is ideal, and when the current of NM1 is equal to that of the current reference, the supply voltage is the trip-voltage of the POR circuit, which means:

$$\mu_1 C_{ox1} \frac{W_1}{L_1}(m_1-1)V_T^2 \exp\left(\frac{V_{trip}-V_{th1}}{m_1 V_T}\right) = N\mu_2 C_{ox2} \frac{W_2}{L_2}(m_2-1)V_T^2 \exp\left(\frac{-V_1-V_{th2}}{m_2 V_T}\right) \quad (6)$$

By solving (6), the trip-voltage can be calculated as follows:

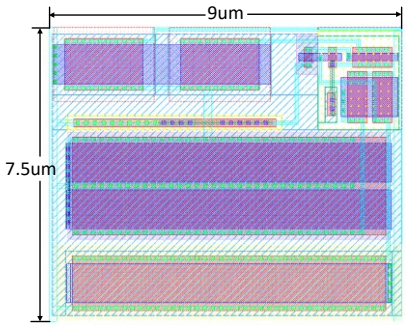

Fig. 3. Layout of the proposed POR circuit.

TABLE I. TRANSISTOR SIZES OF THE PROPOSED POR CIRCUIT

Name	W/L (μm)	Name	W/L (μm)
PM1	0.5/1	NM2	8/1
PM2	0.5/1	NM3	8/1
PM3	1/0.2	NM4	2/1
PM4	0.2/0.2	NM5	2/1
NM1	8/1	NM6	0.2/0.2

$$V_{trip} = \left(V_{th1} - \frac{m_1}{m_2}V_{th2}\right) + m_1 V_T ln\frac{N\mu_2 C_{ox2} W_2 L_1 (m_2-1)}{\mu_1 C_{ox1} W_1 L_2 (m_1-1)} - \frac{m_1}{m_2}V_1 \quad (7)$$

Similarly, the voltage of V_1 can be calculated as follows:

$$V_1 = \left(\frac{m_2 V_{th3} - m_3 V_{th2}}{m_3+m_2}\right) + \left(\frac{m_2 m_3}{m_3+m_2}V_T\right) ln\frac{N\mu_2 C_{ox2} W_2 L_3 (m_2-1)}{\mu_3 C_{ox3} W_3 L_2 (m_3-1)} \quad (8)$$

In (3)-(8), the parameters with subscript 1 are the parameters of NM1, the parameters with subscript 2 are the parameters of NM4 (NM5), and the parameters with subscript 3 are the parameters of NM3. To minimize the temperature coefficient (TC) of the trip-voltage, we should minimize TC of V_1 as well as TC of the first two terms in (7). As analyzed in [11-13], by adjusting the sizes of the native NMOS transistors and NM3, the temperature dependence of the two terms in (8) can cancel each other out and V_1 can be temperature insensitive. Similarly, the temperature dependence of the first two terms in (7) can cancel each other out by adjusting the sizes of the native NMOS transistors and NM1. Finally, a temperature-insensitive trip-voltage can be obtained.

The length of NM4, NM5, NM3 and NM1 is fixed at 1μm, and the width of NM4 and NM5 is fixed at 2μm. When PM3 is off, the best TC of V_1 is obtained when the width of NM3 is 8μm. When PM3 is on, the best width of NM3 is increased to 16μm. In this design, the width of NM3 is set to 8μm to balance the area and the accuracy. Similar analysis is applied to NM1. The width of NM1 is also optimized for the mode when PM3 is off. Interestingly, although the sizes of NM3 and NM1 are optimized for the mode when PM3 is off (VBOR), when PM3 is on, the temperature dependence of the first two terms in (7) and the third term in (7) can cancel each other out to some extent, and TC of the trip voltage when PM3 is on (VPOR) will not deteriorate too much compared with the optimal TC. The transistor sizes of the proposed POR circuit are shown in Table I.

Process variations can result in variations of transistor parameters. But the parameters in (7) and (8) are in pairs, and the parameter changes can cancel each other out, which makes

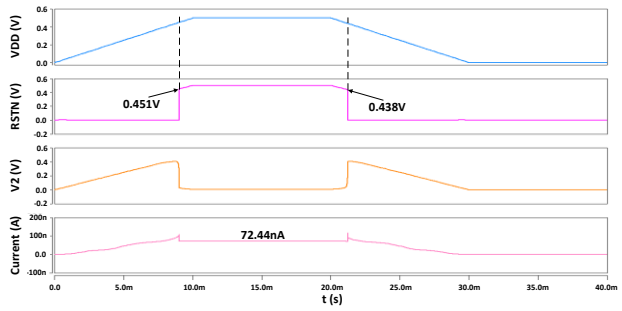

Fig. 4. Transient waveform of the proposed POR circuit (TT, 25 ° C, VDD=0.5V, ramp time=10ms).

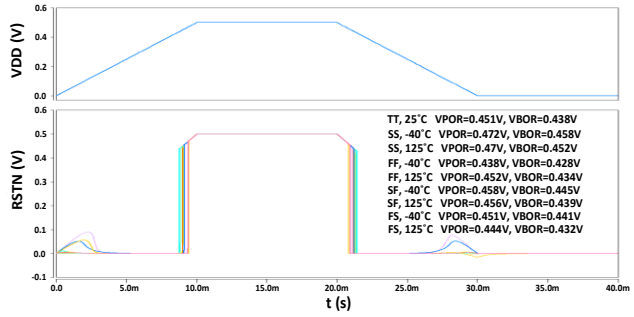

Fig. 5. Transient waveform of the proposed POR circuit at different corners (VDD=0.5V, ramp time=10ms).

TABLE II. TRIP-VOLTAGE AT DIFFERENT TRANSISTOR SIZES

Size (μm)	NM4=2 NM5=2	NM4=1 NM5=2	NM4=2 NM5=6	NM4=1 NM5=4
VPOR (V)	0.451	0.444	0.464	0.455
VBOR (V)	0.438	0.421	0.438	0.421
hysteresis window (mV)	13	23	26	34
VPOR deviation (mV)	34	34	40	35
VBOR deviation (mV)	30	32	30	32

the proposed POR circuit have strong robustness to process variations. For example, the threshold voltage of NM3 varies as large as $\pm 21.1\%$ at different corners, but when we consider $m_2V_{th3} - m_3V_{th2}$, the deviation decreases to $\pm 2.8\%$. In addition, the transistor sizes of NM1, NM3, NM4 and NM5 are relatively large, which further enhances the robustness to process variations.

III. SIMULATION RESULTS AND COMPARISONS

In order to evaluate the performance of the proposed POR circuit, the POR circuit has been implemented based on SMIC 55nm CMOS process. Hspice is adopted for all the following post layout simulations. Since the proposed POR circuit consists of only 10 transistors, the area of the proposed POR circuit is just 67.5μm^2 as shown in Fig.3.

Fig.4 shows the transient waveform of the proposed POR circuit. As shown in Fig.4, VPOR of the proposed POR circuit is 0.451V while VBOR is 0.438V. A hysteresis window of 13mV is obtained. The quiescent current of the proposed POR circuit is 72.44nA at 0.5V when RSTN is released.

In order to verify the effect of temperature and process variations on the trip-voltage, nine PVT corners are under consideration. As shown in Fig.5, at different corners, the trip-voltage deviation of VPOR is only 34mV, the trip-voltage deviation of VBOR is just 30mV, and the hysteresis window is at least 10mV.

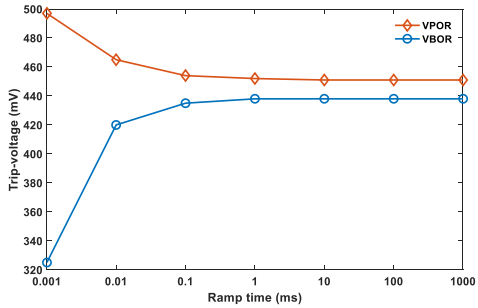

Fig. 6. Trip-voltage of the proposed POR circuit at different supply ramp time (TT, 25°C, VDD=0.5V).

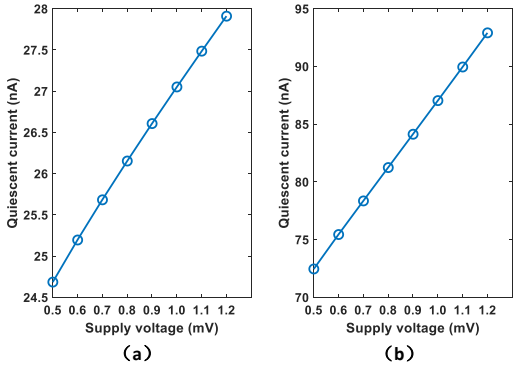

Fig. 7. Quiescent current at different supply voltage: (a) NM4; (b) the POR circuit. (TT, 25°C)

Since the trip-voltage is directly related to the sizes of NM4 and NM5, adjusting the sizes of NM4 and NM5 can adjust the trip-voltage. As shown in Table II, changing the size of NM4 can change both VPOR and VBOR, while changing the size of NM5 can change VPOR without affecting VBOR. Although adjusting the size of NM4 and NM5 will worsen the TC, a small change in TC will only increase the trip-voltage deviation by a small amount as shown in Table II, which is acceptable. If the trip-voltage is to be adjusted substantially, the most direct way is to change the gate voltage of NM1, for example, by giving the gate voltage through a voltage divider rather than directly connecting to the supply voltage.

Fig.6 shows the trip-voltage of the proposed POR circuit at different supply ramp time. As shown in Fig.6, the trip-voltage of the proposed POR circuit has strong robustness to supply ramp time when the ramp time is greater than 0.1ms.When the ramp time is very short, the observed trip voltage changes. This is because the charging and discharging of V2 takes time. When the ramp time is short, the supply voltage changes greatly during the charging and discharging time, and the observed trip voltage varies. As shown in Fig.6, when the ramp time is greater than 0.01ms, which is easily met in many low-voltage Internet-of-Things applications, the deviation of the trip voltage is acceptable.

It can be seen from (1) that when $V_{ds} >> V_T$, V_{ds} has little effect on the sub-threshold current. But the supply voltage can also affect other types of leakage current, so the quiescent current of NM4 increases slowly with the supply voltage as shown in Fig.7 (a). Even though the current mirror is not ideal which would increase the correlation between the quiescent current and the supply voltage, the quiescent current of the proposed POR circuit increases very slowly with the supply voltage as shown in Fig.7 (b). Therefore, the proposed POR can be applied to systems with wide supply range to provide accurate and low power operations.

TABLE III. PERFORMANCE SUMMARY AND COMPARISON OF VARIOUS POR CIRCUIT

	[1]	[2]	[3]	[4]	[5]	[7]	[8]	[9]	Proposed
Publication year	2016	2015	2016	2020	2020	2011	2014	2020	--
Technology	CMOS 65nm	CMOS 65nm	CMOS 14nm	CMOS 65nm	BiCMOS 0.25µm	CMOS 0.18µm	CMOS 0.5µm	CMOS 0.13µm	CMOS 55nm
Type	Bandgap based	Bandgap based	Bandgap based	Bandgap based	Bandgap based	Delay based	Delay based	Delay based	Current reference+ current comparator
Supply voltage (V)	0.55	1.0	1.1	1.0	1.8	1.8	1.8	3.3	0.5
Trip-voltage deviation (mV)	38	80	30	~ 23	234	NA	980	910	34
Stable hysteresis window	26mV	30mV	40mV	18mV~ 24mV	130mV	no	no	no	13mV
Brown out detection	yes	yes	yes	yes	yes	yes	yes	yes	yes
Quiescent current	4.6µA	5µA	451µA	2.25µA	0.4µA	1µA	1.5nA	1.1nA	72.44nA
TC (ppm/°C)	NA	NA	60 @ -10~110	NA	NA	NA	NA	NA	61.2 @ -40~125
Area (µm^2)	NA	NA	20000	14000	8250	12000	27000	4137	67.5
Results	Sim.	Sim.	Meas.	Meas.	Meas.	Meas.	Meas.	Sim.	Sim.

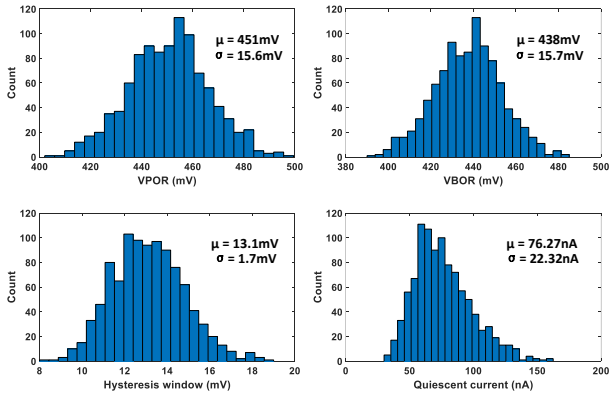

Fig. 8. Monte-Carlo simulation results of the proposed POR circuit (25°C, ramp time=10ms).

Fig.8 shows 1000 points Monte-Carlo simulation results of the proposed POR circuit considering both global variation and local mismatch. As shown in Fig.8, the mean VPOR is 451mV with a standard deviation of 15.6mV. The mean VBOR is 438mV with a standard deviation of 15.7mV. A stable hysteresis window is obtained with a mean value of 13.1mV and a standard deviation of 1.7mV.

Table III shows a comparison of the proposed POR circuit with other POR circuits. As shown in Table III, due to insensitivity to temperature and process variation, the trip-voltage deviation of the proposed POR circuit is only 34mV, which is similar to that of bandgap-based POR circuits and much smaller than that of delay-based POR circuits. Also, a stable hysteresis window is obtained in the proposed POR circuit to prevent glitches due to power supply ripples. The quiescent current of the proposed POR circuits is only 72.44nA, much smaller than that of the bandgap-based POR circuits. Moreover, the proposed POR circuit consists of only 10 transistors and does not need any bipolar cell, resistor or capacitor, so the area is as small as 67.5µm^2, which shows great area efficiency compared with other POR circuits.

IV. CONCLUSION

In this paper, a low voltage high accuracy POR circuit is proposed. Based on a current reference and a current comparator architecture, the proposed POR circuit has low trip-voltage deviation, stable hysteresis window and low quiescent current with only 10 transistors. At the supply voltage of 0.5V, the power consumption of the proposed POR circuit is only 32nW with a trip-voltage deviation of as low as 34mV. With a bipolar cell-less, resistor-less and capacitor-less architecture, the area of the proposed POR circuit is only 67.5µm^2. Moreover, the trip-voltage is tolerant to the supply voltage as well as the supply ramp time. Thus, the proposed POR circuit is well suited to low power systems with wide supply range to provide energy efficient and high accuracy operations.

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