An Accurate Low-Power Power-on-Reset Circuit in 55-nm CMOS Technology

Heng You, *Member, IEEE*, Jia Yuan, Zenghui Yu, and Shushan Qiao, *Member, IEEE*

***Abstract*—In this brief, an accurate low-power power-on-reset circuit is proposed. In order to get an accurate trip-voltage with little overhead, a low-power architecture based on current reference and current comparator is proposed. The reference current in the proposed power-on-reset circuit is mainly provided by the sub-threshold current of several native NMOS transistors, and a stable hysteresis window can be obtained by adjusting the number of enabled native NMOS transistors. Measurement results based on 55nm CMOS process show that the proposed power-on-reset circuit consumes only 32nW at the supply voltage of 0.5V. The measured power-on-reset trip-voltage is 0.45V with a temperature coefficient of 227μV/°C. Since the proposed power-on reset circuit consists of only 10 transistors, the area of the proposed power-on-reset circuit is as low as 67.5μm^2.**

***Index Terms*—Power-on-reset, low-voltage, low-power, high accuracy, area efficient.**

I. Introduction

With the rapid development of Internet of Things (IoT) applications, reducing energy consumption has become an important task in integrated circuit design [1]. As one of the most effective methods to reduce power consumption, low-voltage technique is widely used in low-power systems [2]–[3]. In digital systems, it is necessary to preset the memory elements to a certain state during the power supply ramping up [4]. Therefore, to ensure that the system can work correctly at low supply voltage, an accurate low-voltage power-on-reset (POR) circuit is required. In addition, the POR circuit is always-on after the reset signal is released, so the static power of the POR circuit should be as low as possible to meet the requirements of the system for low power consumption.

During system operation, the power supply voltage may drop significantly in a short time due to supply noise or load changes, which is called a brown-out event. In order to avoid the impact of the short-time supply voltage drop, the POR circuit needs to have a brown-out detection (BOD) function, which can reset the system when the power supply voltage is lower than the BOD trip-voltage. To avoid frequent system resets caused by supply ripples, the BOD trip-voltage is usually slightly lower than the POR trip-voltage. The difference between the POR trip-voltage and the BOD trip-voltage is called hysteresis.

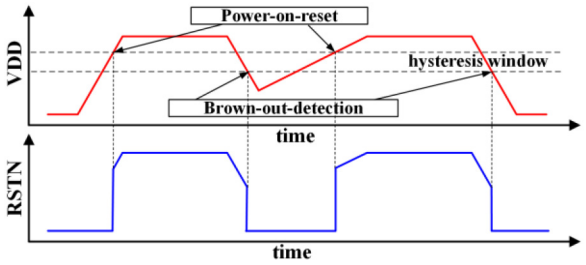

Fig. 1. Function of a power-on-reset circuit with brown-out-detection.

Many reported POR circuits adopt band-gap reference to get an accurate POR trip-voltage [4]–[8]. Although band-gap reference has great robustness to PVT variations, the power consumption of the band-gap reference is usually large, resulting in high power consumption of band-gap based POR circuits, which is not suitable for ultra-low-power systems. The POR circuit in [9] adopts part of the circuit presented in [10] to generate the reference voltage, which greatly reduces the power consumption compared with band-gap reference. However, this results in a significant decrease in the robustness of the POR circuit to PVT variations. Many low-power POR circuits adopt delay elements to generate the POR signal, which can significantly reduce the power consumption of the POR circuit compared with the band-gap based POR circuits [11]–[13]. However, the delay element is very sensitive to PVT variations, resulting in poor robustness of the trip-voltage. Moreover, most of the above POR circuits cannot operate correctly at low supply voltage, which greatly limits their application in low-voltage systems.

In this brief, an accurate low-power power-on-reset circuit is proposed. With the employment of a low-power architecture based on current reference and current comparator, the proposed POR circuit can provide accurate power-on-reset operation with little power overhead. This brief is an extension of [14]. Additionally, experimental results are presented in this brief to further verify the validity of the proposed POR circuit. This brief also presents a variant of the proposed POR circuit to generate POR circuits with different trip-voltages, which can further expand the application of the proposed circuit.

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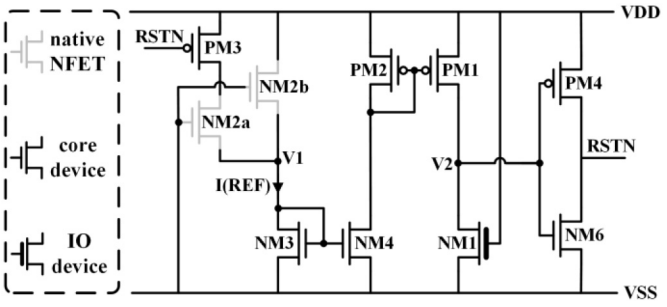

Fig. 2. Schematic of the proposed 10-transistor POR circuit [14].

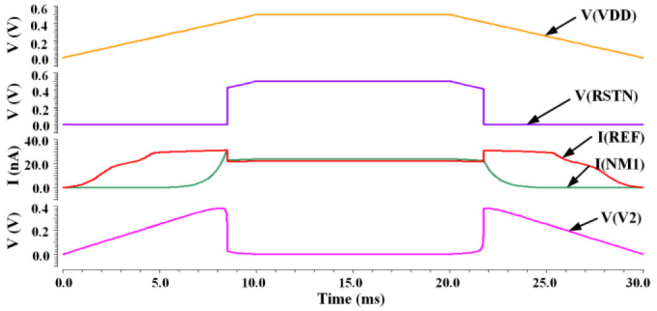

Fig. 3. Transient waveform of the proposed 10-transistor POR circuit.

The remainder of this brief is organized as follows. Section II presents the architecture of the proposed POR circuit as well as the variant of the circuit. Section III shows the experimental results of the proposed circuit and the comparison with other POR circuits. Finally, Section IV draws a conclusion.

II. Architecture of the Proposed POR Circuit

In this section, the architecture of the proposed 10-transistor POR circuit and its variant are analyzed in detail.

A. Architecture of the 10-Transistor POR Circuit

The schematic of the proposed POR circuit is shown in Fig. 2. As shown in Fig. 2, the reference current of the 10-transistor POR circuit is provided by the sub-threshold current of the transistors NM2a and NM2b. Transistors NM3, NM4, PM2 and PM1 act as current mirrors to replicate the reference current. Since the gate of transistor NM1 is directly connected to VDD, the current of NM1 represents the voltage of the power supply. The voltage of node V2 is determined by the current of the current reference and the current of NM1. When the reference current is larger than the current of NM1, node V2 charges to high through PM1. When the current of the current reference is smaller than the current of NM1, node V2 discharges to low through NM1. Transistors PM4 and NM6 act as an inverter and output the reset signal RSTN.

The detailed operation of the 10-transistor POR circuit is shown in Fig. 3. As shown in Fig. 3, the 10-transistor POR circuit works as follows. When the power supply starts to ramp up, the current of the current reference and transistor NM1 rises gradually. Since NM2a, NM2b, NM3 and NM1 are in sub- threshold region, the current of these transistors can be calculated as follows [15]:

$$I_d = \mu C_{ox}\frac{W}{L}(m-1)V_T^2 \exp\left(\frac{V_{gs}-V_{th}}{mV_T}\right)\left(1-\exp\left(-\frac{V_{ds}}{V_T}\right)\right) \quad (1)$$

It can be seen from (1) that when the supply voltage is relatively low, the current of the current reference increases with the increase of the supply voltage, and when the supply voltage rises to a higher value ($V_{ds} >> V_T$), the current of the current reference remains stable. It can also be seen from (1) that the current of NM1 increases exponentially as the supply voltage increases. Since the threshold of transistors NM2a and NM2b is much lower than that of transistor NM1, the reference current is larger than the current of NM1 when the supply voltage is relatively low, and node V2 charges to high. As the supply voltage increases, the current of NM1 increases rapidly until it is greater than the reference current, and node V2 discharges to low, the reset signal RSTN changes to high. When the reset signal RSTN is high, the current of NM2a is totally cut off by transistor PM3, and the reference current decreases. After the reset signal RSTN is released, the current of NM1 is slightly larger than the reference current to ensure that the node V2 remains low and RSTN remains high. When the power supply starts to ramp down, the current of NM1 decreases gradually. When the current of NM1 drops below the reference current, node V2 charges to high and the reset signal RSTN changes to low. Since the reference current is larger when RSTN is low (PM3 is on), the POR trip-voltage (VPOR) is larger than the BOD trip-voltage (VBOD), and a hysteresis window is obtained.

In order to further analyze the trip-voltage of the proposed 10-transistor POR circuit, the trip-voltage of the POR circuit can be expressed as follows [14]:

$$V_{trip} = \left(V_{th1} - \frac{m1}{m2}V_{th2}\right) + m_1 V_T ln\frac{N\mu_2 C_{ox2} W_2 L_1 (m_2-1)}{\mu_1 C_{ox1} W_1 L_2 (m_1-1)} - \frac{m_1}{m_2}V_1 \quad (2)$$

where V1 can be expressed as follows:

$$V_1 = \left(\frac{m_2 V_{th3} - m_3 V_{th2}}{m_3+m_2}\right) + \left(\frac{m_2 m_3}{m_3+m_2}V_T\right) ln\frac{N\mu_2 C_{ox2} W_2 L_3 (m_2-1)}{\mu_3 C_{ox3} W_3 L_2 (m_3-1)} \quad (3)$$

In (2)-(3), the parameters with subscript 1 are the parameters of NM1, the parameters with subscript 2 are the parameters of NM2a (NM2b), and the parameters with subscript 3 are the parameters of NM3. Parameter N represents the number of enabled native NMOS transistors. When the reset signal RSTN is low, parameter N is equal to 2, and the trip-voltage is the POR trip-voltage. When RSTN is high, the current of NM2a is totally cut off by PM3, parameter N is equal to 1, and the trip-voltage is the BOD trip-voltage.

Since V_{th} is complementary to temperature [15] and V_T is proportional to temperature, the temperature coefficients of the first two terms in (2) can be set to cancel out by adjusting the size of the transistors. Similarly, the temperature coefficients of the two terms in (3) can also cancel each other out. To minimize temperature sensitivity, the optimal sizes of transistors NM1, NM2a (NM2b) and NM3 can be calculated by solving the equations $dV_{trip}/dT = 0$ and $dV_1/dT = 0$. To simplify the analysis, we consider the first-order temperature dependence of V_{th} and V_T, and ignore the temperature dependence of μ and m as well as the second-order temperature dependence of

TABLE I
THRESHOLD VOLTAGE VARIATION OF THREE TYPES OF TRANSISTORS

MOSFET Type	Native NFET	Core Device	IO Device
standard deviation (mV)	10.9	12	17.1
6σ (mV) *	65.4	72	102.6

* : Threshold voltage deviation between fast corner and slow corner

TABLE II
TRIP-VOLTAGE OF THE PROPOSED 10-TRANSISTOR POR CIRCUIT

Corner	TT 25°C	SS -40°C	SS 125°C	FF -40°C	FF 125°C
VPOR (V)	0.451	0.472	0.47	0.438	0.452
VBOD (V)	0.438	0.458	0.452	0.428	0.434

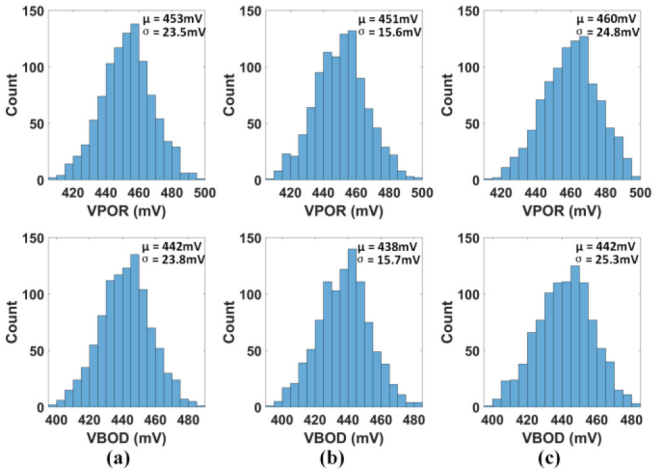

Fig. 4. Monte-Carlo simulation results of the 10-transistor POR circuit: (a) −40°C; (b) 25°C; (c) 125°C.

V_{th} [16]. Then the optimum width ratio can be expressed as follows:

$$(\frac{W_2}{W_1})_{opt} = \frac{(m_1-1)\mu_1 C_{ox1} L_2}{(m_2-1)N\mu_2 C_{ox2} L_1} \cdot \exp(\frac{q}{k} \cdot \frac{m_1 C_{Vth2} - m_2 C_{Vth1}}{m_1 m_2}) \quad (4)$$

$$(\frac{W_2}{W_3})_{opt} = \frac{(m_3-1)\mu_3 C_{ox3} L_2}{(m_2-1)N\mu_2 C_{ox2} L_3} \cdot \exp(\frac{q}{k} \cdot \frac{m_3 C_{Vth2} - m_2 C_{Vth3}}{m_2 m_3}) \quad (5)$$

where C_{Vth} is the first-order temperature coefficient of the threshold voltage and k is Boltzmann's constant.

It can be seen from (2) and (3) that the trip-voltage of the POR circuit is related to the threshold voltage V_{th}, so the V_{th} variation will affect the trip-voltage V_{trip}. For example, an increase in V_{th1} leads to an increase in V_{trip}, an increase in V_{th2} leads to a decrease in V_{trip}, and an increase in V_{th3} leads to a decrease in V_{trip}. The threshold voltages of the three types of transistors are significantly affected by the process variations as shown in Table I, but the factors affecting the trip-voltage all appear in pairs, so they can cancel each other out, thereby significantly improving the robustness of the proposed POR circuit to process variations. Table II shows the trip-voltage of the proposed POR circuit at different corners. As shown in Table II, the trip-voltage deviation of VPOR is only 34mV, and the trip-voltage deviation of VBOD is only 30mV. To further verify the robustness of the proposed POR circuit to process variations, Fig. 4 shows 1000 points Monte-Carlo simulation results of the proposed POR circuit at different temperatures considering both global variation and local mismatch. At the temperature of 25°C, the mean VPOR is 451mV with a standard deviation of 15.6mV, and the mean VBOD is 438mV with a standard deviation of 15.7mV.

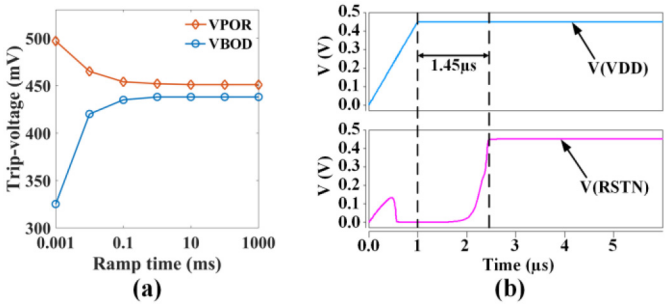

Fig. 5. (a) Observed trip-voltage of the 10-transistor POR circuit at different ramp time; (b) Transient waveform of the POR circuit when the supply voltage is 0.451V and the ramp time is 1μs.

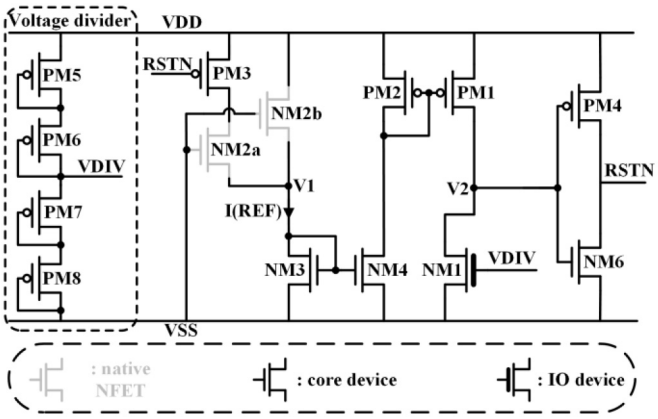

Fig. 6. Schematic of the proposed 14-transistor POR circuit.

In order to verify the effect of supply ramp time on the trip-voltage, Fig. 5 (a) shows the observed trip-voltage of the 10-transistor POR circuit at different ramp time. As shown in Fig. 5 (a), the trip-voltage of the 10-transistor POR circuit has strong robustness to supply ramp time. When the ramp time is very short, the observed VPOR increases and the observed VBOD decreases. This is because the charging and discharging of node V2 takes time, and there will be a certain delay in the reset signal, which is similar to other band-gap based POR circuits [7], [8]. As shown in Fig. 5 (b), the proposed POR circuit can work correctly at a supply voltage of 451mV and a ramp time of 1μs, indicating that the actual trip-voltage of the POR circuit is still 451mV. The delay time of the reset signal is 1.45μs, which is smaller than that in [7], [8].

B. Architecture of the Variant of the Proposed POR Circuit

Systems with different power supply voltages have different requirements for the trip-voltage of the POR circuit. The 10-transistor POR circuit proposed above works well in low-voltage systems, but is relatively unsuitable for higher voltage systems. In order to make the proposed architecture more applicable to systems with different power supply voltages, a variant consisting of 14 transistors is proposed, which can generate higher trip-voltage as required.

The schematic of the proposed 14-transistor POR circuit is shown in Fig. 6. As shown in Fig. 6, a voltage divider is added

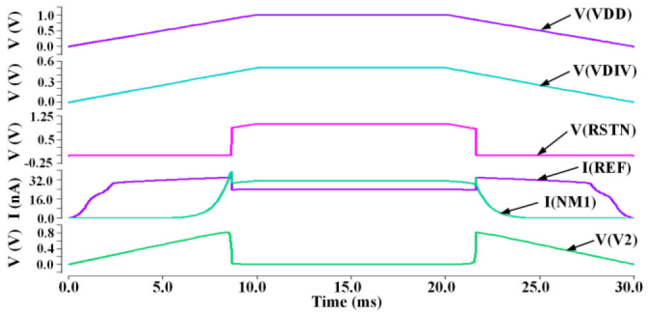

Fig. 7. Transient waveform of the 14-transistor POR circuit.

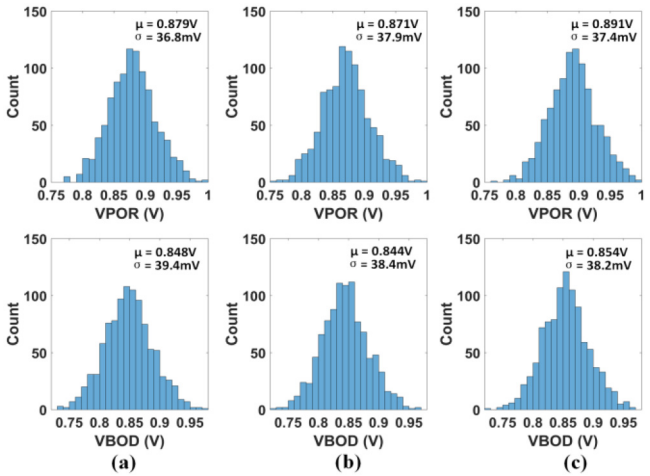

Fig. 8. Monte-Carlo simulation results of the 14-transistor POR circuit: (a) −40°C; (b) 25°C; (c) 125°C.

to divide the supply voltage. A stacked-diode based voltage divider is employed rather than the traditional resistor based voltage divider to reduce the area and power overhead. The gate of the transistor NM1 is adjusted to be controlled by the output of the voltage divider, thereby scaling down the gate voltage of the transistor NM1.

The detailed operation of the 14-transistor POR circuit is shown in Fig. 7. As shown in Fig. 7, the operation of the 14-transistor POR circuit is similar to that of the 10-transistor POR circuit. The only difference is that since the gate of NM1 in the 14-transistor POR circuit is connected to the output of the voltage divider rather than the power supply, the reset signal RSTN will be released only when VDIV is sufficient to discharge node V2 to low, so the 14-transistor POR circuit can get a higher trip-voltage. Assuming that the trip-voltage of the 10-transistor POR circuit is V_{trip0} and the voltage division coefficient of the voltage divider is k ($VDIV = k * VDD$), the trip-voltage of the 14-transistor POR circuit can be expressed as $V_{trip} = 1/k * V_{trip0}$. So the trip-voltage of the 14-transistor POR circuit is to amplify the trip-voltage of the 10-transistor POR circuit by $1/k$ times. By adjusting the voltage division coefficient of the voltage divider, POR circuits with different trip-voltages can be obtained.

Table III shows the trip-voltage of the 14-transistor POR circuit at different corners, where the voltage division coefficient k is approximately 0.5. As shown in Table III, the trip-voltage of the 14-transistor POR circuit is increased to approximately

TABLE III
TRIP-VOLTAGE OF THE PROPOSED 14-TRANSISTOR POR CIRCUIT

Corner	TT 25°C	SS -40°C	SS 125°C	FF -40°C	FF 125°C
VPOR (V)	0.87	0.912	0.908	0.843	0.875
VBOD (V)	0.845	0.886	0.872	0.824	0.838

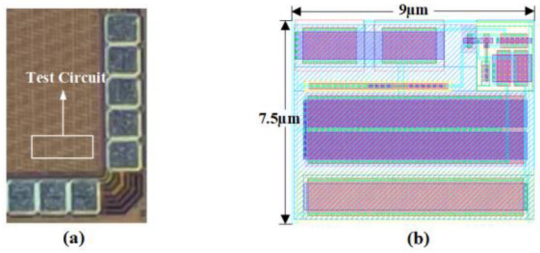

Fig. 9. (a) Die photo of the test chip; (b) Layout of the 10-transistor POR circuit.

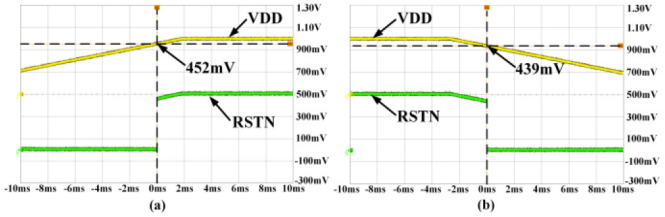

Fig. 10. Measured waveform of the proposed 10-transistor POR circuit: (a) POR function; (b) BOD function.

twice the trip-voltage of the 10-transistor POR circuit. The trip-voltage deviation of VPOR is 69mV, the trip-voltage deviation of VBOD is 62mV, which is slightly larger than that of the 10-transistor POR circuit. This is because the deviation is also amplified while the trip-voltage of the POR circuit is amplified, but the deviation is still small, and the proposed 14-transistor POR circuit can still provide an accurate POR function.

In order to verify the robustness of the 14-transistor POR circuit to process variations, Fig. 8 shows 1000 points Monte-Carlo simulation results of the 14-transistor POR circuit considering both global variation and local mismatch. At the temperature of 25°C, the mean VPOR of the 14-transistor POR circuit is 0.871V with a standard deviation of 37.9mV, the mean VBOD of the 14-transistor POR circuit is 0.844V with a standard deviation of 38.4mV.

III. EXPERIMENTAL RESULTS AND COMPARISONS

In order to further verify the effectiveness of the proposed architecture, the 10-transistor POR circuit was fabricated in SMIC 55nm CMOS technology. Fig. 9 shows the die photo of the test chip as well as the layout of the 10-transistor POR circuit. Since the POR circuit consists of only 10 transistors, the area of the POR circuit is just 67.5μm^2.

Fig. 10 shows the measured waveform for POR and BOD operations of the proposed 10-transistor POR circuit. As shown in Fig. 10, the measured VPOR is 452mV at the ramp time of 10ms, where the temperature is room temperature and the supply voltage is 500mV. The measured VBOD under the same conditions is 439mV. Fig. 11 shows the measured

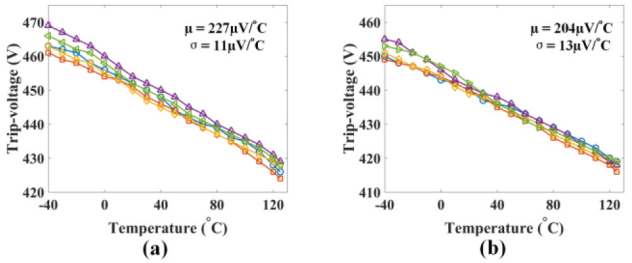

Fig. 11. Measured trip-voltage of the proposed 10-transistor POR circuit at different temperatures: (a) VPOR; (b) VBOD.

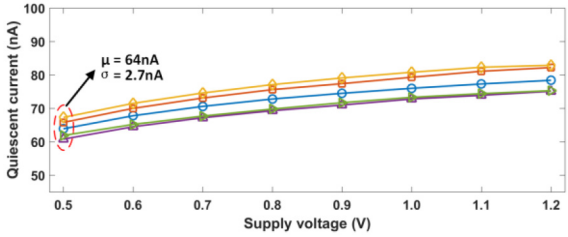

Fig. 12. Measured quiescent current of the proposed 10-transistor POR circuit at different supply voltages.

TABLE IV
PERFORMANCE COMPARISON OF VARIOUS POR CIRCUITS

	[5]	[8]	[9]	[12]	Proposed
Technology	70nm	65nm	0.13μm	0.13μm	55nm
Type	Band-gap based	Band-gap based	Reference based	Delay based	Current based
Native NFET	No	No	No	No	Yes
Voltage (V)	3.0	0.65	1.2	3.3	0.5V
VPOR (V)	2.0	0.59	0.95	1.37	0.45
TC (μV/°C)	292@ 25~90	292@ -10~110	4000@ 0~50	NA	227 @ -40~125
Static power	3.6μW	2.6μW	3.6nW	3.3nW	32nW
Area (μm²)	64000	95000	NA	4137	67.5
Results	Meas.	Meas.	Meas.	Sim.	Meas.

trip-voltage of the proposed 10-transistor POR circuit across 5 chips at different temperatures. As shown in Fig. 11, for the −40°C to 125°C temperature range, the measured temperature coefficient of VPOR is 227μV/°C with a standard deviation of 11μV/°C, and the measured temperature coefficient of VBOD is 204μV/°C with a standard deviation of 13μV/°C.

Fig. 12 shows the measured quiescent current of the proposed 10-transistor POR circuit across 5 chips at different supply voltages. As shown in Fig. 12, the quiescent current of the proposed 10-transistor POR circuit increases very slowly with the supply voltage. When the supply voltage is 0.5V, the average quiescent current of the POR circuit is just 64nA.

Table IV shows a comparison of the proposed POR circuit with other POR circuits. As shown in Table IV, the trip-voltage of the proposed POR circuit is 0.45V, which is suitable for low-voltage operations. The proposed POR circuit can work correctly in a wide temperature range from −40°C to 125°C with a temperature coefficient of only 227μV/°C, which is comparable to that of the band-gap based POR circuits. The static power of the proposed POR circuit is only 32nW, much smaller than that of the band-gap based POR circuits. Moreover, since the proposed POR circuit consists of only 10 transistors, the area is as small as 67.5μm², which shows great area efficiency compared with other POR circuits.

IV. CONCLUSION

In this brief, an accurate low-power POR circuit is proposed. With the employment of a low-power architecture based on current reference and current comparator, the proposed POR circuit is robust to PVT variations. The trip-voltage of the proposed 10-transistor POR circuit is 0.45V, which is suitable for low-voltage systems. In order to meet the requirements of higher trip-voltage, a variant based on the POR circuit is also proposed, which has a higher trip-voltage. The static power of the 10-transistor POR circuit is only 32nW, which is much lower than band-gap based POR circuits. Since the proposed POR circuit consists of only 10 transistors, the area is just 67.5μm². Overall, the proposed POR circuit has accurate trip-voltage, low static power, and small area, which is very suitable for low-voltage and low-power systems.

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