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TITLE - Traffic light controller

Objective - > the objective is to develop a traffic signal controller, which can be sensitive to changing traffic management policy. And to achieve a wide range of transport and environmental objectives. Main objective is minimize the vehicle delays and stops.

Language -> Verilog.

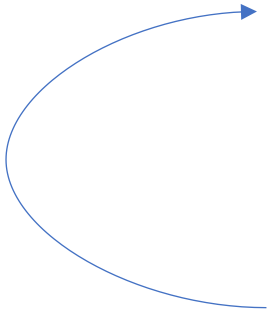
Functionality - > There will be 3 inputs 1. Clock, 2.clear, 3.X

X=1 → if there is a car on the crossing road.

X=0 → if there is no car on the crossing road.

The Highway signal remain green by default.

The traffic signal for the crossing road must turn green only long enough to let the cross on the crossing road go.



State	Signal change
S0	Highway -> Green, Crossing road -> Red
S1	Highway -> Yellow, Crossing road -> Red
S2	Highway -> Red, Crossing road -> Red
S3	Highway -> Red, Crossing road -> Green
S4	Highway -> Red, Crossing road -> Yellow