

International Institute of Information Technology, Hyderabad
 (Deemed to be University)

EC2.101 – Digital Systems and Microcontrollers

Mid Semester Examination

Max. Time: 1.5 Hr

Max. Marks: 40

CALCULATORS ARE NOT ALLOWED

Numbers in square brackets [x] after a statement show the marks for that question.

Numbers in {} brackets are for administrative use. Please ignore.

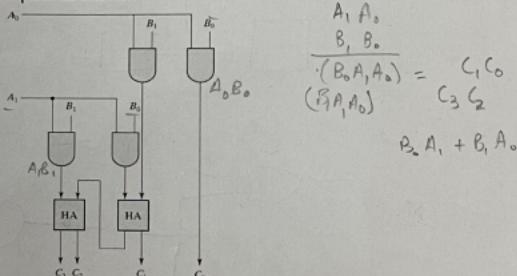
Q1. Imagine there is a terrible crime, and the police catch hold of four suspects: Abdul, Bishnoi, Carren and David. The police questions them and after a lot of investigation, finds out that they are deceiving the police in a set pattern:

- Abdul is lying only when either Bishnoi is telling the truth, or Carren is lying. $A=0 \text{ if } B=0 \text{ or } C=1 \text{ (B+C)}$
- Bishnoi is lying only when either Abdul is lying, or David is telling the truth. $B=0 \text{ if } (A+B)$
- Carren is lying only when Abdul is lying. $C=0 \text{ if } A$
- David is telling the truth only when either Abdul and Bishnoi are both lying, or Carren is lying. $D=1 \text{ if } AB+C$

Find out the condition when *all the above* statements are simultaneously true. Who is telling the truth? (Hint: the “or” in the above statements is inclusive).

[10 marks]{CO-1}

Q2. Say we create a 2-bit binary multiplier as shown:



However, when we test the circuit, we find that the output is correct only for the four cases when $A=10$ or 11 and $B=01$ or 11 . We investigate and find out that because of a problem with the breadboard, one of the internal wires is permanently getting connected to either ground or VDD, i.e., it is either stuck at ground or VDD level. Can you find out which wire is problematic and what value it is getting stuck at?

[10 marks]{CO-2}

Q3. In the n-bit binary adder, there is a choice between the speed and power/area of the circuit. We can make a fast circuit with the carry lookahead logic, or we can make a slow circuit with cascaded full adders. Let us quantify the circuit complexity increase in going from the simple full adder-based circuit to the carry lookahead circuit. Calculate the number of transistors in each implementation for an n-bit binary adder. (Consider a two level AND-OR implementation for carry look ahead circuit, 2-input ExOR is 16 transistors and 3-input ExOR is obtained using two two-input ExOR).

[10 marks]{CO-1}

Q4. A 4-digit decimal number of the form $(aabb)$ is a perfect square. What is the value of the digits a and b ? Provide detailed mathematical reasoning.

[10 marks]{CO-2}