# INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI

## Department of EEE

## EE 304 Design Project Report


Group No: 12

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TITLE:

OTP authenticated Cycle Lock System Based on LoRa Transceiver

# ABSTRACT

OTP authenticated Cycle Lock System can be augmented to public cycle systems, where instantaneous access of shared cycle is required for a user. Lora , patented by SEMTECH , is a new Long range low power long range spread spectrum modulation scheme for low bit rates. Currently in a public cycle system the smart cycle locks are based on RFID, GSM communication which either prove to be expensive or redundant. LoRa based communication for smart lock provides a long range, low power, bit rates which apparently are optimal necessities for a campus public cycles systems.

# WORK DONE

*Literature related to the following have been studied:

*LoRa modulation

*Datasheet SX1272 IC

*Programming 8bit ATMEL ATMEGA 328p microcontroller

* Networks Stack, Protocols

* serial communication between MCU and PC

*Programmed ATMEL ATMEGA 328P unit using the Embedded C as client Node (Lock)

*Constructed a Keypad using generic circuit, assembled other peripherals viz. SX1272 IC, Servo motor etc. to the MCU unit of the node as mentioned in the circuit diagram.

*Made a simple mobile interface for the user to query an OTP

* Constructed a server by interfacing the Arduino with SX1272 and PC along with executing programs developed for the server to act as a gateway between Lora network and the Internet

*Used googles firebase server to store data of the user and connected internet to the Lora network by using Node.js

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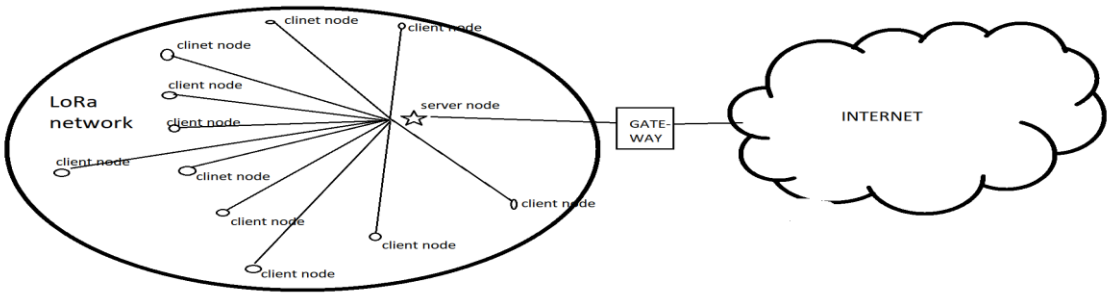
# 1. Literature Review

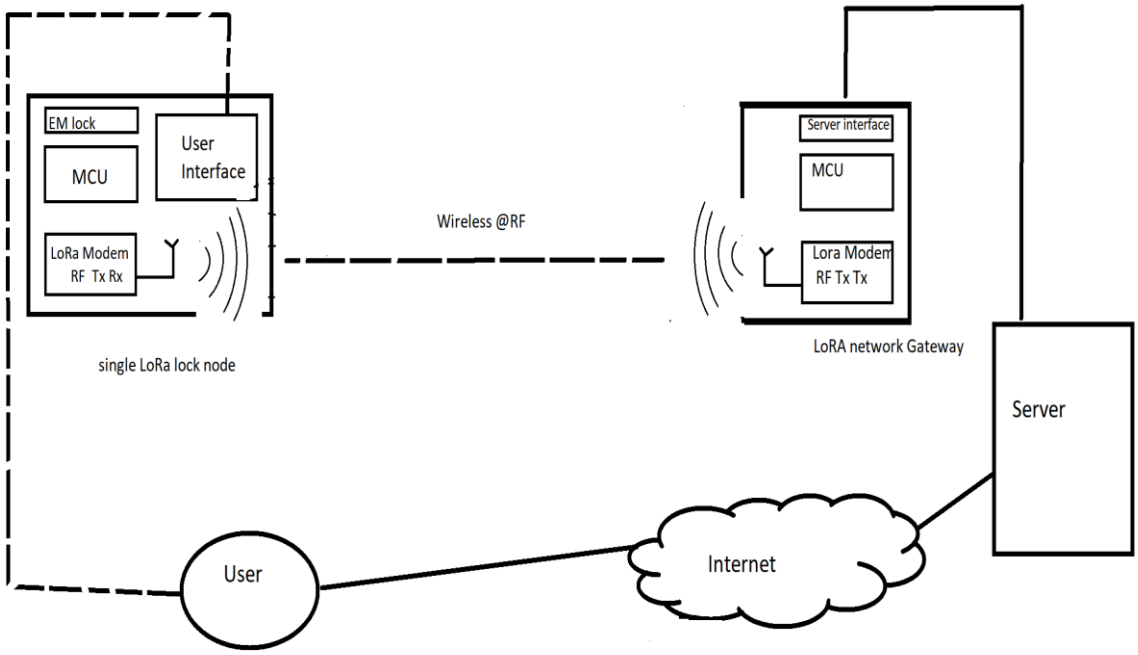
LoRa SX1272 IC data sheet by SEMTECH is quite detailed enough to understand its architecture, configurations, SPI interface and other electronic information to operate the IC. AVR tutorials and other blogs along with the data sheet have been handy for programming the ATMEL ATEMGE 328 p microcontroller. Literature on Chirp modulation and LoRa modulation have given us an insight into the LoRa modulation scheme which is a proprietary modulation scheme patented by SEMTECH. Nodejs and pyserial tutorials have enabled us to write scripts so as to establish a gateway between LoRa network and the internet using a PC and Arduino.

# 2.System Design

Multiple LoRa Locks acts as client nodes which communicate independently to a single server node connected to the internet gateway (acts as an interface between LoRa based network and internet). This can be perceived as Internet of things over LoRa.




A user who needs a cycle is required to enter address of the cycle and requests for an OTP via an mobile app. A server sends the OTP to both cycle's smart lock, over LoRa communication and to the user over internet. The user can then enter password via keypad provided in the system and can unlock the lock.



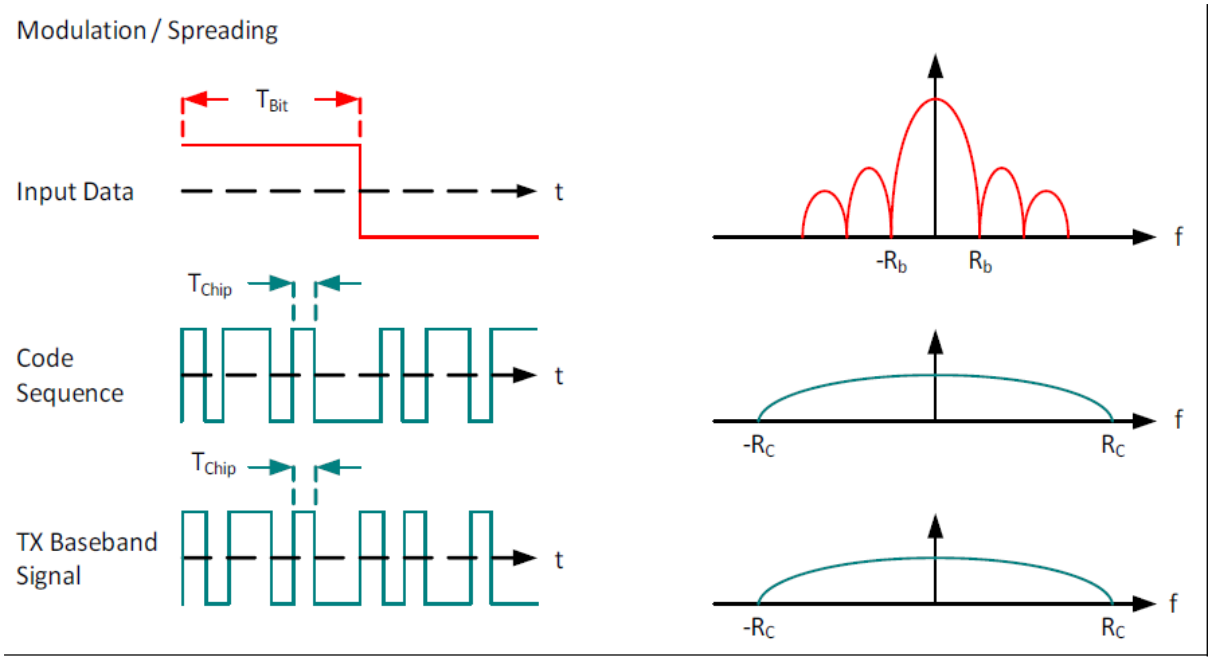

*EM lock :electromechanical lock
*MCU :Micrcontroller unit

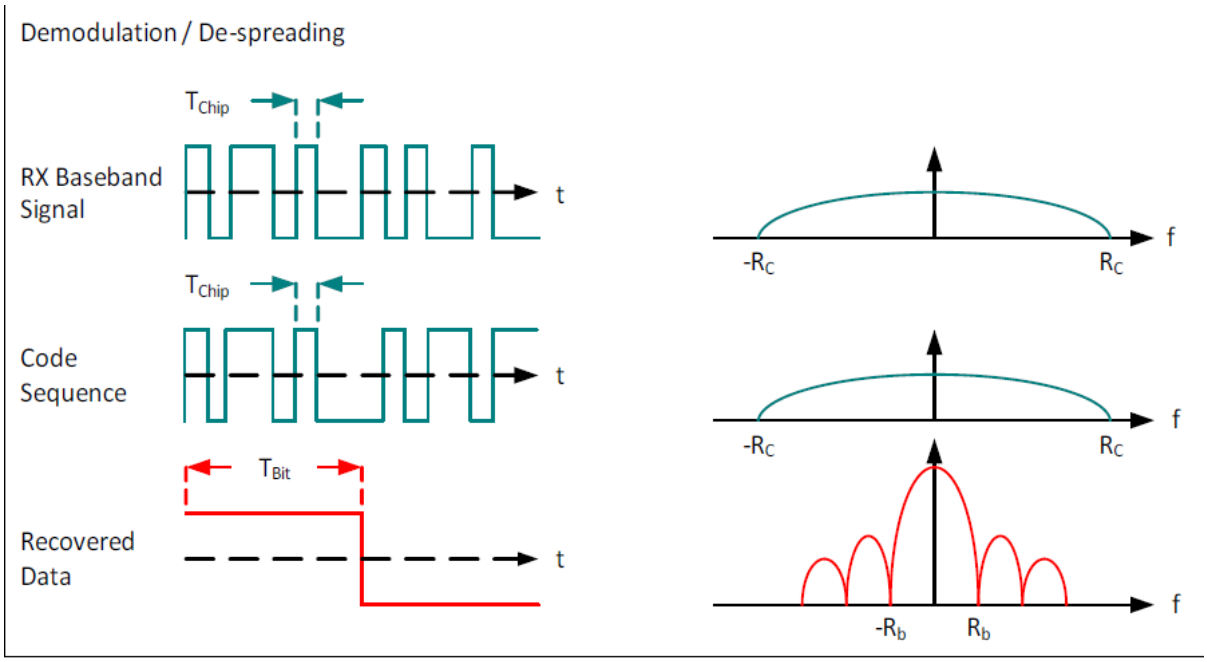
network and their interconnnection for single node

## 2.1. LoRa Modulation:

LoRa is a Spread Spectrum modulation scheme. In LoRa modulation the spreading of the spectrum is achieved by generating a chirp signal that continuously varies in frequency. An advantage of this method is that timing and frequency offsets

between transmitter and receiver are equivalent, greatly reducing the complexity of the receiver design. The frequency bandwidth of this chirp is equivalent to the spectral bandwidth of the signal.




## Key features of LoRa modulation

* LoRa modulation is both bandwidth and frequency scalable

* LoRa is a constant envelope modulation scheme which means that the same low-cost and low-power high-efficiency PA stages can be re-used without modification

* LoRa signal is very resistant to both in-band and out-of-band interference mechanisms

* chirp pulse is relatively broadband and thus LoRa offers immunity to multipath and fading, making it ideal for use in urban and suburban environments, where both mechanisms dominate.

* An inherent property of LoRa is the ability to linearly discriminate between frequency and time errors.

LoRa is the ideal modulation for radar applications and is thus ideally suited for ranging and localization applications such as real-time location services.

## 2.2. Network Architecture:

The system consists of single Server node that acts as a gateway connecting the LoRa network to internet and multiple nodes each node being a LoRa lock. Since LoRa is reliable over long range and the required data is few bytes a single gateway is sufficient for a campus wide node network.

The network structure is single server multiple client model. To establish a successful communication between the nodes and the gate way and a simpler system. A protocol stack as described in below figure has been Implemented.

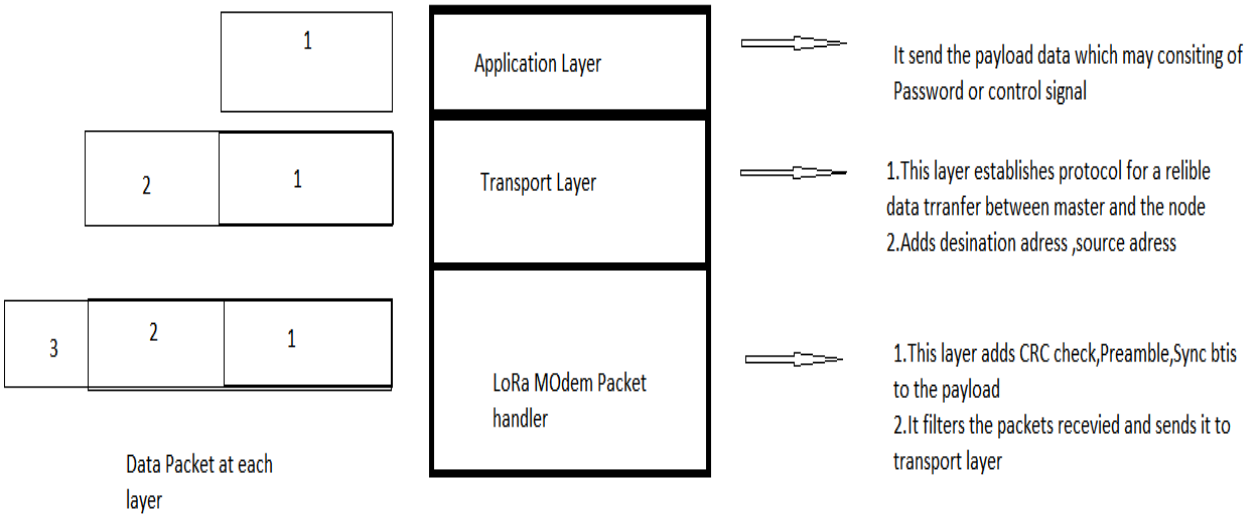



Fig:Communication stack for the network

### 2.2.1. Application layer

This layer manages the sequence of data communication between the node and the server process.

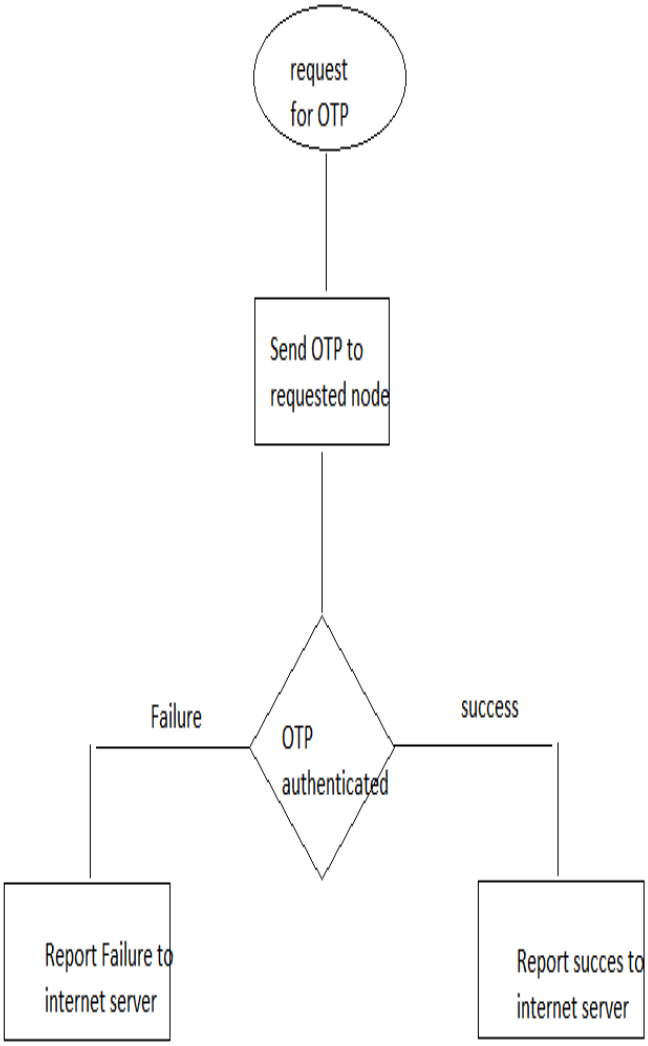
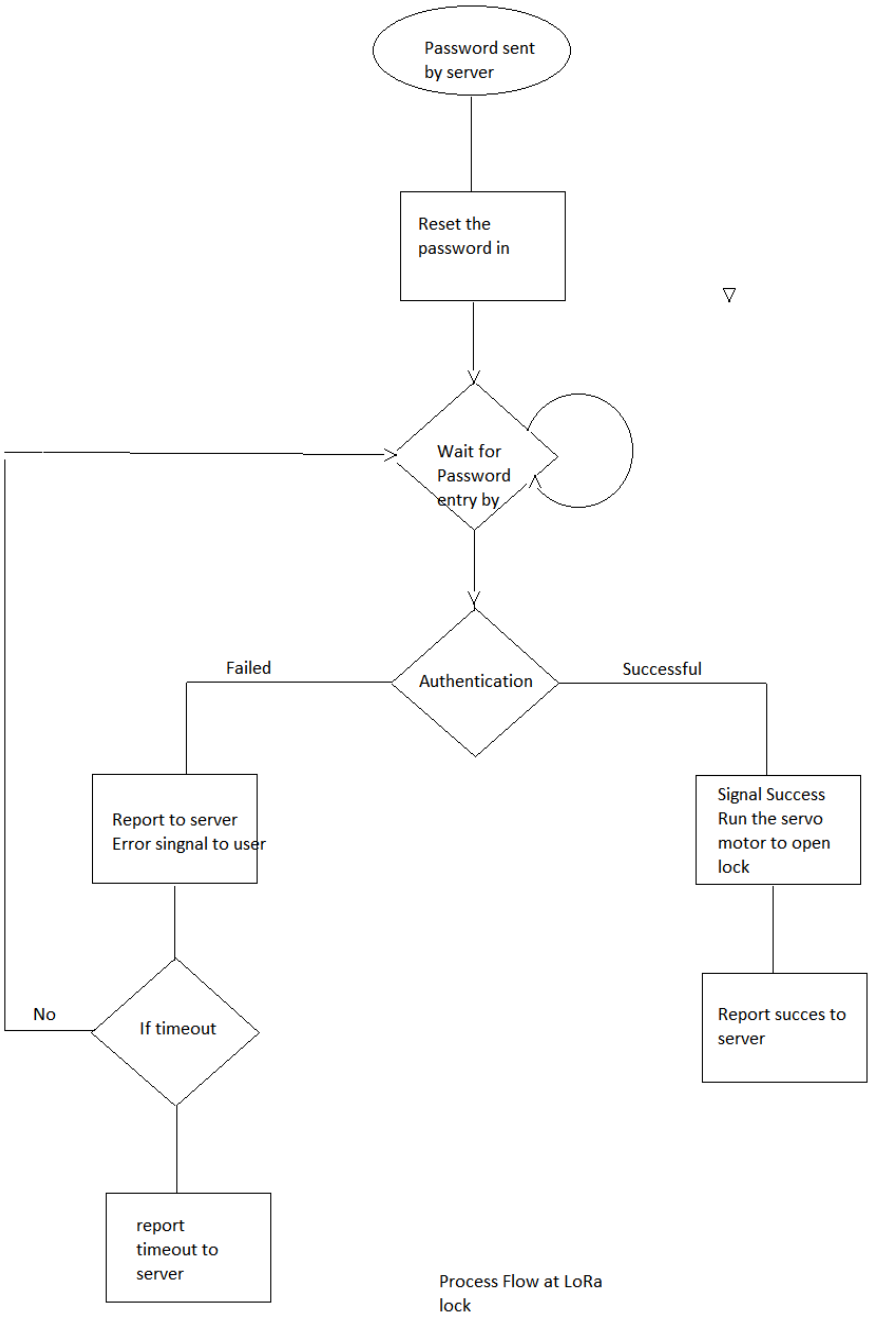



Fig: Application level data flow at server LoRa gateway




Process Flow at LoRa lock

## 2.2.2. Transport layer:

To check packet loss or errors and establishing a reliable communication, the transport layer is implemented on the principles of reliable data transfer. With tools like timers, ACK signals reliable data transfer has been ensured.

The following  Protocol has been implemented to establish reliable data transfer(rdt)

Sender side:

It keeps sending the of a particular sequence number packet until acknowledgement is received if acknowledgement is received with an acknowledged sequence same as the sent packet sequence number increment the sequence number

Receiver side:

If the packet is received correctly it sends an acknowledgement.

### 2.2.3. SX1272 LoRa Modem and Packet handler :

@transmitter end: This layer adds header and sync bits and CRC check bits to the pay load thus completing the packet .

@Receiver end: This processes the received packets, filters them and transfers the data to transport layer. It does error checks Based on CRC and drops the packet if there is an error

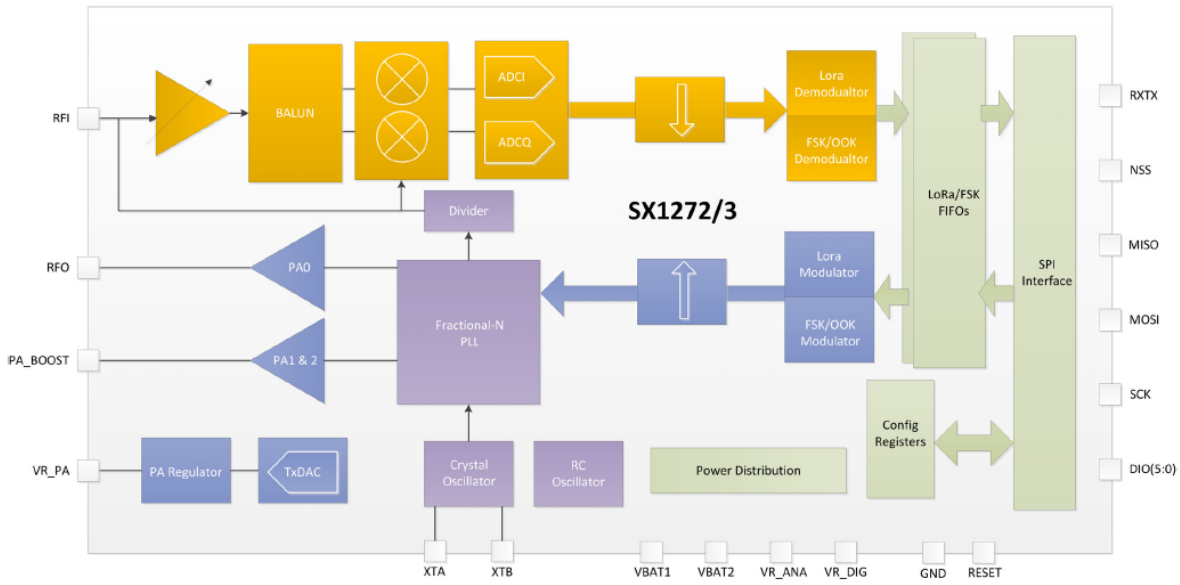



*Figure 1. SX1272/73 Block Diagram*

## 2.3. SPI communication:

SX1272 IC is manipulated for different configurations and data transmission or reception using SPI communication between Microcontroller and SX1272.

The SPI interface gives access to the configuration register via a synchronous full-duplex protocol corresponding to CPOL = 0 and CPHA = 0 in Motorola/Freescale nomenclature. Only the slave side is implemented.

Three access modes to the registers are provided:

i. SINGLE access: an address byte followed by a data byte is sent for a write access whereas an address byte is sent and a read byte is received for the read access. The NSS pin goes low at the beginning of the frame and goes high after the data byte.

ii. BURST access: the address byte is followed by several data bytes. The address is automatically incremented internally between each data byte. This mode is available for both read and write accesses. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer

iii. FIFO access: if the address byte corresponds to the address of the FIFO, then succeeding data byte will address the FIFO. The address is not automatically incremented but is memorized and does not need to be sent between each data byte. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.

The figure below shows a typical SPI single access to a register

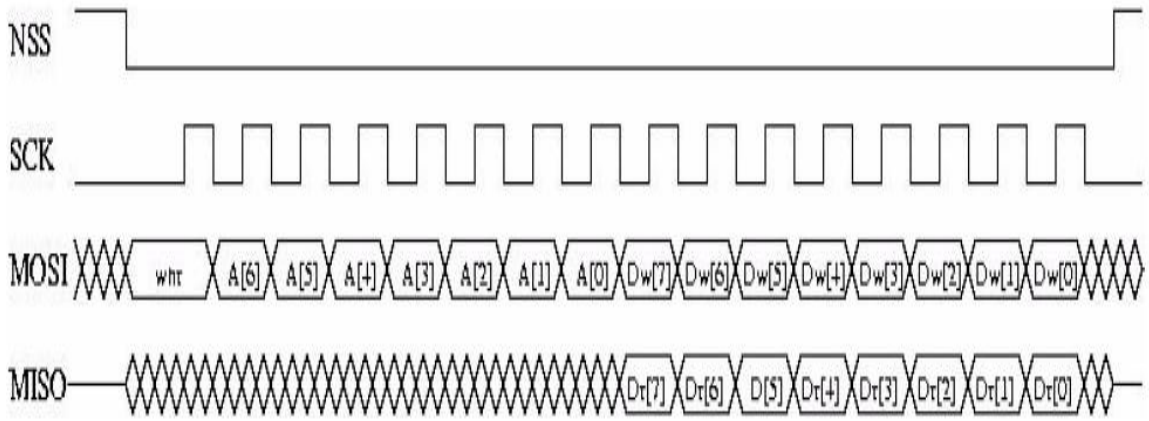



*Figure 39. SPI Timing Diagram (single access)*

A transfer is always started by the NSS pin going low. MISO is high impedance when NSS is high.

The first byte is the address byte. It is comprises:

The second byte is a data byte, either sent on MOSI by the master in case of a write access or received by the master on MISO in case of read access. The data byte is transmitted MSB first.

*A wnr bit, which is 1 for write access and 0 for read access.

* Then 7 bits of address, MSB first.

## 2.4. Configuration of SX1272 IC

### Transceiver Configurations

Bandwidth :125kHz
Frequency :868Mhz
Spreading factor : 7
RF op power : -1 dbm to 20 dbm

### SPI configuration s

Bitrate=4Mhz
CPOL = 0
CPHA = 0

## 2.5. Components For Prototype:

### 2.5.1. For client node

Atmega328P microcontroller

SX1272 IC

Servo motor

Keypad

LEDs

Power Source 5V

Voltage regulators 5V

Capacitors 22pF x2

Clock 16Mhz

### 2.5.2. For Server node

Arduino

Personal Computer (To connect to the Internet Server)

SX1272 LoRa Transceiver IC

## 3. Circuit Diagram:

## For the node :

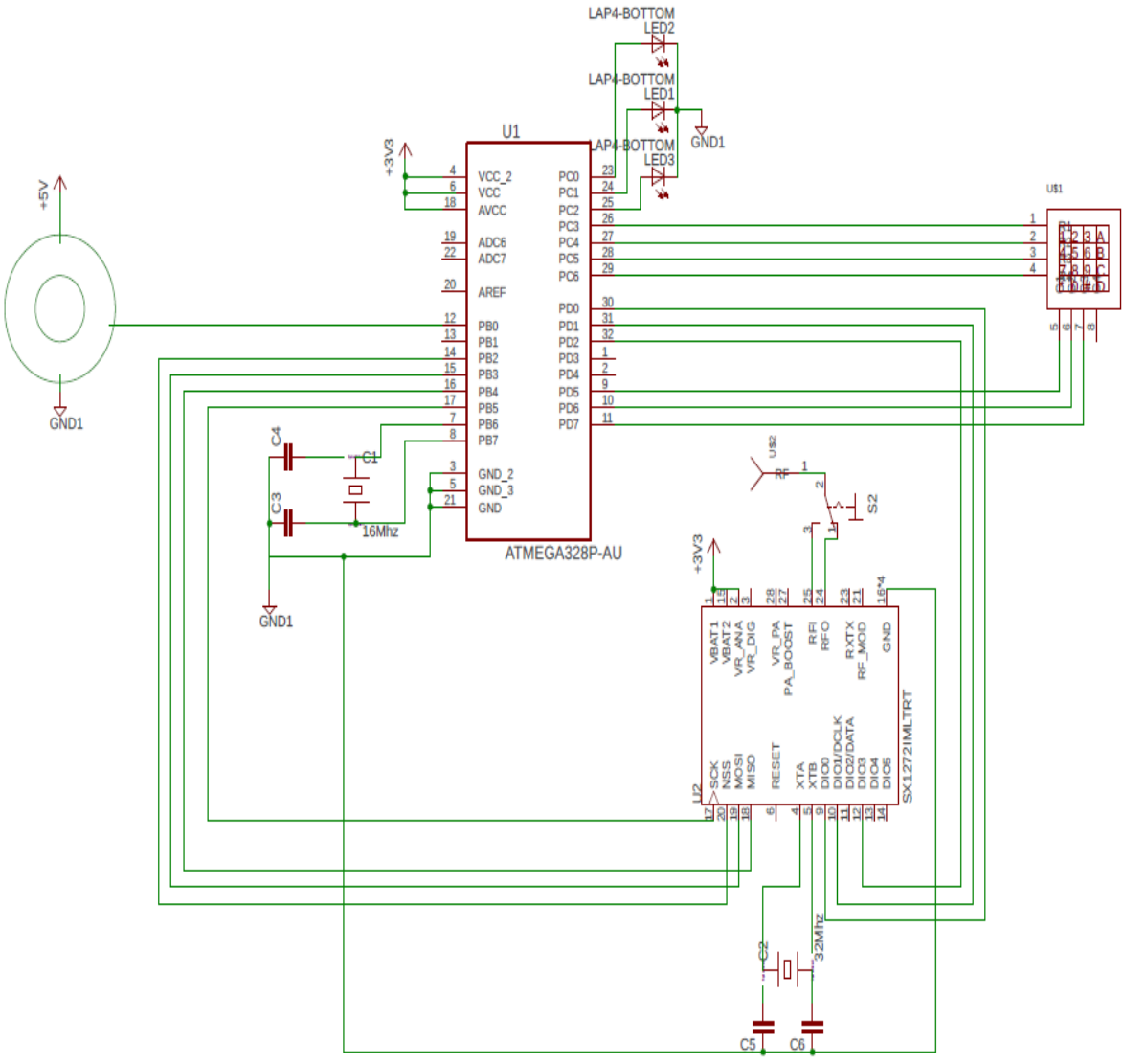
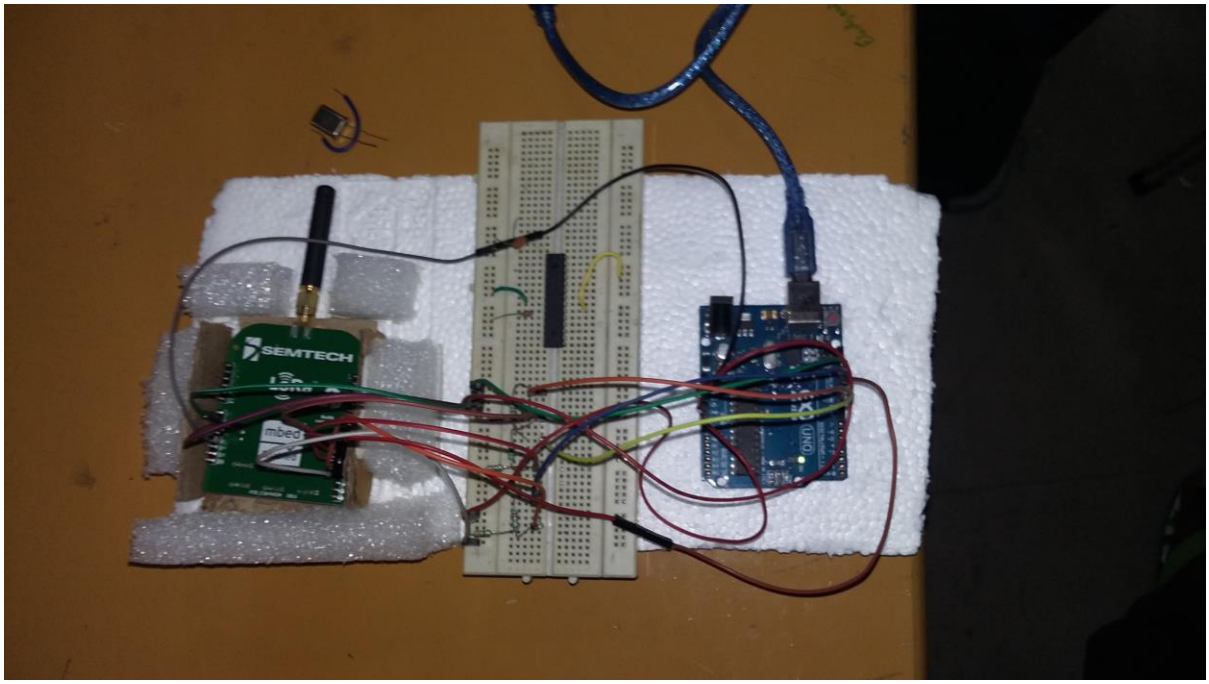



*Figure 1: LoRa Lock Node*

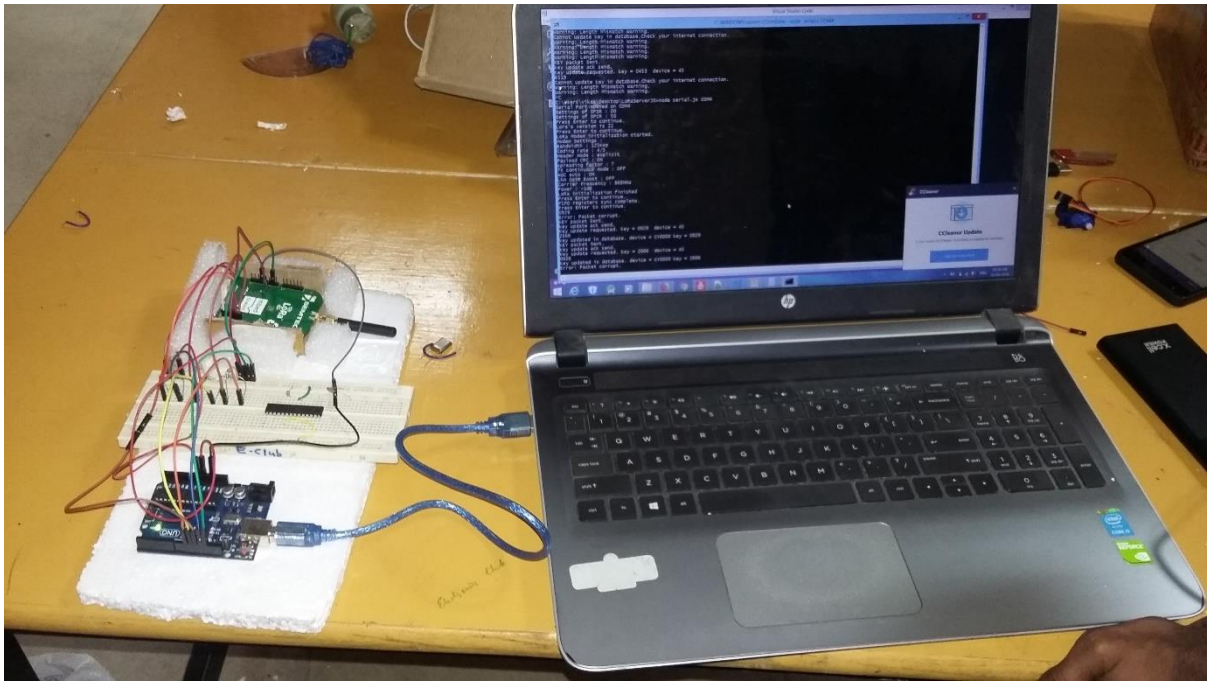
## 4. Results :

1.The following systems have been built and tested.

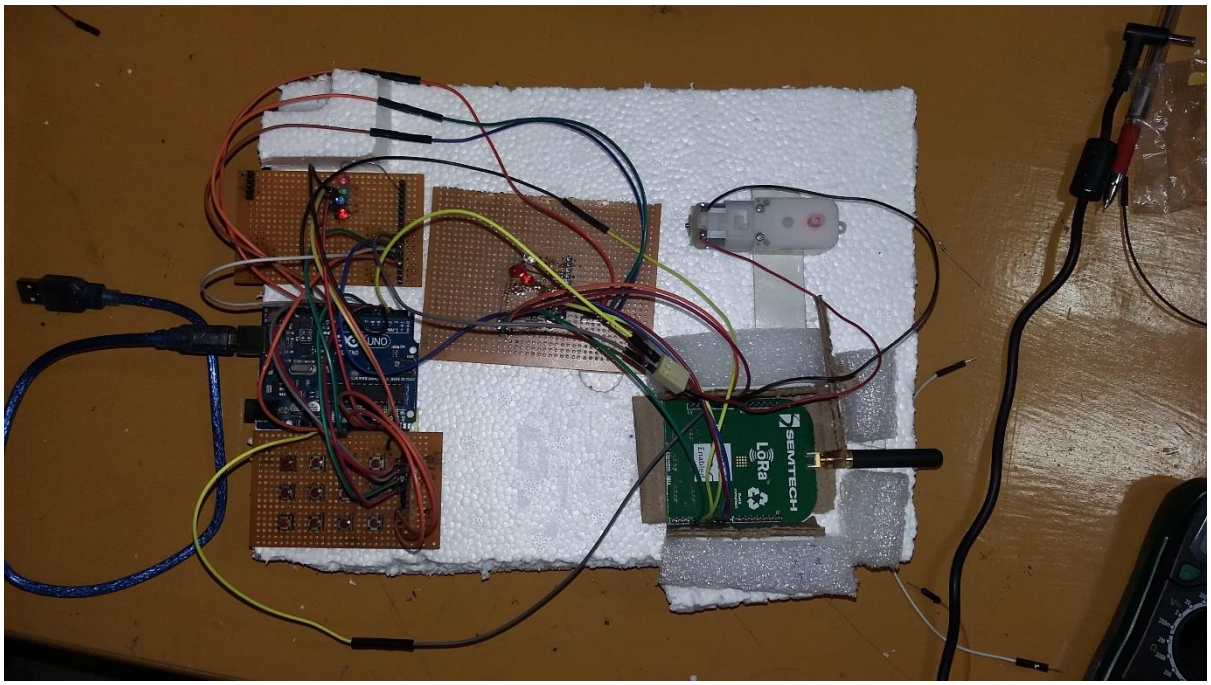
a)Server node



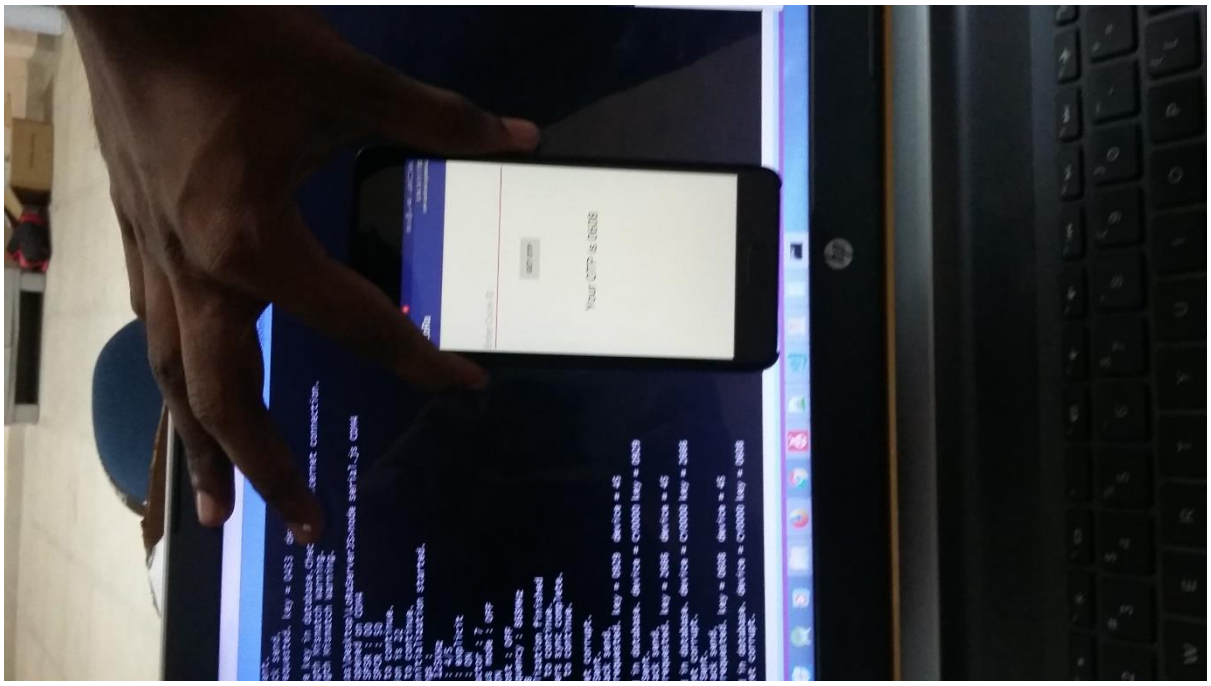

b)server node with PC executing necessary software



c) the  LoRa lock node (client)




d) The user interface



## 5. Potential of the project:

This kind of authentication system over using lora is very apt for a campus wide public cycle system.A public cycle system has been initiated by IIT Guwahati known as “Green Cycles”. But this initiative

apparently failed because of no proper authentication system Our project shows solution to the issue.

Low power and Long range of LoRa modulation based RF transmitter receiver will enable in building a sustainable and low cost public cycle sytem.