भारतीय सूचना प्रौद्योगिकी संस्थान, नागपुर
Indian Institute of Information Technology, Nagpur
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CMOS

Project Report

Designing of 2:4 Decoder

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Submitted to -

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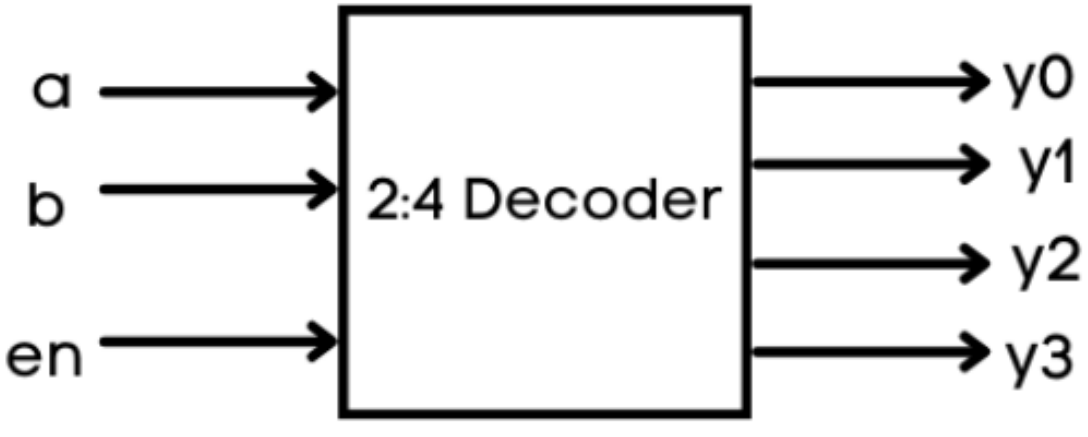
■Theory:

Decoder is a combinational circuit that has ‘n’ input lines and maximum of 2n output lines. One of these outputs will be active High based on the combination of inputs present when the decoder is enabled. That means decoder detects a particular code. The decoder outputs are nothing but the min terms of ‘n’ input variables lines when enabled.

A decoder is a combinational logic circuit that has ‘n’ input signal lines and 2n output lines. In the 2:4 decoder, we have 2 input lines and 4 output lines. In addition, we provide ‘*enable*‘ to the input to ensure the decoder functions whenever Enable is 1 and it is turned off when Enable is 0. The truth table, logic diagram, and logic symbol are given.

■Decoder Diagram:

The Circuit Diagram of the 2:4 Decoder with enabled input using and not gate is shown below:

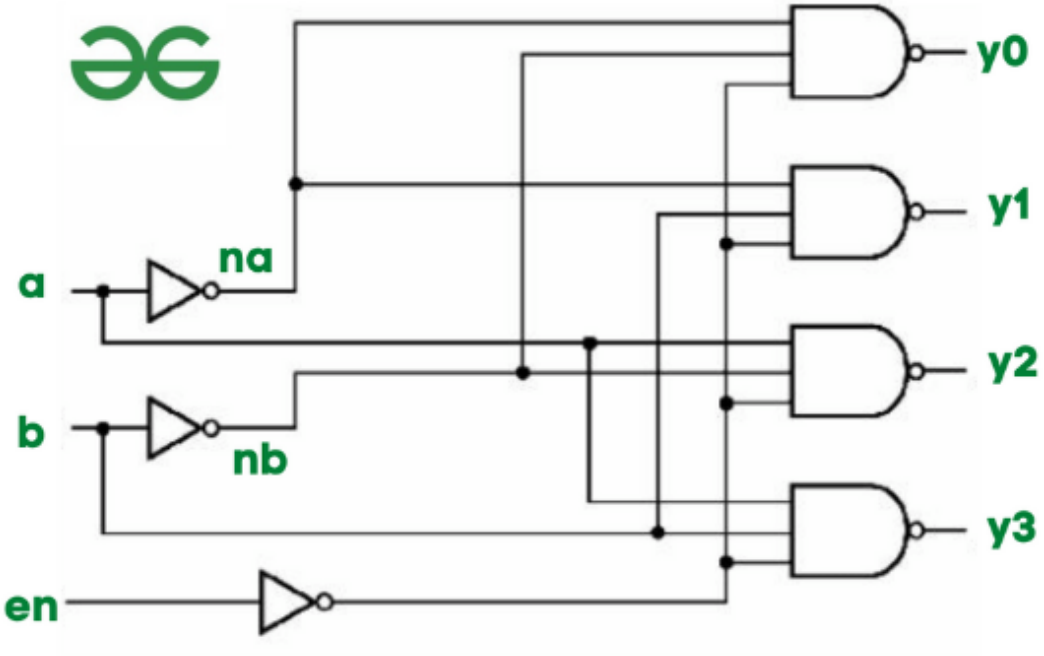


■Truth Table:

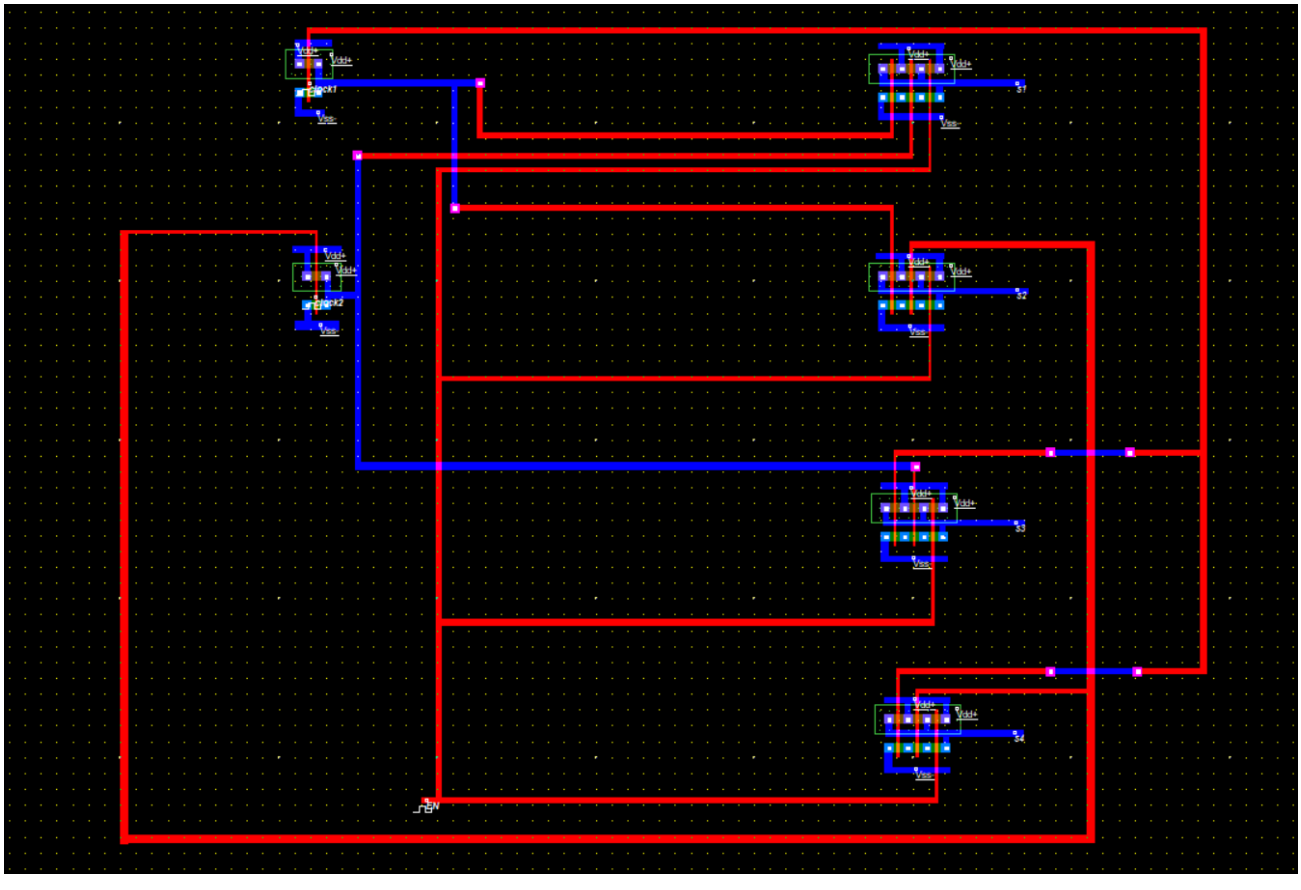
En	Input		Output			
	a	b	y3	y2	y1	y0
1	x	x	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1

■Circuit Diagram:

Each output is having one product term. So, there are four product terms in total. We can implement these four product terms by using four AND gates having three inputs each & two inverters. The **circuit diagram** of the 2: 4 decoder is shown in the following figure.



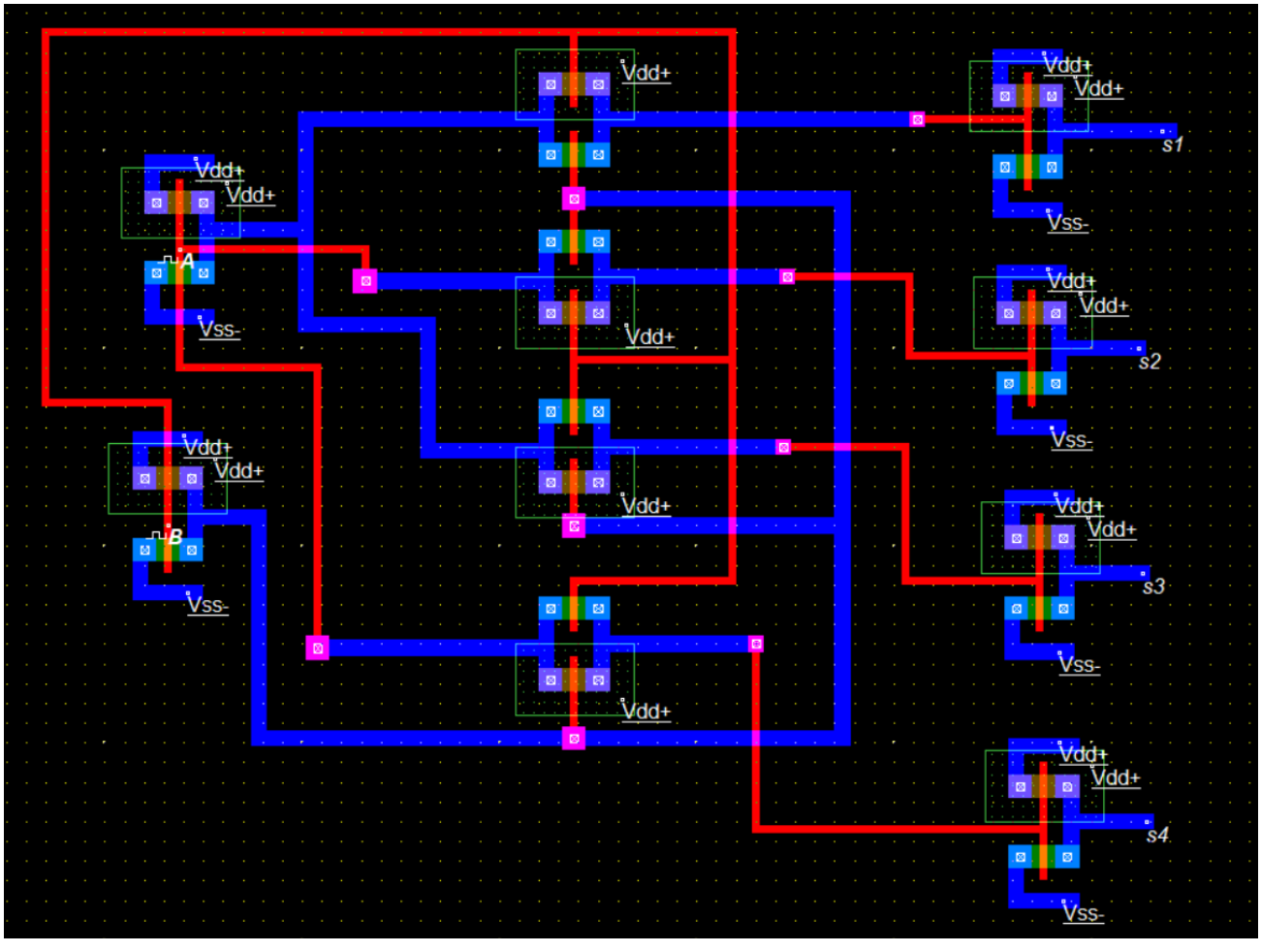
■Implementation using Cmos(Microwind layout):



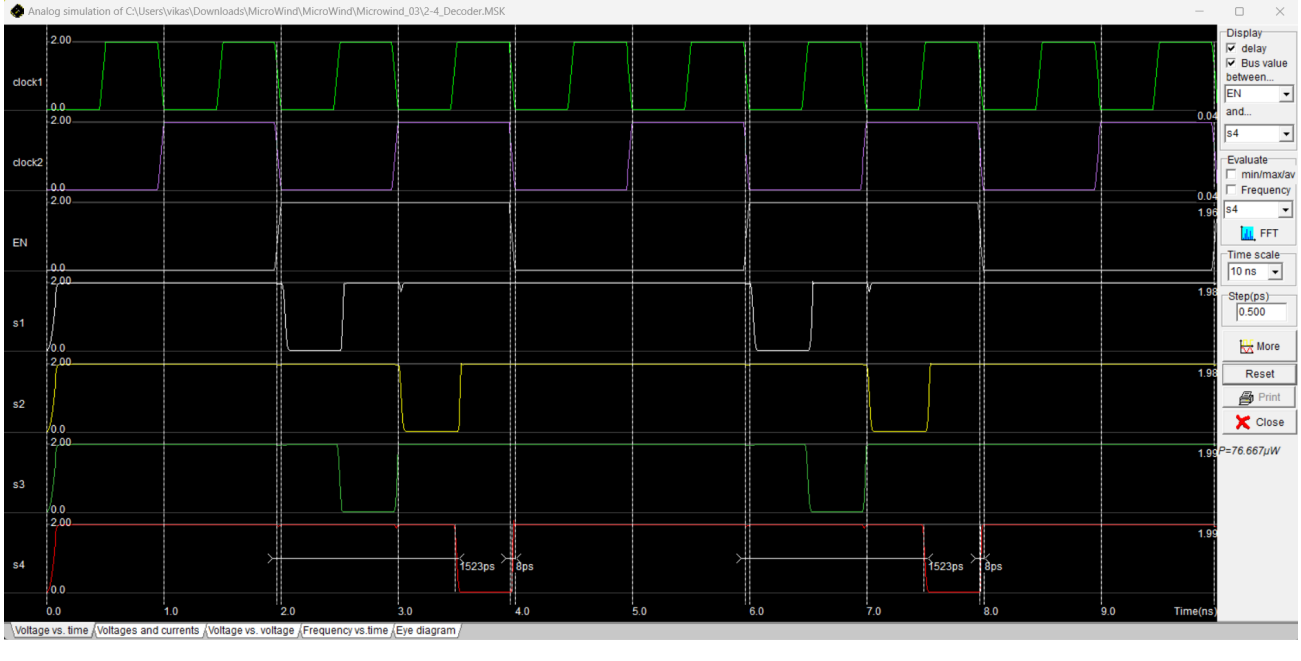
Here we have used NAND and NOT gate for designing this decoder. Every NOT gate contains single pmos and nmos similarly every single 3 input NAND gate contains 3 pmos and 3 nmos. So here we used a total of 28 transistors.

So For Reducing Power Consume and reducing the number of gates we optimize this circuit by using Transmission Gates.

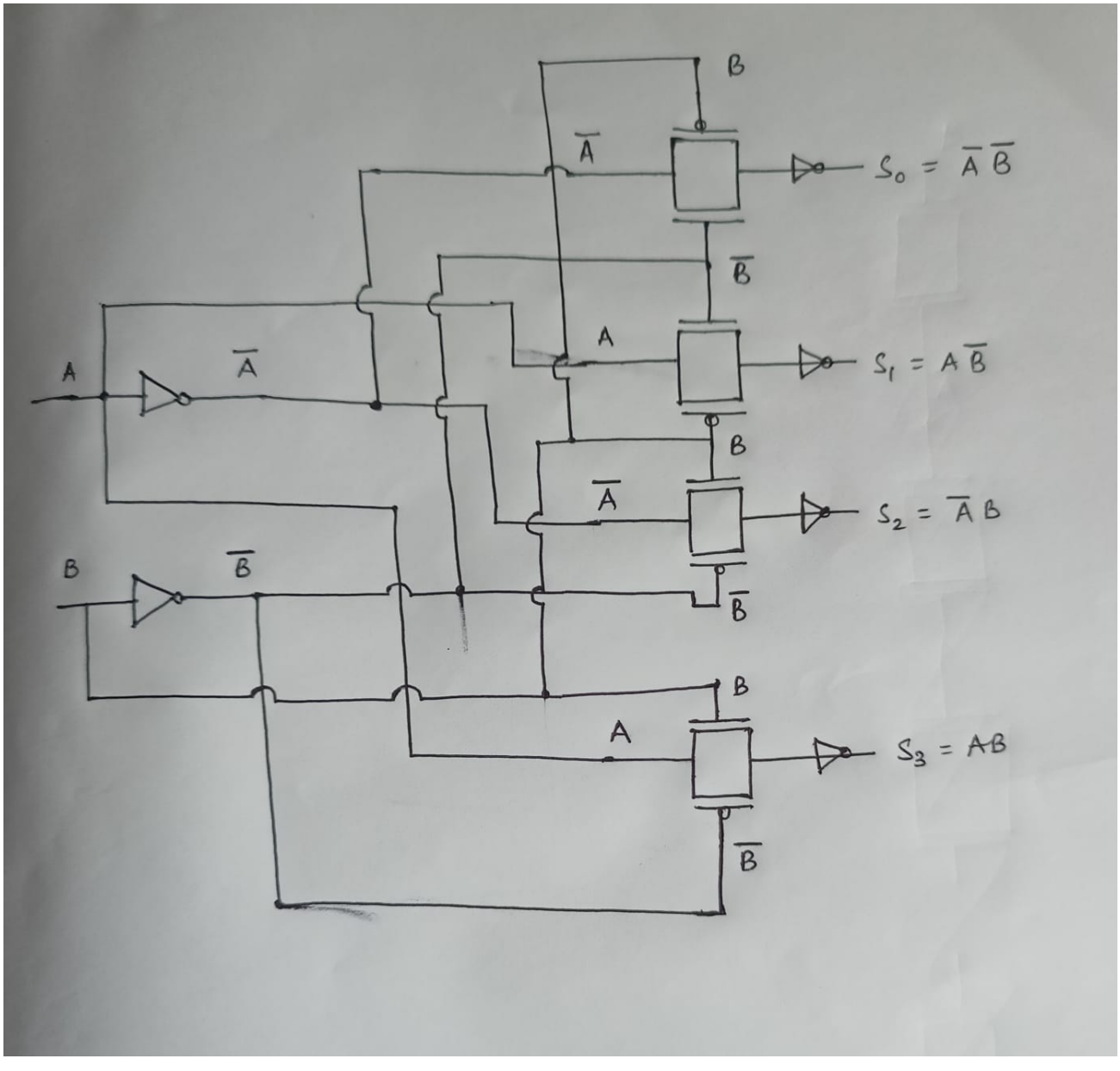
■Implementation using Transmission Gate (Microwind layout)(Optimized Circuit):



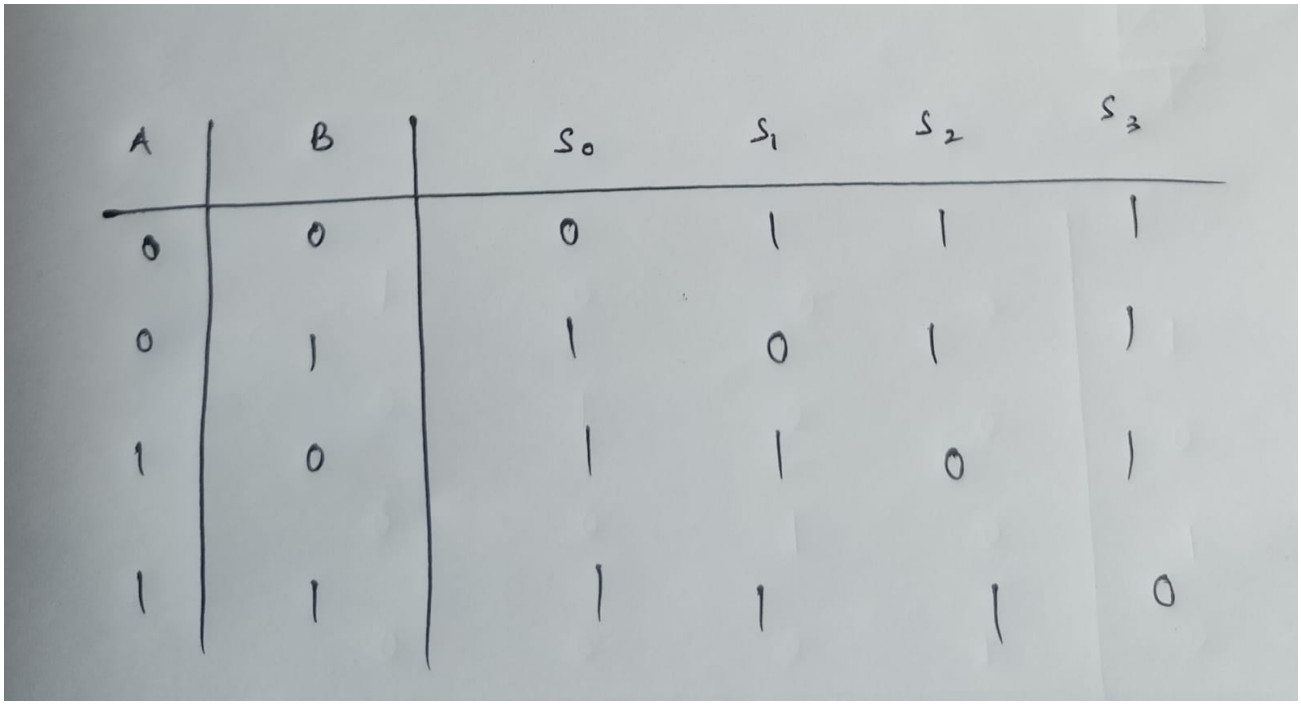
■Output:



In this optimized circuit we use less number of mos gates and the output is the same as the previous circuit.



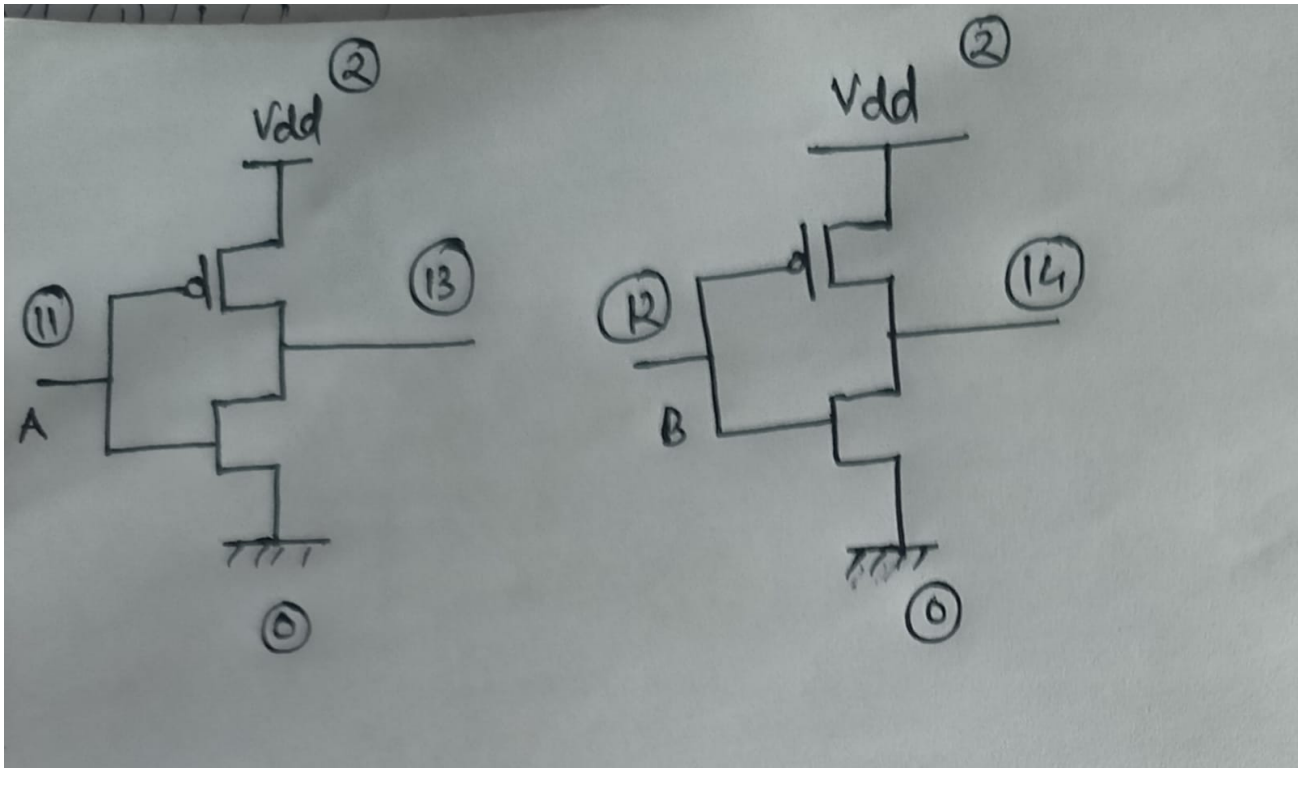
Truth Table for the above circuit -

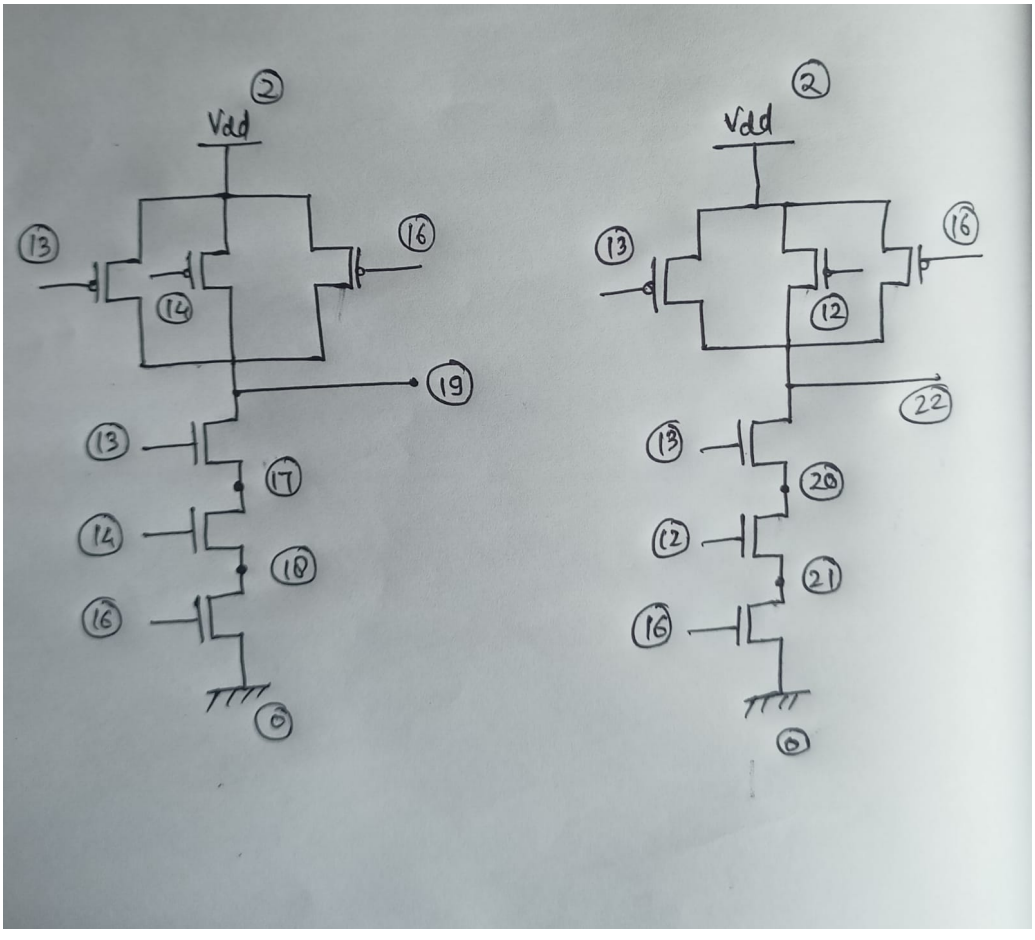


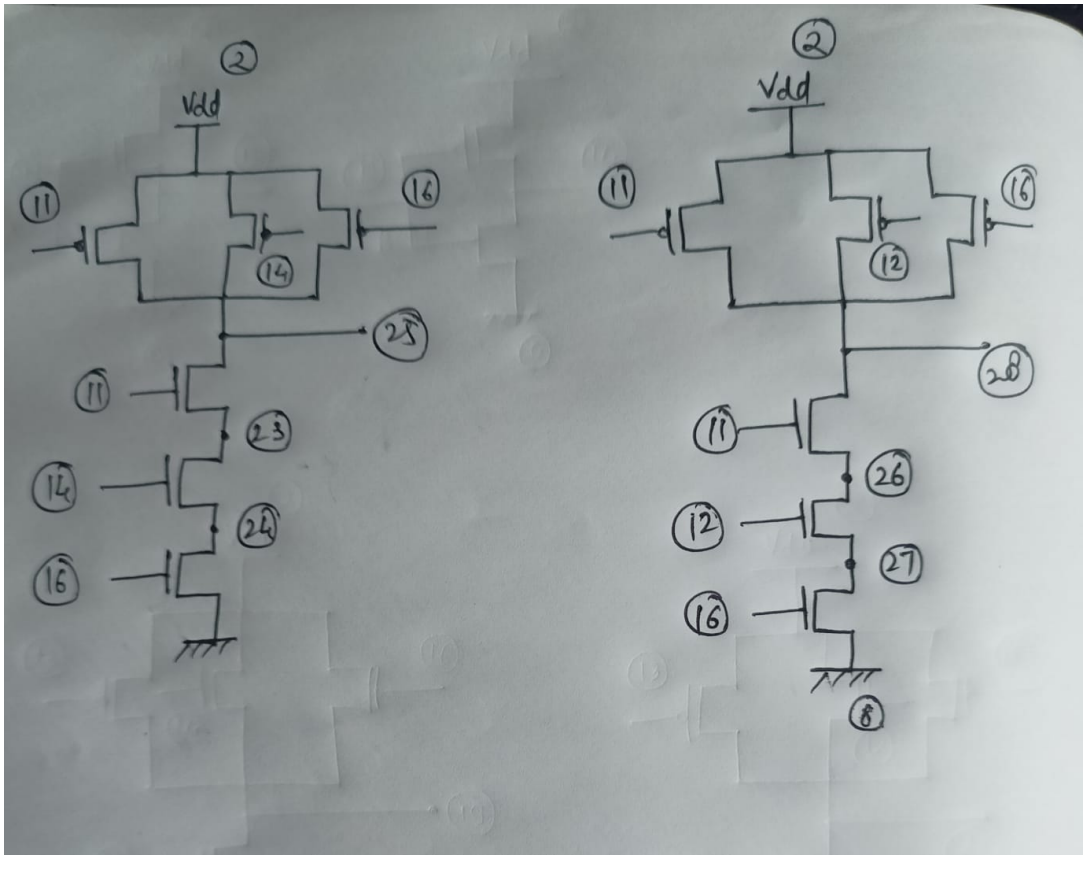
A	B	S_0	S_1	S_2	S_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

■Ngspice NetList:

Circuit components design with node numbering(3 NOT Gate, 4 NAND Gate)-




2
Vdd
13
16
14
19
13
17
14
18
16
0
2
Vdd
13
16
12
22
13
20
12
21
16
0


2
Vdd
11
16
14
25
11
23
14
24
16
2
Vdd
11
16
12
28
11
26
12
27
16
8

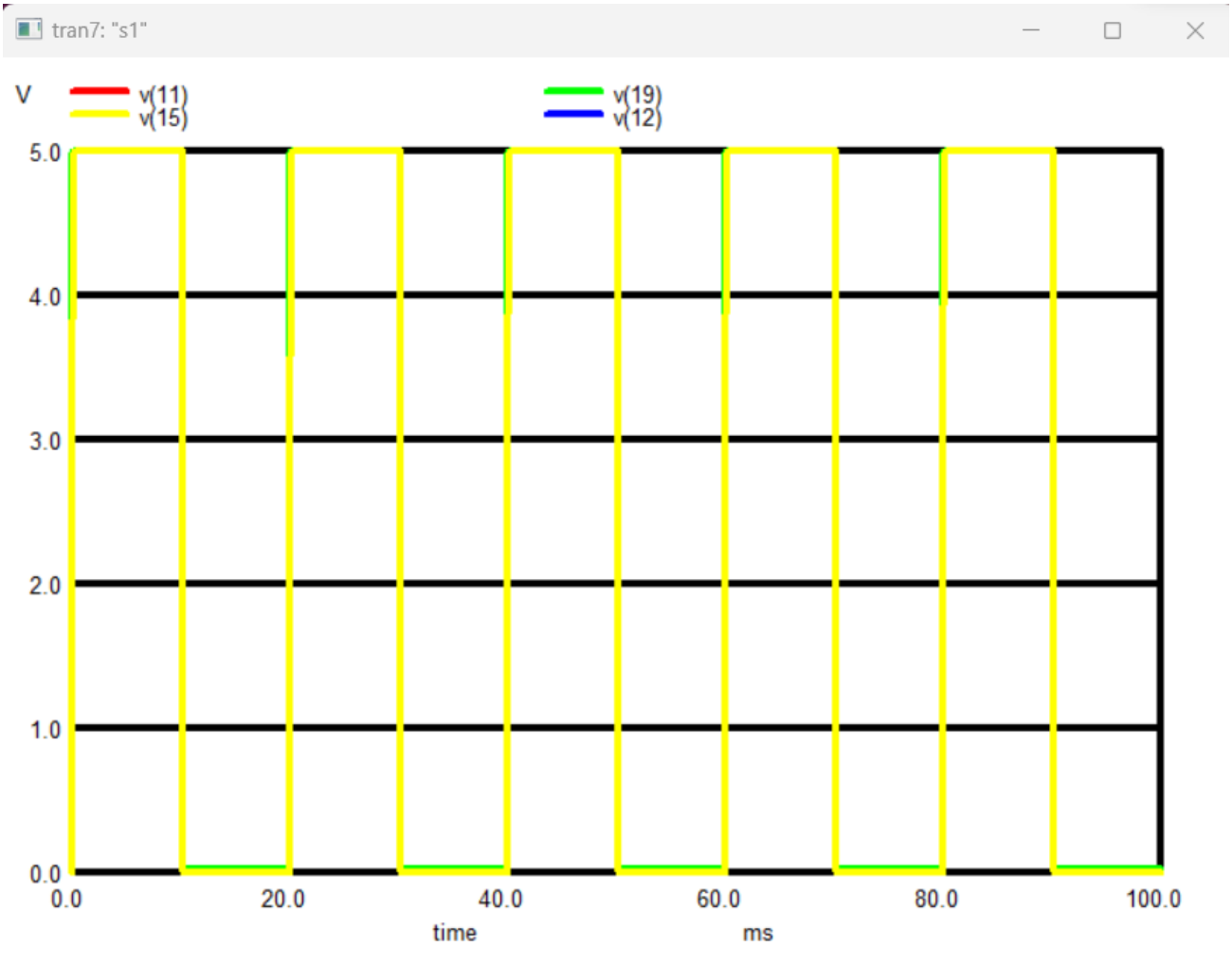
Ngspice NetList -

```
***Cmos_Project_1

Vx 11 0 pulse(0 5 0 0 0 10m 20m)
Vy 12 0 pulse(0 5 0 0 0 10m 20m)
Vz 15 0 pulse(0 5 0 0 0 10m 20m)
vdd 2 0 dc 5v

.model nmod nmos version=54 level=4.7
.model pmod pmos version=54 level=4.7

m11 13 11 0 0 nmod w=100u l=10u
m12 13 11 2 2 pmod w=100u l=10u

m13 14 12 0 0 nmod w=100u l=10u
m14 14 12 2 2 pmod w=100u l=10u

m15 16 15 0 0 nmod w=100u l=10u
m16 16 15 2 2 pmod w=100u l=10u

m17 19 13 17 17 nmod w=100u l=10u
m18 17 14 18 18 nmod w=100u l=10u
m19 18 16 0 0 nmod w=100u l=10u
m20 19 13 2 2 pmod w=100u l=10u
m21 19 14 2 2 pmod w=100u l=10u
m22 19 16 2 2 pmod w=100u l=10u
```

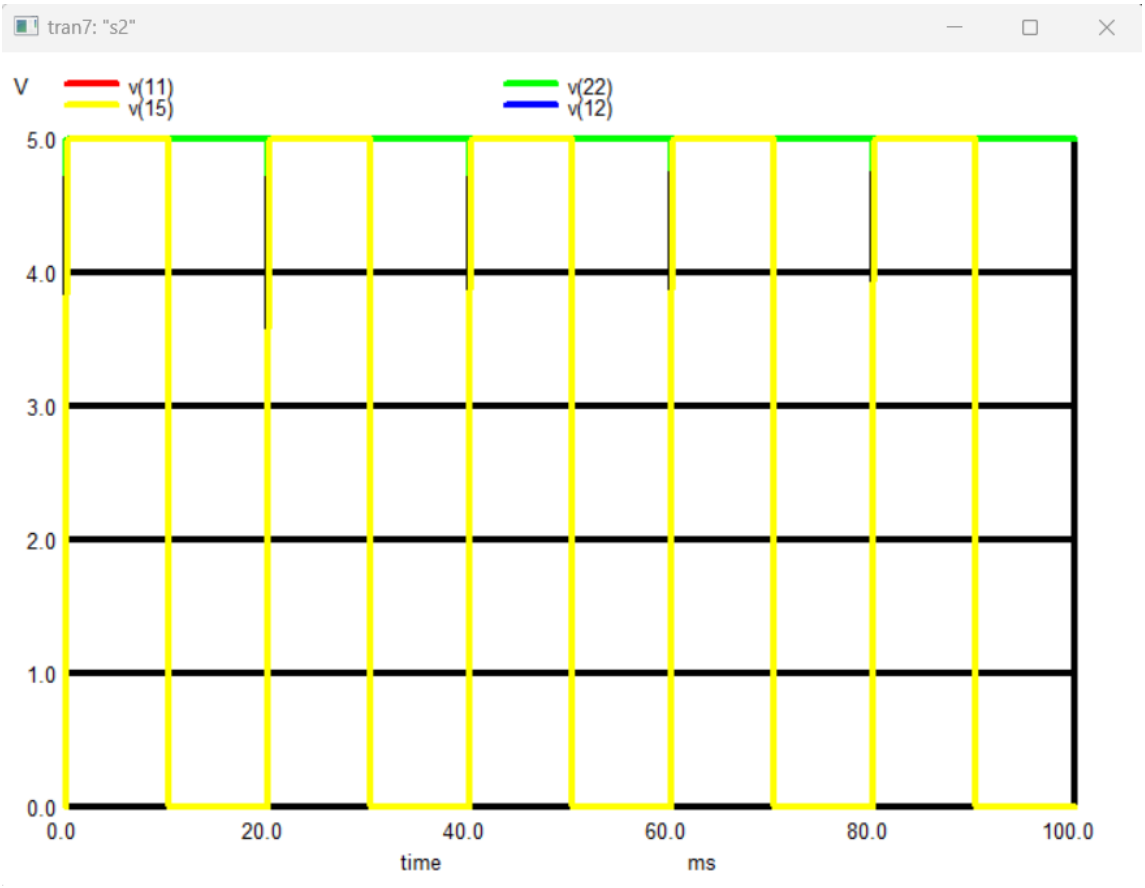
```
m23 22 13 20 20 nmod w=100u l=10u
m24 20 12 21 21 nmod w=100u l=10u
m25 21 16 0 0 nmod w=100u l=10u
m26 22 13 2 2 pmod w=100u l=10u
m27 22 12 2 2 pmod w=100u l=10u
m28 22 16 2 2 pmod w=100u l=10u

m29 25 11 23 23 nmod w=100u l=10u
m30 23 14 24 24 nmod w=100u l=10u
m31 24 16 0 0 nmod w=100u l=10u
m32 25 11 2 2 pmod w=100u l=10u
m33 25 14 2 2 pmod w=100u l=10u
m34 25 16 2 2 pmod w=100u l=10u

m35 28 11 26 26 nmod w=100u l=10u
```

```
m36 26 12 27 27 nmod w=100u l=10u
m37 27 16 0 0 nmod w=100u l=10u
m38 28 11 2 2 pmod w=100u l=10u
m39 28 12 2 2 pmod w=100u l=10u
m40 28 16 2 2 pmod w=100u l=10u


.tran 0.1m 100m
.control
run
set color0 = white
set color1 = black
set xbrushwidth =4.5
plot V(19) V(11) V(12) V(15) title "s1"
plot V(22) V(11) V(12) V(15) title "s2"
plot V(25) V(11) V(12) V(15) title "s3"
plot V(28) V(11) V(12) V(15) title "s4"
.endc
.end
```

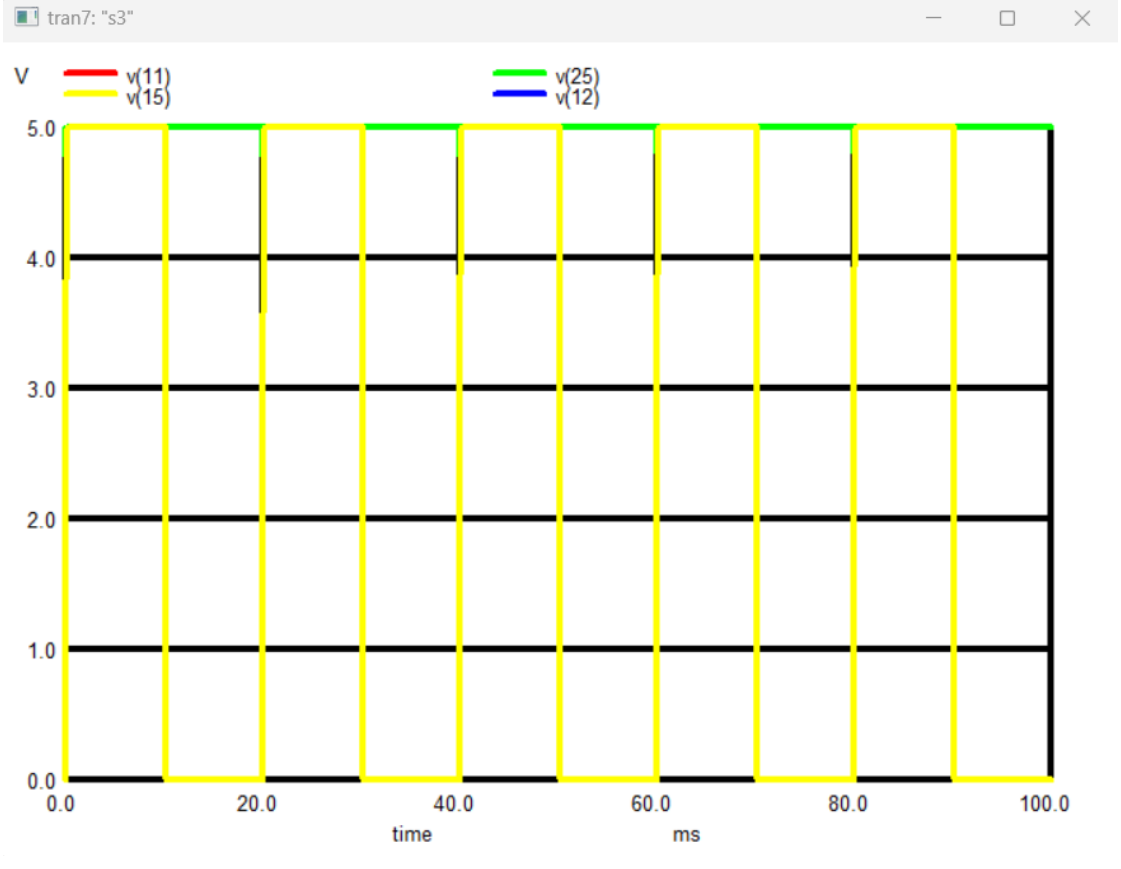
Output - (For S1 vs input)



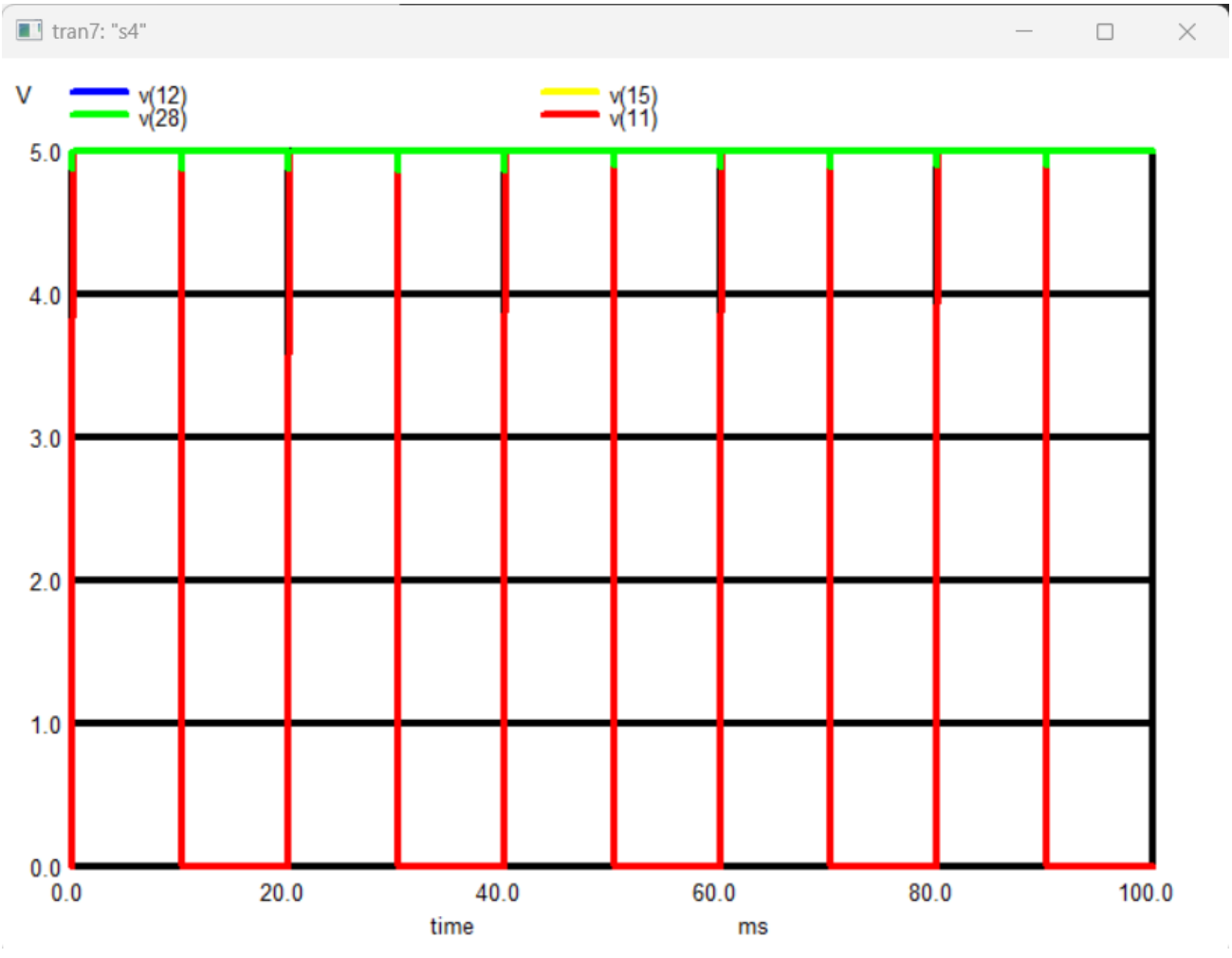
(For S2 vs input)



(For S3 vs input)



(For S4 vs input)



■Conclusion:

We have successfully implemented the 2:4 decoder using CMOS technology and the transmission gate and verified the output using the truth table of that circuit. Using that we have also created the netlist in the ngspice software and observed all outputs wrt the given inputs.