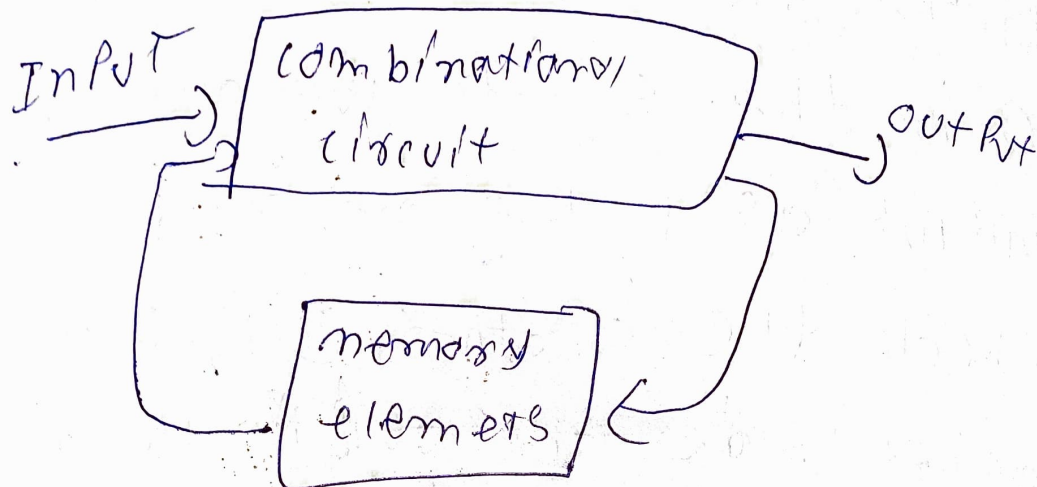


Unit 6 Sequential Circuits



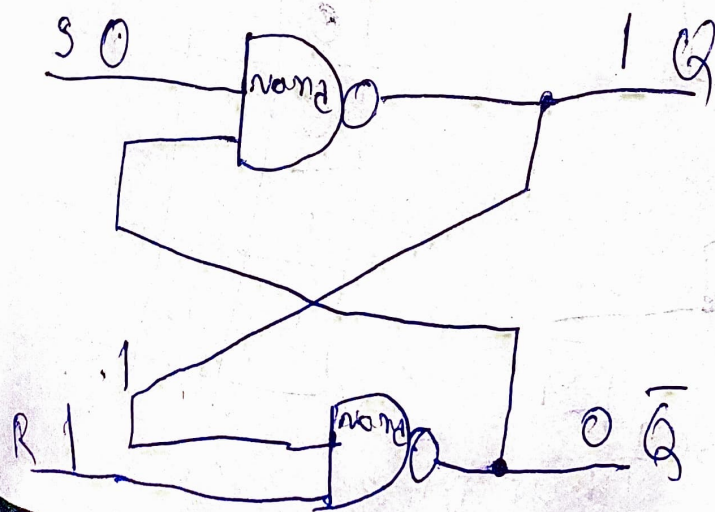
SR latch using NAND gate

NAND gate

Input	Output
0 0	1
0 1	1
1 0	1
1 1	0

Case 1

(0, 1)



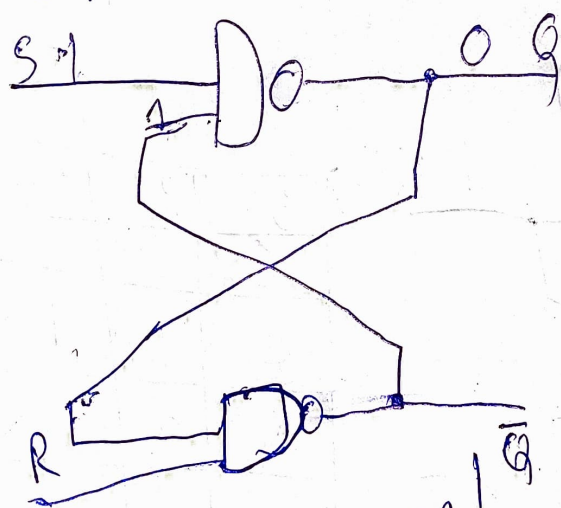
S	R	Q(n+1)
0	0	
0	1	1
1	0	
1	1	

Explanation

In the SR when we give output 0 on the S side we get the output as 1, we not need to check the another I/P, & on the other side the output is 1 & 1 so the output is 0, & the both the outputs will be complement.

Case 2

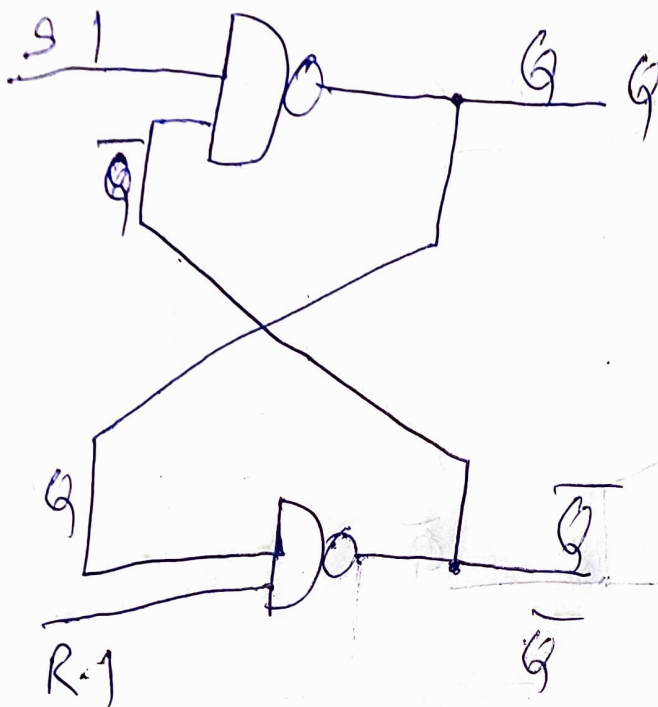
(1, 0)



S	R	Q(next)
0	0	
0	1	
1	0	0
1	1	

same as case 1 but vice versa

Case 3 (1,1)



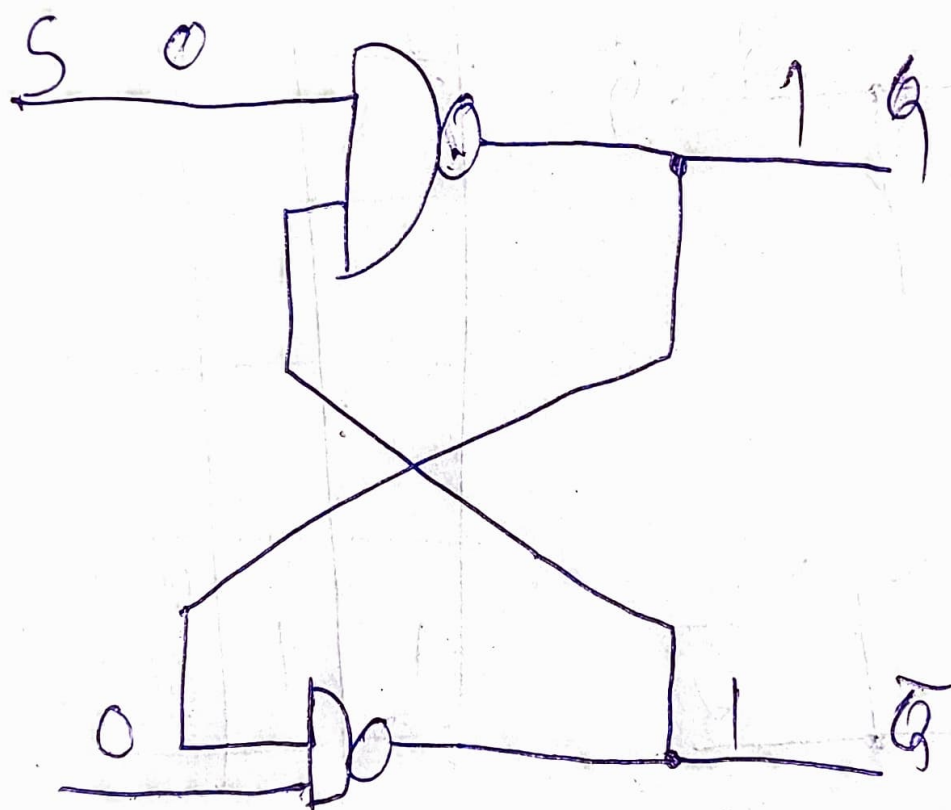
S	R	Q (next)
1	1	Hold State

$$\begin{array}{c|c}
 \overline{1} \cdot \overline{1} & \overline{1} \cdot \overline{1} \\
 \overline{1} + \overline{1} & 0 + \overline{1} \\
 0 + \overline{1} &
 \end{array}$$

Explanation

In the above we have give (1,1) as Input, by the Inputs S will get $\overline{1}$ & R will get $\overline{1}$ as Input & we will get output as $\overline{1}, \overline{1}$ & It will get into hold state

Case 4 (0,0)



S	R	Q (next)
0	0	Invalid
0	1	0
1	0	1
1	1	0

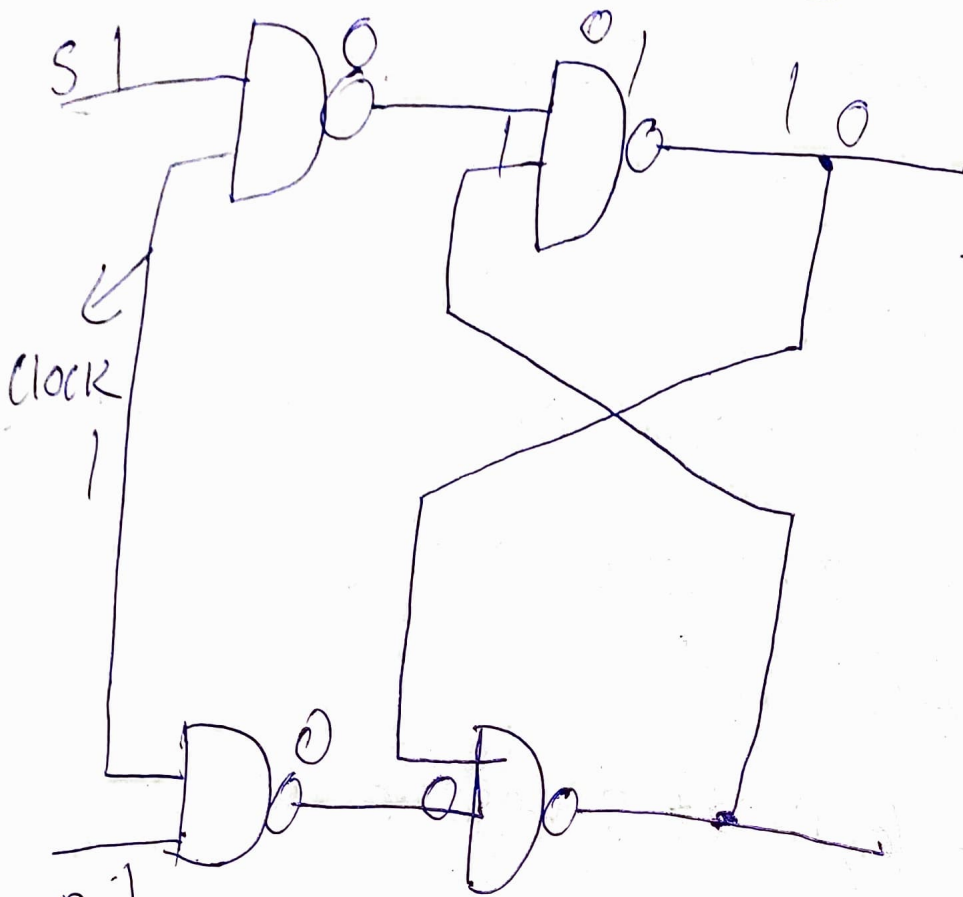
R

exp Here we took the I/P as 0,0

& got o/p as 1,1.

→ by rule we should get the o/p complement but we are getting same so it becomes Invalid state.

SR flip flop & A NAND gate



R
S latch

S	R	Q(n+1)
0	0	Inv
0	1	1
1	0	0
1	1	Held

Clock	S	R	Q _{n+1}
not Trigg	X	X	Q _n
Trigg	0	0	Hold
Trigg	0	1	0 → Reset
Trigg	1	0	1 → Set
Trigg	1	1	Invalid

Explanation

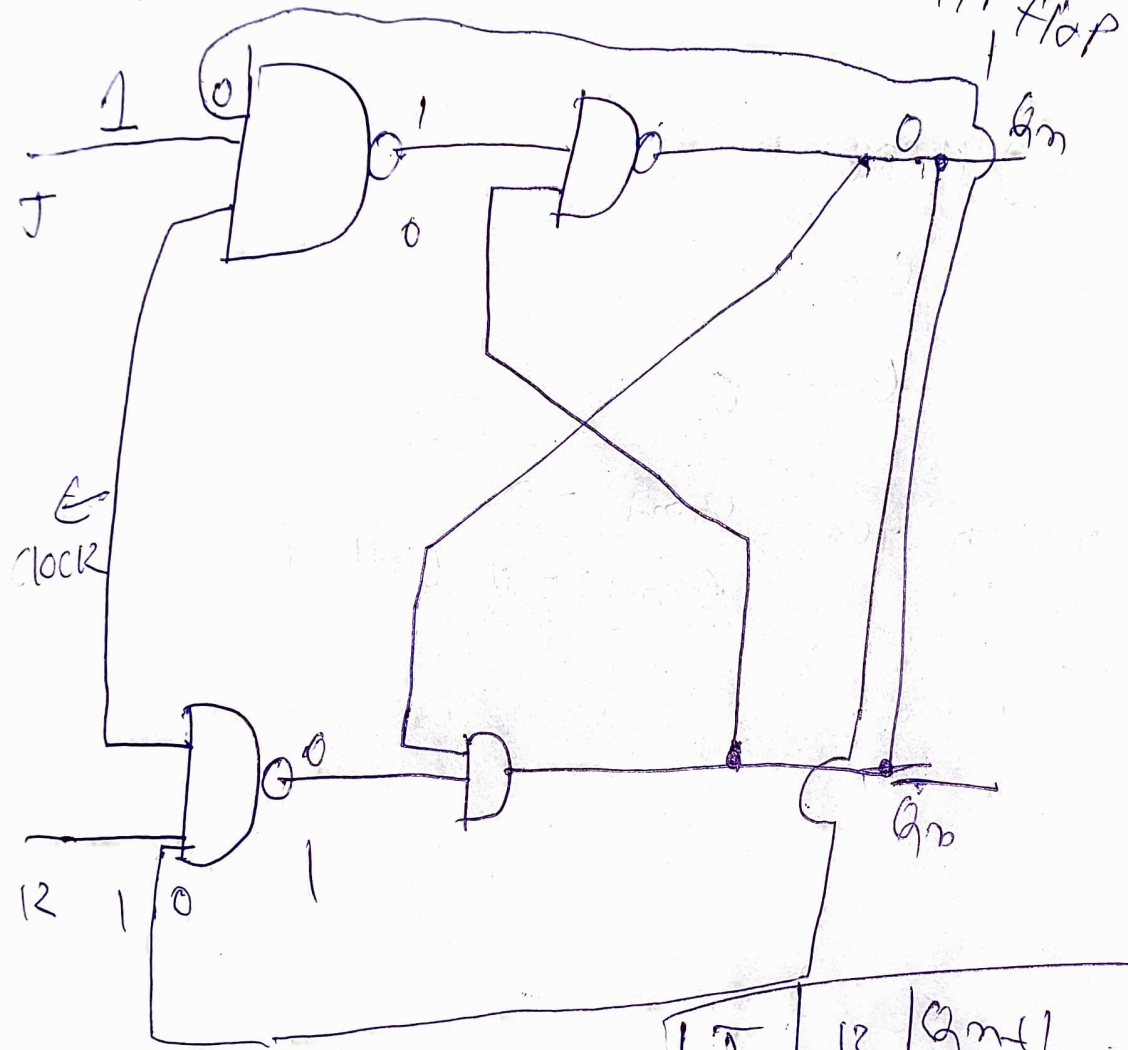
- When the clock does not trigger it does not give output
- When the clock is trigger at the I/P 0,0 it gives Hold state
- At (0,1) it gives 0, which is called Reset
- At (1,0) ^{O/P} → 1 - set
- At (1,1) It goes to Invalid state.

JK flip flop

→ 75% SR flip flop

→ JK flip flop solves the

(1,1) situation of SR flip flop



Case 1

$Q_n = 1$ $Q_{n+1} = 0$

Case 2

$Q_n = 0$

$Q_{n+1} = 0$

{

J	K	Q_{n+1}
0	0	Hold
0	1	0 Reset
1	0	1 Set
1	1	$\overline{Q_n}$ toggle

Exp

In this JK flip flop It solves
(1,1) situation of SR flip flop

called toggle

→ Here we have 2 cases

$$Q_n = 1$$

$$Q_n = 0$$

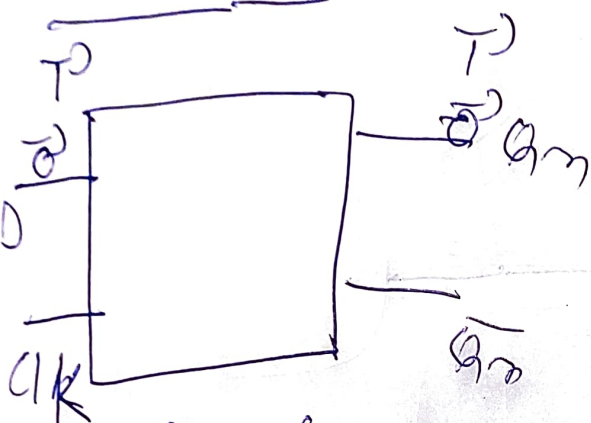
which turns $Q_{n+1} = 0$

$Q_{n+1} = 1$ called toggle

D flip flop

→ Transparent latch of flip flop

Block diag



D	Q _{n+1}
0	0
1	1

DIP x (Input = output)

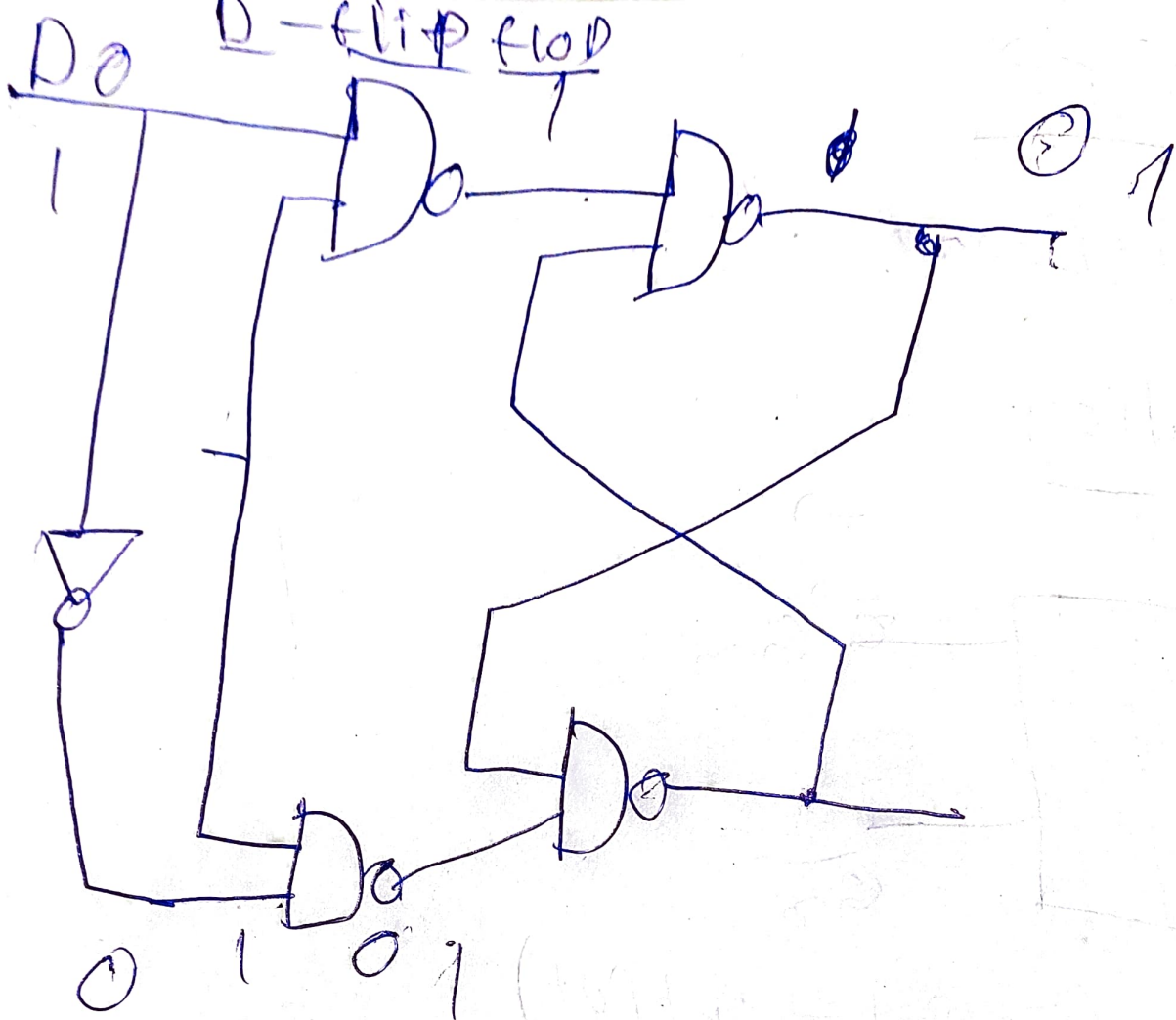
D	Q _n	Q _{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Characteristic T/b


$$Q_{n+1} = Q_n + D$$

excitation T/b

Q _n	Q _{n+1}	P
0	0	0
0	1	1
1	0	1
1	1	1



→ In D flip flop what
I/P is given same output
will come


 भारत सरकार, शिक्षा विभाग
 भारत सरकार, शिक्षा विभाग
 इन इलाकों में बिजली बंद रही

A hand-drawn schematic diagram of a square block. On the left side, there are four horizontal lines representing inputs, labeled from top to bottom as T , 1 , 0012 , and 1 . On the right side, there are two horizontal lines representing outputs, labeled from top to bottom as Q and \bar{Q} .

T	Q_{n+1}	
0	Q_n (Present O/P)	
1	$\overline{Q_n}$	Q

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$$Q_{n+1} = T + Q_n$$

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Exp

→ By its name

It converts into

Toggle