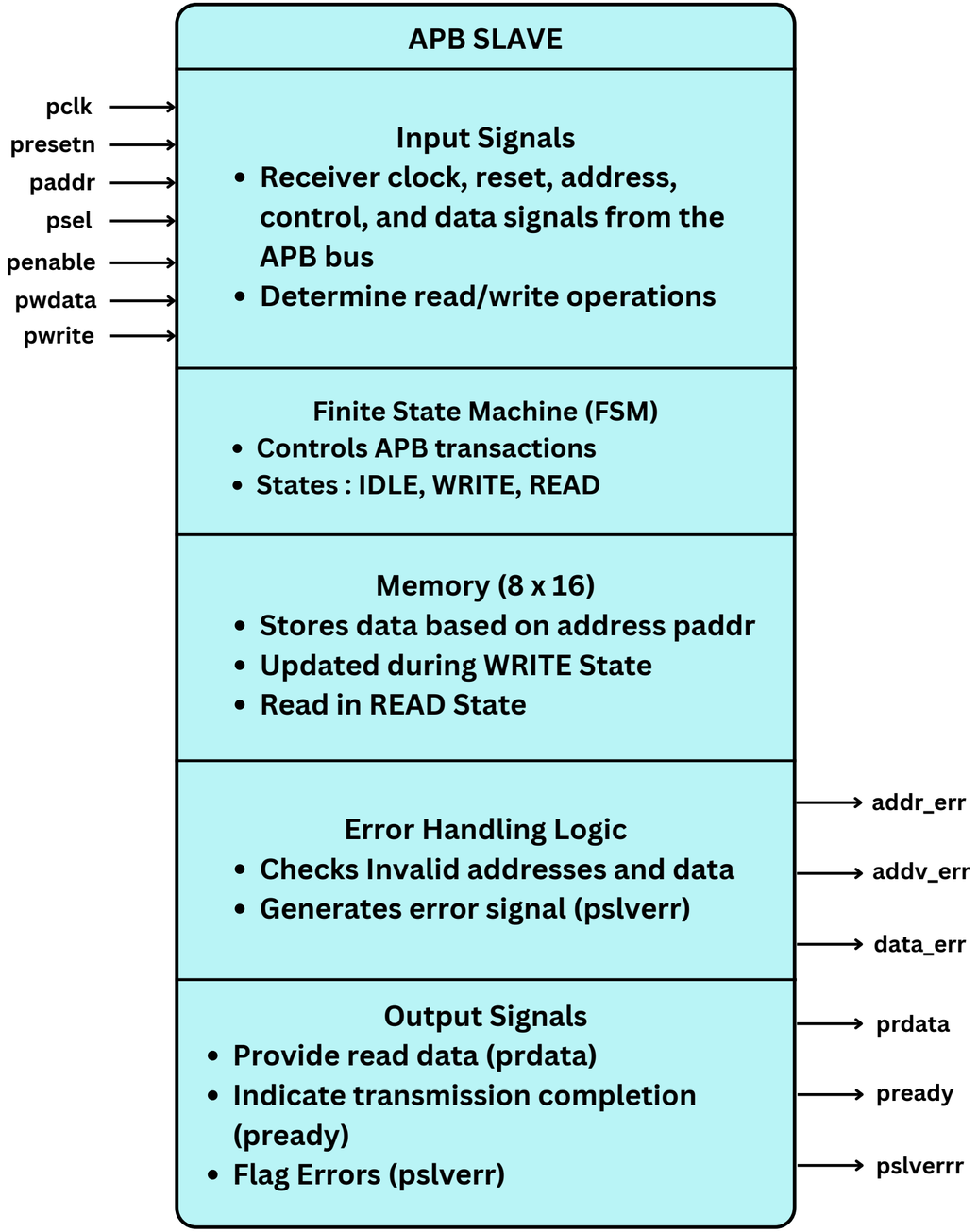
APB SLAVE
pclk
presetn
paddr
psel
penable
pwdata
pwrite
Input Signals
Receiver clock, reset, address, control, and data signals from the APB bus
Determine read/write operations
Finite State Machine (FSM)
Controls APB transactions
States : IDLE, WRITE, READ
Memory (8 x 16)
Stores data based on address paddr
Updated during WRITE State
Read in READ State
Error Handling Logic
Checks Invalid addresses and data
Generates error signal (pslverr)
addr_err
addv_err
data_err
Output Signals
Provide read data (prdata)
Indicate transmission completion (pready)
Flag Errors (pslverr)
prdata
pready
pslverrr