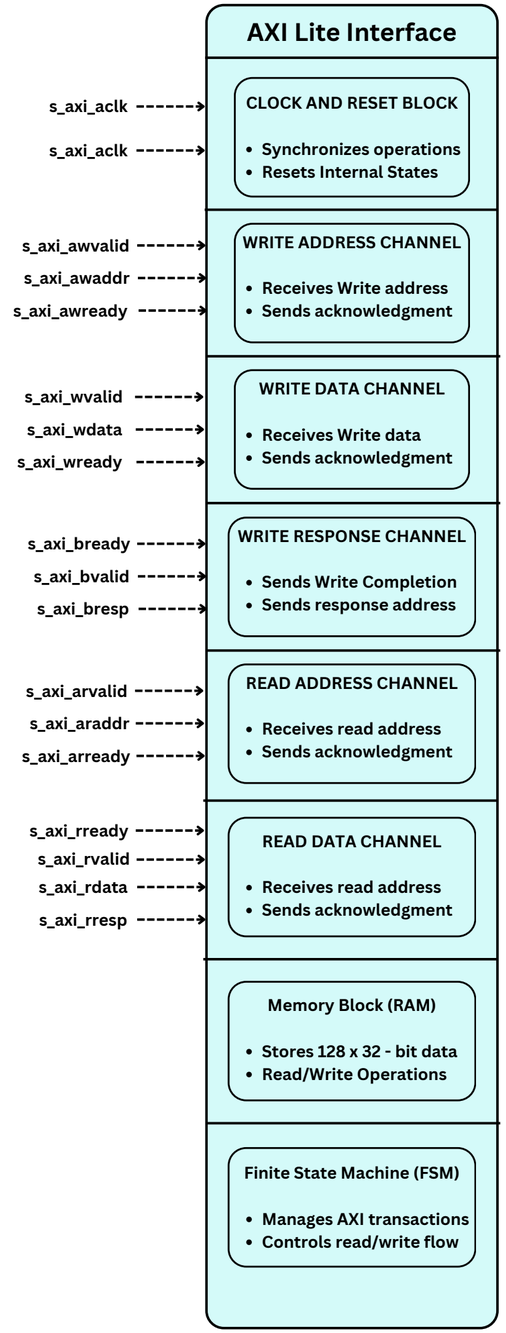
AXI Lite Interface
s_axi_aclk
s_axi_aclk
CLOCK AND RESET BLOCK
Synchronizes operations
Resets Internal States
s_axi_awvalid
s_axi_awaddr
s_axi_awready
WRITE ADDRESS CHANNEL
Receives Write address
Sends acknowledgment
s_axi_wvalid
s_axi_wdata
s_axi_wready
WRITE DATA CHANNEL
Receives Write data
Sends acknowledgment
s_axi_bready
s_axi_bvalid
s_axi_bresp
WRITE RESPONSE CHANNEL
Sends Write Completion
Sends response address
s_axi_arvalid
s_axi_araddr
s_axi_arready
READ ADDRESS CHANNEL
Receives read address
Sends acknowledgment
s_axi_rready
s_axi_rvalid
s_axi_rdata
s_axi_rresp
READ DATA CHANNEL
Receives read address
Sends acknowledgment
Memory Block (RAM)
Stores 128 x 32 - bit data
Read/Write Operations
Finite State Machine (FSM)
Manages AXI transactions
Controls read/write flow