

## #DTE Practical #

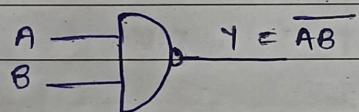
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- (1) Test the functionality of specified logic gates using breadboard (IC 7404, 7408, 7432)
- (a) Voltage at logic level 0 :- 0V
- Voltage at logic level 1 :- 5V
- (b) NAND Gate (7400)

Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Symbol :-

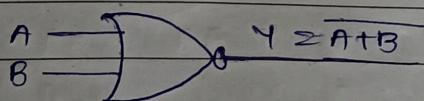


NOR Gate (IC - 7402)

Truth table :-

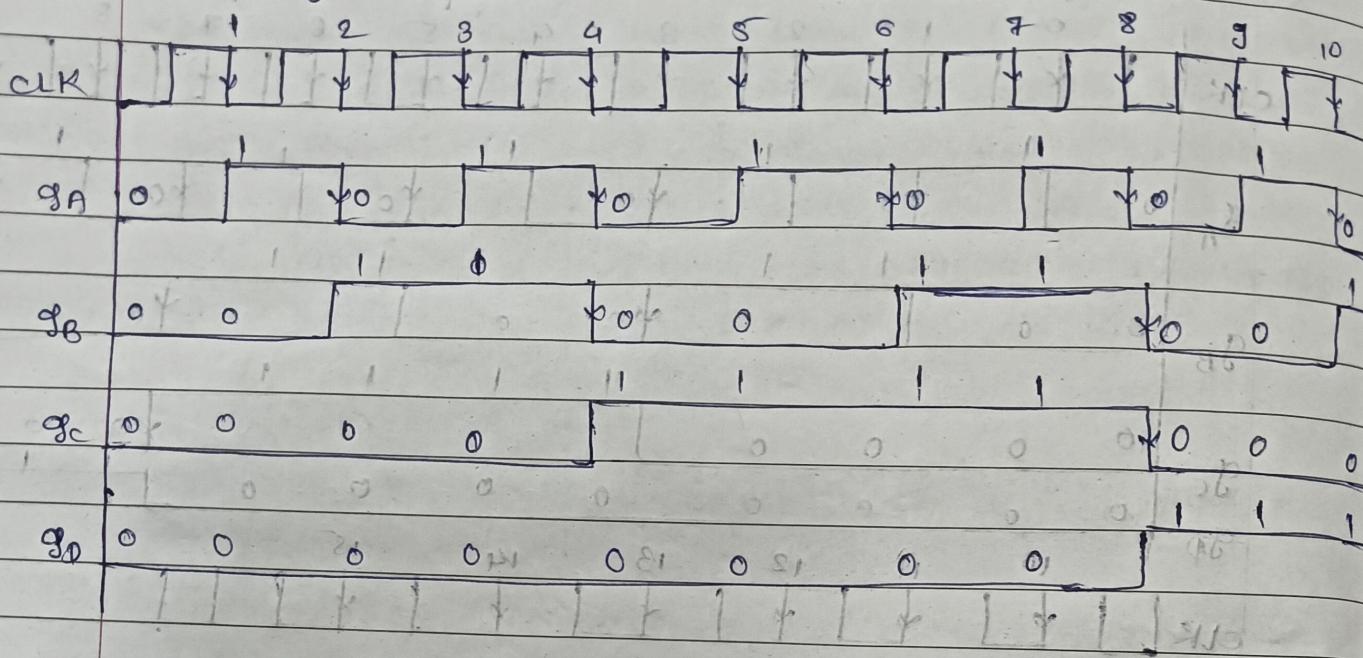
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Symbol :-



13. Implement decade counter using digital ICs.

(a) Timing diagram of decade counter.



(b) MOD-5 counter.

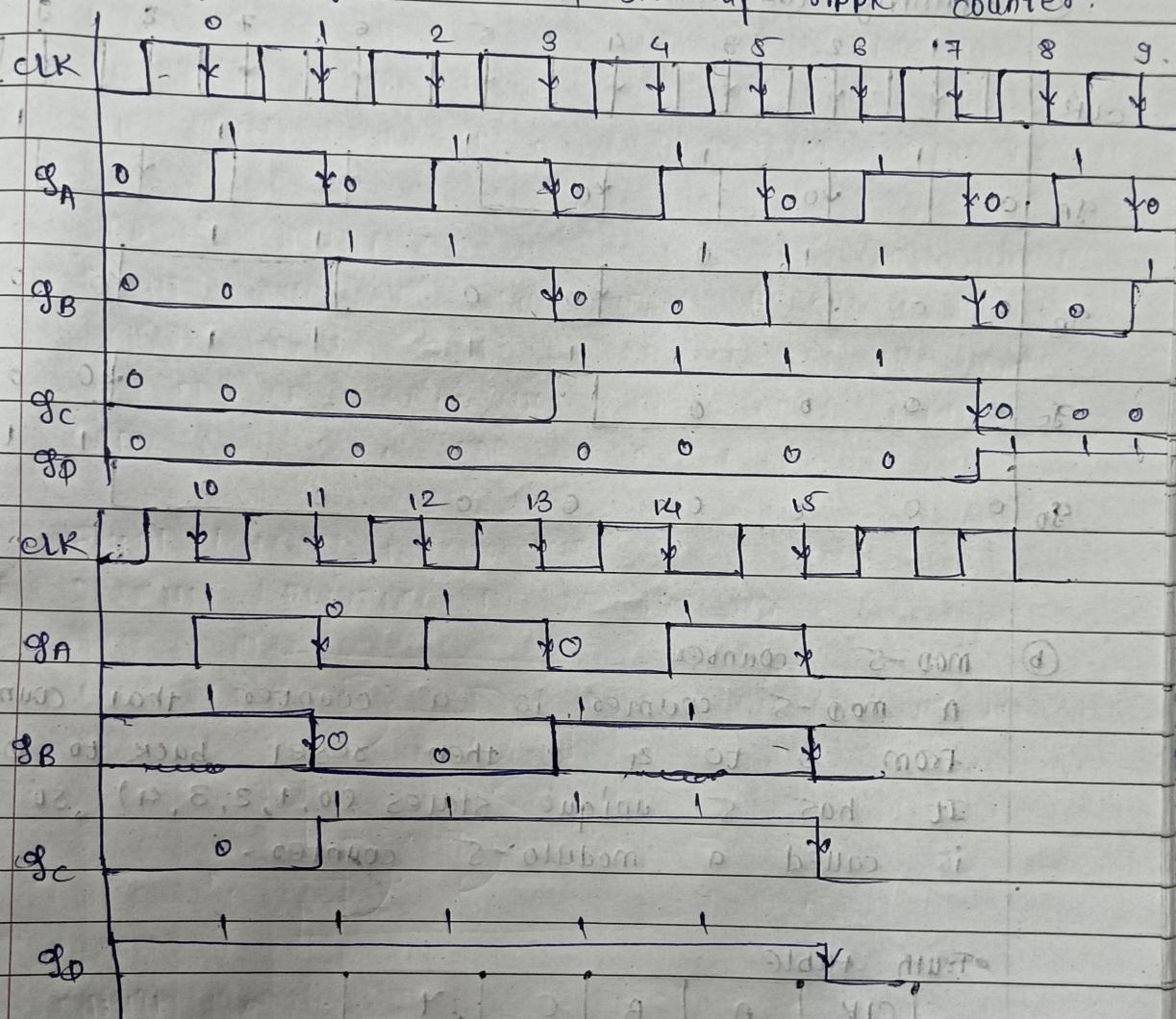
A MOD-5 counter is a counter that counts from 0 to 4 and then reset back to 0. It has 5 unique states (0, 1, 2, 3, 4), so it is called a modulo-5 counter.

Truth table

CLK	A	B	C	D	
0	0	0	0	1	2
1	0	0	1		
2	0	1	0		- valid states
3	0	1	1		
4	1	0	1		
5	1	0	0	0	2
6	1	0	1	0	
7	1	1	0	0	- invalid states

Date : \_\_\_\_\_  
Page : \_\_\_\_\_

- (12) Implement Ripple counter using digital IC  
(a) Timing diagram for 4-bit up ripple counter.



- ⑥ Application of counter

  - ⑦ In digital clock.
  - ⑧ In the frequency counters.
  - ⑨ In time measurement.
  - ⑩ In digital voltmeters.
  - ⑪ In the counter type A to D converter.
  - ⑫ In the digital triangular wave generator.
  - ⑬ In the frequency divider circuit.

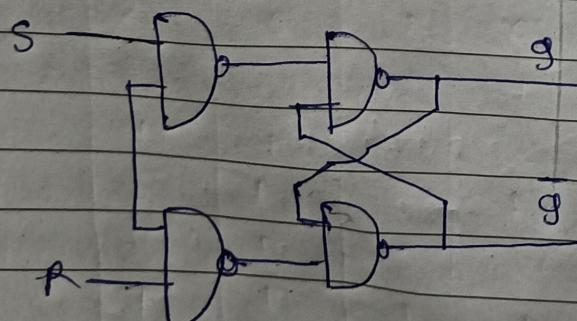
- (a) Draw back of RS flip-flop.
- RS flip-flop has the following drawbacks:
- Invalid condition:** When both the Set(S) & Reset(R) inputs are High simultaneously ( $S=1, R=1$ ) then the outputs  $Q$  &  $\bar{Q}$  become intermediate. This is because both outputs are forced to be 1 at the same time, which violates their fundamental property of flip-flop where one output is the complement of the other.

- (b) Construct & test functionality of D flip-flop & T flip-flop.

(a) Race-around condition

The race-around condition occurred in a JK-flip flop when both inputs J & K are High ( $J=1, K=1$ ) & the flip-flop is triggered by a clock signal that remains high for an extended period. During this time, the output toggles (or race) continuously between 1 & 0 as long as the clock signal is high.

- (b) SR flip flop
- circuit diagram



Truth table

S	R	Q <sub>n+1</sub>
0	0	Q <sub>n</sub>
0	1	0
1	0	1
1	1	invalid

Modes of operation	Up or down	Serial or parallel
Types	Up, down, up/down counter	SISO, PIPD, SIPO, PIPO
Applications	Digital-clock, frequency and time	Data storage, ring counter as a delay

Q. 14 Explain the operation of Johnson's counter.

Date: \_\_\_\_\_  
Page: \_\_\_\_\_

Q. Build / Test functionality of DEMUX 74155/74154.

(a) Function of pin 12, 3 & 5 of IC 74154.

• Pin 2 (Y12) : This is the active-low output line 12.

• Pin 3 (Y11) : This is the active-low output line 11.

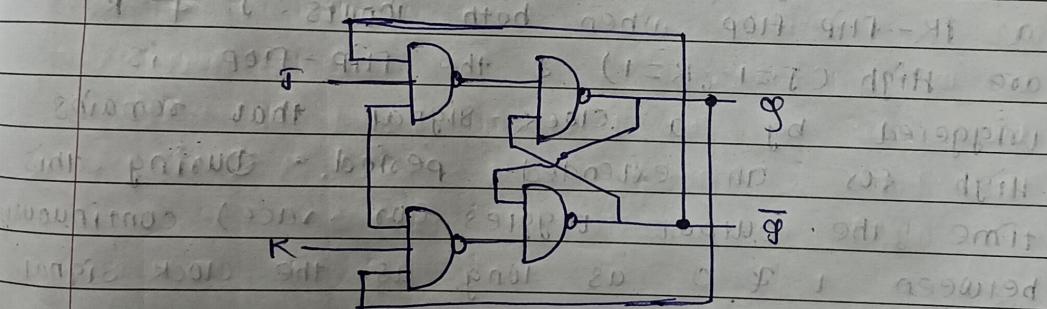
• Pin 5 (Y10) : This is the active-low output line 10.

(b) MUX : Multiplexer is a type of combinational circuit with 'N' data inputs & 1 output & 2 select inputs that select one of the input dependent on combination of select input.

Suppose if  $S_2 S_1 S_0 = 010$  then  $Y \neq D_2$ .

(c) Build / test functionality of DRS flip-flop.

(d) Circuit diagram of JK flip flop.



• Truth table

J	K	Q <sub>n+1</sub>
0	0	Q <sub>n</sub>
0	1	0
1	0	1
1	1	Q <sub>n</sub>

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### (b) Half Subtractor

• Truth table

A	B	DIFF	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

• K-map for DIFF.

A	B	0	1
0	0	0	1
1	0	1	0

$$Y = \overline{AB} + \overline{A}\overline{B}$$

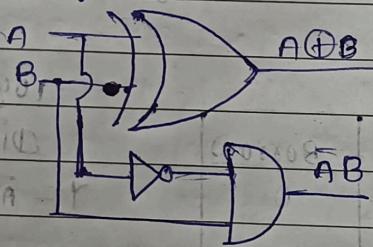
$$Y = A \oplus B$$

• K-map for borrow.

A	B	0	1
0	0	0	1
1	0	0	0

$$Y = \overline{AB}$$

• logic diagram:



Q8. Build or test functionality of MUX4151.

(a) function of pin 5 & 6 & 7 of IC74151.

• Pin 5 (D5) : This is the input for data line 5.

• Pin 6 (D6) : It is one of the 8 data inputs (D0 to D7) that the MUX selects from.

• Pin 7 (D7) : This is input for data line 6.

• Pin 7 (D7) : This is input for data line 7.

(b) DEMUX : Demultiplexer is a type of combinational circuit in which it has 1 data input 'N' outputs & m select lines. That select one of the output from ~~eight~~, output depending on combination of select inputs.

bits we have to use a group of flip flops. Such a group of flip flop is known as

Q. 12 Draw the circuit for mod-12 counter. Explain the same with neat waveforms.

Date : \_\_\_\_\_  
Page : \_\_\_\_\_

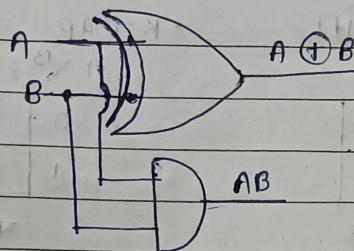
• K-map for sum

A	B	0	1
0	0	0	1
1	1	1	0

$$Y = A\bar{B} + \bar{A}B$$

$$\therefore Y = A \oplus B$$

• Diagram :-



• K-map for carry

A	B	0	1
0	0	0	0
1	1	0	1

$$Y = AB$$

Q7. Design half subtractor using boolean expression.

(a) full subtractor

• Truth Table

A	B	C	Diff.	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	1

• logic expr for

Diff :-

$$Y = \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C}$$

$$+ AB\bar{C}$$

$$+ A\bar{B}C$$

$$+ A\bar{B}\bar{C}$$

$$+ A\bar{B}C$$

Q6. Design full adder using boolean expression.

(a) Full Adder.

• Truth table :-

A	B	Cin	sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

• logic expr for sum :-

$$Y = \overline{ABC} + \overline{AB}\overline{C} + \overline{A}\overline{BC}$$

$$+ ABC$$

$$\therefore Y = A \oplus B \oplus C$$

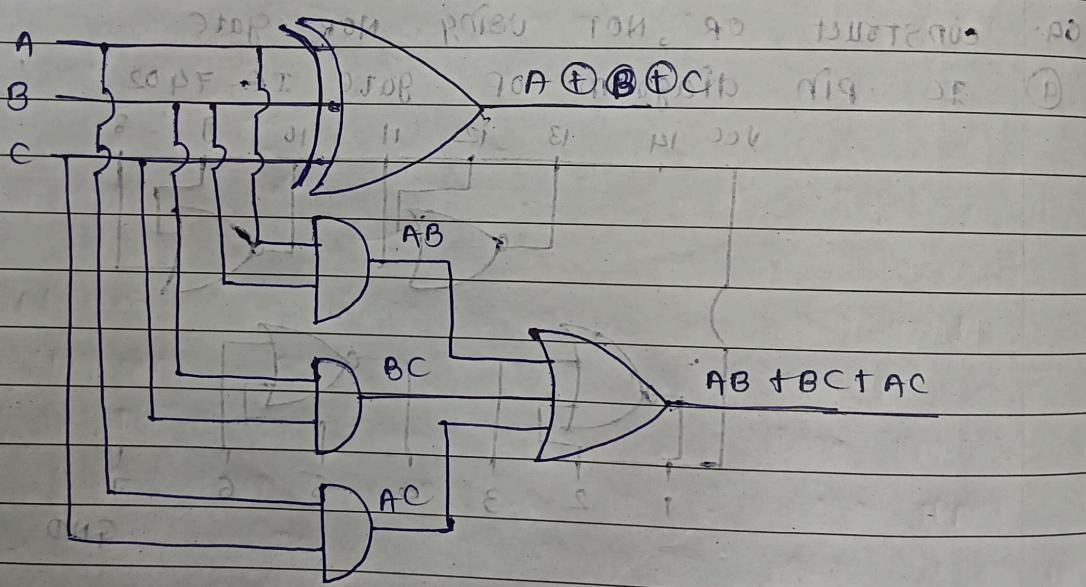
• logic expr for carry :-

$$Y = \overline{ABC} + \overline{AB}\overline{C} + \overline{A}\overline{BC}$$

$$+ ABC$$

$$\therefore Y = AB + BC + AC$$

• Diagram :-



(b) Half adder.

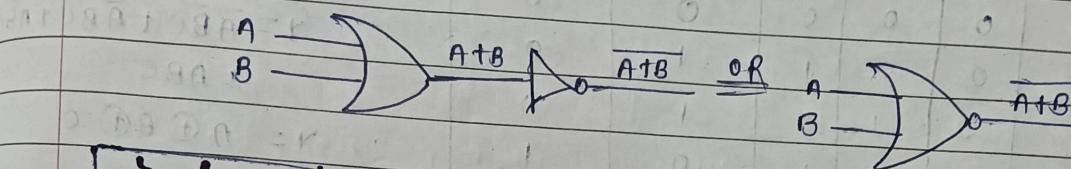
• Truth table :-

A	B	sum	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Theorem 2°  $\overline{A+B} = \overline{A} \cdot \overline{B}$

This theorem states that the sum of complement of two input is equal to product of two input with compliment of each input.

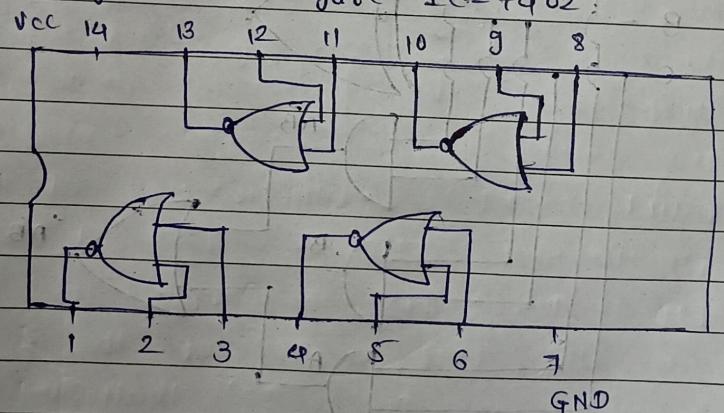
LHS :



A	B	$A+B$	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$	RHS :-
0	0	0	1	1	1	0	$\overline{A} \cdot \overline{B}$
0	1	1	0	1	0	0	$\overline{A} \cdot \overline{B}$
1	0	1	0	0	1	0	$\overline{A} \cdot \overline{B}$
1	1	1	0	0	0	0	$\overline{A} \cdot \overline{B}$

Q9. construct OR, NOT using NOR gate.

(a) IC pin diagram of gate IC-7402.



(b) In question (a) #2.

(c) Verify demorgans 1st & 2nd theorem.

IC used in 1st theorem :- IC-7400

IC-7404

IC-7402

IC used in 2nd theorem :- IC-7402

IC-7404

IC-7408

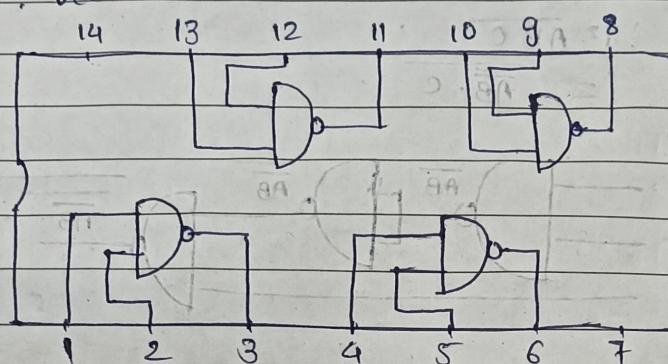
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K-map for Y.  
G<sub>C</sub> G<sub>B</sub> G<sub>A</sub>  
00 00 00  
01 01 01  
10 10 10  
11 11 11

- Invalid States

Q3. Construct AND, NOT gate using NAND gate.

(a) IC pin diagram of NAND gate (IC 7400).

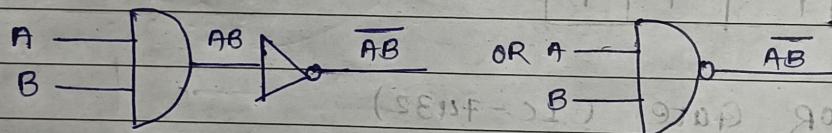


(b) DeMorgan's Theorem

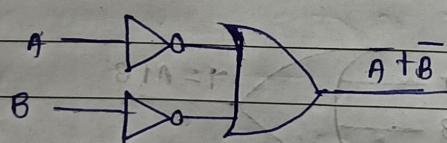
Theorem 1:  $\overline{AB} = \overline{A} + \overline{B}$  (NAND  $\equiv$  Bubbled OR).

This theorem states that the product of complement of two input is equal to the sum of two input with inverted present.

LHS :-



RHS :-



A	B	AB	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{\overline{A}} + \overline{\overline{B}}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

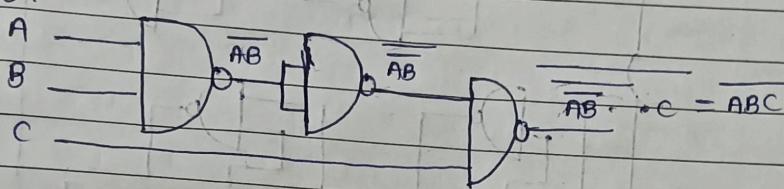
		Such a group of flip flop is known as register.
Modes of operation	Up or down	Serial or parallel
Types	Up, down, up/down counter	SISO, PIPD, SIPO, PIPO Data storage, ring

- Q. 13 Explain the operation of a ring counter.  
Q. 14 Explain the operation of Johnson's counter.

Date: \_\_\_\_\_  
Page: \_\_\_\_\_

02. Test the functionality of NAND & NOR logic Gates.
- (a) 3 input NAND Gate using 2-input NAND Gate.
- output Eqn of 3-input NAND Gate is  $Y = \overline{ABC}$

• Gates:

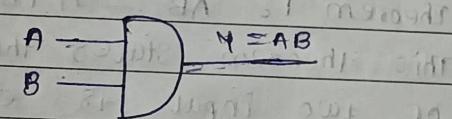


- (b) AND Gate (IC-7408)

Truth table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

• Symbol

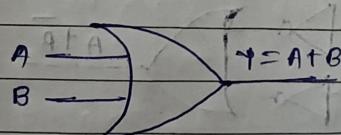


- OR Gate (IC-7432)

Truth table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

• Symbol

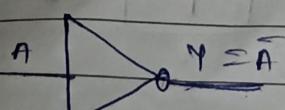


- NOT Gate (IC-7404)

Truth table

A	Y
0	1
1	0

• Symbol



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fo

K-map

- Invalid

GENO.:

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counter.

8)

require