MAR-21-210033

B. Tech. EXAMINATION, March 2021

Semester III (CBCS)

DIGITAL ELECTRONICS (ECE, EE, EEE, CSE, IT)

EC-302

www.zoomy.in

Time : 3 Hours   Maximum Marks : 60

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt *Five* questions in all, selecting *one* question from each Sections A, B, C and D. Q. No. 9 is compulsory.

Section A

1. (a) Convert the following no. to decimal :   2.5

    (i) $(1001001.011)_2$

    (ii) $(121.21)_3$

    (iii) $(1032.2)_4$

(b) Convert the gray code 110101 to binary form. **2.5**

(c) Write a short note on codes for error detection and correction. **2.5**

(d) What do you understand by Hamming code ? **2.5**

2. (a) Explain tristate logic gates and Schmitt gates. **2.5**

(b) Describe totem-pole output stage. **2.5**

(c) Perform the following arithmetic operations **2.5**
   (i) Add 96 and 56 BCD numbers
   (ii) Subtract 748 from 983 BCD number.

(d) Explain Fan in and Fan out of logic gates. **2.5**

Section B

3. (a) Draw a logic circuit to realize the function :

$$\gamma = A \cdot B \cdot C + \overline{A} \cdot \overline{B} \cdot \overline{C} + B$$

Simplify the expression and draw and logic for the simplified expression. **5**

(b) Minimize the following function by Tabular method :

$$F(A, B, C, D) = \Sigma_m (0, 2, 3, 6, 7, 8, 9, 10, 13).$$
   5

4. (a) Explain the priority encoder. **5**

(b) Draw the circuit of four bit amplitude comparator and explain its operation. **5**

Section C

5. (a) Explain the working of TTL. What are the sub-families of TTL logic family ? **5**

(b) Write a short note on Demultiplexer tree. **5**

6. Describe flip-flop timing parameters and its application. **10**

Section D

7. (a) Draw the circuit of a serial-in-parallel-out shift register and explain its working. **5**

(b) Design a mod 7 binary counter. Draw its state diagram and circuit. **5**

8. (a) Differentiate between PAL and PLA. **5**

(b) In a 3 bit addressable ROM, the following functions are required :

$$h_0 = \Sigma\ 0, 2, 5, 6$$

$$h_1 = \Sigma\ 0, 2, 4, 6, 7$$

$$h_2 = \Sigma\ 0, 2, 4, 7$$

$$h_3 = \Sigma\ 1, 2, 3, 5, 7.$$
   5

(Compulsory Question)

9. (i) What does volatile memory ?

   (ii) Compare ECL with Shottky TTL.

   (iii) What are shift register operation ?

   (iv) What is mod-m binary (ripple) counter ?

   (v) How can a sign integer be represent in binary system ?

   (vi) Discuss Ex-OR gate.

   (vii) What do you mean by universal logic gates ?

   (viii) What is meant by code converter circuits ?

   (ix) Define state diagram.

   (x) Define Fan in, Noise margin, Fan-out. 2×10=20