AN62338 – PCB Guidelines for AC-DC Controller as a LED Driver

AN62338

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Application Note Abstract

AN62338 provides information about printed circuit board (PCB) design for LED power drivers using off-line AC/DC controller (CY8CLEDAC0x). It illustrates component placement, signal routing, power routing, power paths, and thermal dissipation. These guidelines can be implemented for any LED driver.

Each section includes information about specific requirements during the design process.

Introduction

A clear understanding of the circuit is necessary for a PCB designer to create successful designs. Each circuit and design has its own critical parameters. A power-LED driver circuit is no exception, as there are significant levels of power flowing and switching throughout the design.

To understand a power-LED driver circuit, consider a switching voltage regulator. The difference between a switching voltage regulator and a LED driver is that a switching voltage regulator controls an output voltage, while a power-LED driver controls an output current.

If you have designed a switching voltage regulator, designing a power-LED driver using CY8CLEDAC0x will be an easy process, because many of the guidelines for a successful design are identical. Even if you are new to power electronics design, the AC0x (CY8CLEDAC01 or CY8CLEDAC02) simplifies most of the design with its high integration of power control.

This application note starts with discussing points of PCB design and the effects of each. At the end of this application note is a PCB layout example for CY8CLEDAC02 in a PAR30 form factor.

If you want to quickly get into the AC0x PCB layout, directly go to the AC02 specifics in Example PCB Layout starting on page 9. However, reviewing of PCB Guidelines in the following section refreshes your knowledge on PCB design.

Guidelines

Following are the guidelines for PCB layout using the CY8CLEDAC0x:

- Evaluate power loops
- Coupling between nets
- Place key components close to each other
- Optimize trace length and routing
- Use copper sized for power
- Use copper pours and copper thieving
- Via usage
- Power guidelines
- Voltage and power loss
- Multiple via (if necessary) for power
- Evaluate current loops
- Consider return (ground) current
- Thermal dissipation
- UL safety
- Layer count and usage
- Assemble surface mount versus through hole

PCB Guidelines

The guidelines for LED PCBs are similar to those for analog PCBs. They cover copper weight and trace size, copper pours, via use, and trace length.

Power Loops

To create an off-line AC/DC LED driver, first analyze the schematic for power loops. For an AC01 (CY8CLEDAC01) design, evaluate Flyback, Auxiliary, and Output loops. For an AC02 (CY8CLEDAC02) design, along with three loops, evaluate Boost loop.

The basic Flyback loop encloses the bulk capacitor, transformer primary winding, switching field effect transistor (FET), and current-sense resistors.

The basic Auxiliary loop encloses the Auxiliary winding of the transformer, controller IC, and its VCC capacitors.

The basic Output loop encloses the output rectification diode, output storage capacitor, LED load, and output winding of the transformer.

The Boost loop in an AC02 design encloses the Boost capacitor, Boost inductor, Boost FET, and dimmer load resistors. After the loops are identified, the components can be placed on a PCB design.

Coupling

Coupling or crosstalk between nets can cause system accuracy and performance issues. The reason for crosstalk is placing nets in close proximity to each other when one or both of the nets have large dV/dt or dI/dt signals. The base correction for crosstalk is separation of the two nets that are coupling. The separation reduces or minimizes the coupling to a point where the crosstalk is not affecting the system operation or performance.

Components Guidelines

This section discusses placement of key components, trace length, test point placement, and test point placement for ground.

Place Key Components Close to Each Other

This is a major step in PCB design for an AC0x LED driver board. After the power loops are identified, the parts within each loop needs to be placed in such a way that the copper interconnecting the components is short. The proper placement is to have the output (sourcing) pin of a component physically next to the input (load) pin of the receiving component. The Flyback, Auxiliary, Output, and Boost loops mentioned in the Power Loops section are interconnected with either Ground or High Voltage. This interconnection adds complexity to component placement as the current flows and switches within each loop that can add EMI issues.

Minimize Trace Length

System performance and reliability always improve when interconnecting traces are short. A long trace has power loss associated with voltage drop directly related to the trace length. When power is lost in the trace, system power efficiency is lower. Longer traces create additional traces, require additional vias, reduce the area for component placement, and increase the system cost because a larger PCB is required.

Prioritize Trace Routing

Minimizing all traces is often not possible, as placement of key components require some traces to be longer than desired. In this case, it is necessary to prioritize or rank the importance of trace routing. Table 1 shows a prioritization of nets. The table is an example; evaluate your design for importance of each net.

Table 1. Net Usage Prioritized

Priority	Net Usage
1	Analog (AC)
2	Analog (static/DC)
3	Power (high current)
4	Power control (high current switching)
5	Digital signals (high speed - MHz)
6	Digital signals (low speed - kHz)
7	Digital signals (static/DC)

Use Copper Sized for Power

Copper weight is one of the design parameters, where the choice is between options (½-ounce or 1-ounce), based on personal preference, cost, or company requirements. Trace width is another design parameter that is accepted at default parameter or a trace width that works globally for system components.

In power design, using a default copper weight or global trace widths can potentially have system failures because of open traces (traces can fail at high current due to excessive temperatures that melts copper).

There are several resources available on the internet to calculate trace width based on copper weight, current capacity, and temperature rise. Use the following equations for internal and external traces. (Following equations are from Wikibooks: trace current capacity)

Trace Cross-section Area

$$Trace_{cross-section} = h * w \quad \text{Equation 1}$$

External Trace Power

$$I_{max} = 0.0647 * \Delta T^{0.428} * (h * w)^{0.673} \quad \text{Equation 2}$$

Internal Trace Power

$$I_{max} = 0.0150 * \Delta T^{0.545} * (h * w)^{0.735} \quad \text{Equation 3}$$

In the equations:

I_{max} is the maximum current (in Amps) the trace can handle.

ΔT is the increase in trace temperature due to current flow. It is recommended to limit the temperature increase to between 10 ºC and 20 ºC.

h is the height of the copper. ½-ounce copper is 0.675 mil inches; 1-ounce copper is 1.35 mil inches; 2-ounce copper is 2.7 mil inches.

w is the width in mil of the copper trace.

An example for trace width calculation is:

I_{max} = 1A, ΔT = 20 ° C, copper weight = 2 ounce (2.7 mil inches), external layer.

Using Equation 2:

$$I_{max} = 0.0647 * \Delta T^{0.428} * (h * w)^{0.673}$$
$$1 = 0.0647 * 20^{0.428} * (2.7 * w)^{0.673}$$
$$1 = 0.0647 * 3.605 * (2.7 * w)^{0.673}$$
$$1 = 0.233 * (2.7 * w)^{0.673}$$
$$4.288 = (2.7 * w)^{0.673}$$
$$8.699 = 2.7 * w$$
$$3.22 = w(in\_mils)$$

Copper Pour

When determining the copper size for a power signal, the required trace width is typically 0.050 inches or more. Trace widths of this size are very difficult to route between and around components. The solution is to use copper pours for these electrical connections.

A copper pour is a polygon placed on a signal layer. The polygon size covers an area that allows connections of all pins for a specific signal (typically a power or ground signal that connects many components).

There may be one or more copper pours, on the same or different signal layers in a design. Each copper pour provides any one or a combination of the following benefits.

- Reduces power loss of interconnects
- Improves thermal dissipation
- Provides electro magnetic interference (EMI) shielding
- Improves PCB fabrication (copper thieving)

Copper Thieving

Copper thieving is a term used by PCB fabrication companies. When a PCB has copper thieving applied, small chunks of copper remain on the board in the large areas where no copper was originally present. The process has a dual improvement for the fabrication company. During the plating process, the copper plating is more even throughout the PCB and the etchant (copper removal chemical) lasts longer, as creation of the PCB removes less copper.

Copper thieving is beneficial as the PCB fabrication company has less waste and more profit, while you get a higher quality and less expensive board.

However, when you allow a PCB fabrication company to add copper thieving, you can never be sure if the design performs according to your requirements. Therefore, the designer should solve the copper thieving question and maintain design control by adding copper pours to the layout before releasing for PCB fabrication.

To prevent the copper pour from acting as an antenna, connect each end of the copper pour to a power or ground net.

Via Usage

Avoid Using Vias

Vias are often one of design's capabilities that engineers typically overuse or use incorrectly when designing a power electronics board such as a power-LED driver system.

We tend to think of vias as having zero effect upon a design. This is far from reality, as vias have capacitance, inductance, and resistance. Capacitance causes an edge rate to decrease; inductance delays a signal; and resistance causes a signal to decrease in amplitude.

Placing vias reduce the space available for traces. When this space is reduced, a signal may need a circuitous and longer route leading to system noise and signal degradation.

Placing vias reduces the area through which ground currents can flow. Ground currents flow using the path of least resistance and placing a via in the direct path causes the ground current path to be indirect, thus adding unnecessary noise to the system ground.

If a via is used, ensure that your system performance is not affected; additional effort during placement and routing can avoid potential issues.

Placing Power Vias for Decoupling

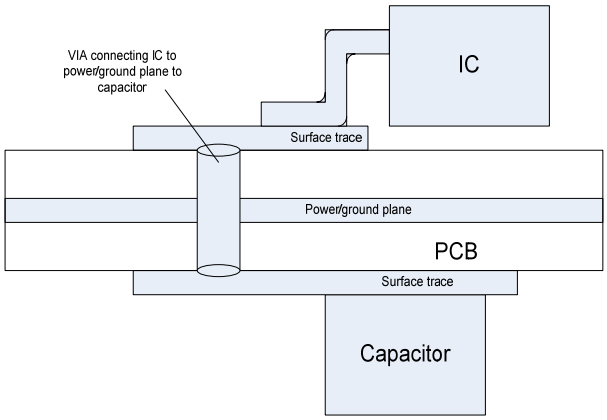
Although avoiding the use of vias is difficult when connecting from a power/ground plane to surface-mount components, let us evaluate their effectiveness for decoupling.

A typical example of placing vias is connecting a power plane to a decoupling capacitor and power pin of an IC. There are a minimum of three cases (and many more derivatives) for placing vias connecting a decoupling capacitor and an IC's power to a power/ground plane.

- The capacitor and IC are on opposite sides of the power/ground plane as shown in Figure 1.

  This implementation is almost the same as using no capacitor. As the power/ground plane is between the IC (current load) and the capacitor, the power/ground plane sources the majority of power directly. The capacitor is now acting as bulk power storage as opposed to the noise filter needed. This implementation is not the correct method to connect decoupling capacitors.

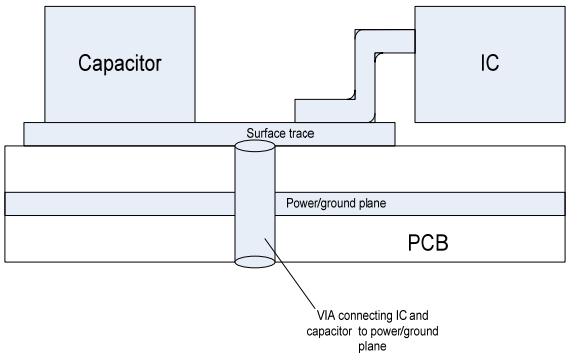
Figure 1. Capacitor, IC, and Via Orientation 1



- Capacitor and IC on same side of power/ground plane, with via placed between them for connection to power/ground plane as shown in Figure 2 on page 2.

  This implementation is slightly better than not using a capacitor. As the power/ground plane via connection is between the IC (current load) and the capacitor, the power/ground plane sources the power in parallel with the capacitor. In this orientation, the capacitor accomplishes only a partial functionality.

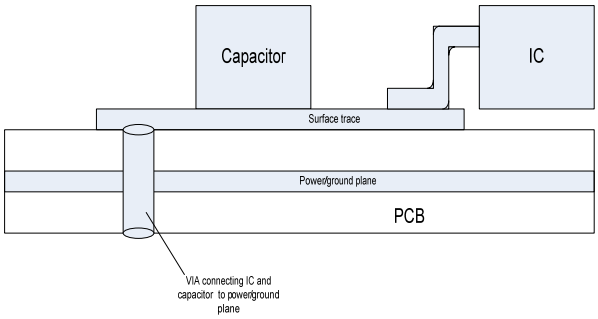
  Figure 2. Capacitor, IC, and VIA orientation 2



- Capacitor and IC on same side of power/ground plane, with the capacitor placed between the IC and the via connecting to the power/ground plane as shown in Figure 3.

  This is the ideal implementation. As the capacitor is between the power/ground plane via and the IC (current load), the capacitor is the first source of power for the IC. This allows the capacitor to function as required. It prevents unwanted power noise from reaching the power/ground plane and affecting other system components.

Figure 3. Capacitor, IC, and VIA Orientation 3



Additional consideration during placement of decoupling capacitors on a board is when more than one decoupling capacitor is for a power pin. Place the capacitors with the smaller value closer to the pin so that it can respond to the high frequency power demands quicker than larger capacitors placed further, to handle the lower frequency power demands before the power gets into the rest of the system.

Via Size

The size of vias is another design parameter accepted at its default value. When specifying a via, smaller vias are preferred for space consideration while maintaining manufacturability.

Vias are defined for different uses as basic signal, power control, or power. Just as trace width is determined for power nets, vias also need to be defined for a specified use.

A via used for a basic signal interconnect may be small, such that its size is at the lower limits for manufacturability. A basic signal via size may be 10/15 (hole/pad size in mils) or 15/20.

A via used for power control may be slightly larger, based upon the amount of current passing through it. A power control via size may be 15/20 or 20/25.

A via used for power may be sized even larger depending upon the level of current that it passes. A power via size may be 15/20, 20/25, 25/30, or larger.

To calculate via current yourself, use the following equations:

Via Circumference (mils)

$$C_V = (T_V + D_V) * Pi \qquad \text{Equation 4}$$

C_V is Circumference of via.

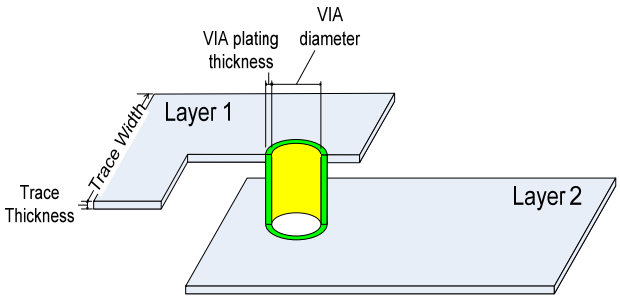
T_V is Via plating thickness.

D_V is Via diameter after plating. This value is typically the value specified as the hole-diameter for the PCB fabrication. The PCB fabricator overdrills the hole and then plates back to the specified hole-diameter.

Circumference is calculated from the center of plating on one side of the via directly across to the center of plating on the opposite side of the via. (½ via plating + via diameter + ½ via plating) = (via plating + via diameter)

Note: If the via diameter is one-third the trace width, its circumference is approximately the trace width.

Figure 4. Cutaway View of Via



With the via circumference calculated, use that value as w (the width) and use the via plating thickness as h (the height) to determine the via's cross section

Via Cross-section Area

$$VIA_{cross-section} = h * w \text{ (mils)} \qquad \text{Equation 5}$$

h is Via plating thickness

w is Via circumference

For a via to handle current equal to the trace it is used in, the via cross-section must be equal to or greater than the trace's cross-section it is used in.

An example for via calculation is:

Via diameter = 15 mil, Plating thickness = 1 mil

Using Equation 4 to calculate via circumference (in mils)

$$Cv = (Tv + Dv) * Pi$$
$$Cv = (1 + 15) * Pi$$
$$Cv = 16 * Pi$$
$$Cv = 50.27$$

Using Equation 5 to calculate via cross-section (sq. mils)

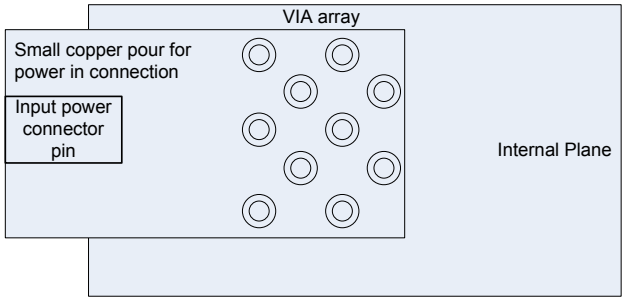
$$VIAcross-section = h * w$$
$$VIAcross-section = 1 * 50.27$$
$$VIAcross-section = 50.25$$

Via Quantity

We have discussed using one via at a time. However, you can use parallel vias similarly for any basic resistor, capacitor, or inductor.

Figure 5 is an example where parallel vias are used to connect a surface mount connector to a power/ground plane. Using a single via to pass large current damages it quickly due to excessive heat. It also increases the noise on the power/ground plane. Placing several vias in parallel provides many paths for current flow between the connector and power plane, increases heat dissipation and decreases noise.

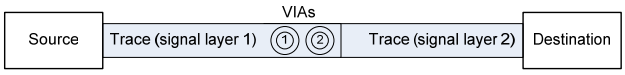
Figure 5. Via Array for Power or Ground Plane Connection



Another, not-so-obvious example is using multiple vias interconnecting signal layer changes for power control nets. For example, when driving the gate of a FET, often 1-Amp or more of gate current flows during the t_{on} and t_{off} of the FET.

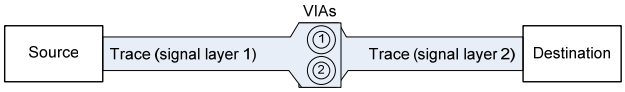
In Figure 6, an example of two vias in a power control trace shows an ineffective method of paralleling vias. The issue arises when the power passes the first via, the amount of trace width narrows due to the loss of surface copper related to the via hole. The issue occurs twice in this example, one on each layer. As the signal travels from the source, the narrowing occurs as the signal passes via1 to via2. After the signal passes through the vias, a second narrowing occurs as the signal travels from via1 past via2 to the destination.

Figure 6. Two Vias in Power Trace - Poor Implementation



In Figure 7, an example of two vias in a power control trace shows an effective method of paralleling vias. The narrowing of traces issue shown in Figure 6 is no longer present as the power passes to and from both vias equally with no restriction.

Figure 7. Two Vias in Power Trace - Good Implementation



Thermal Power Connections

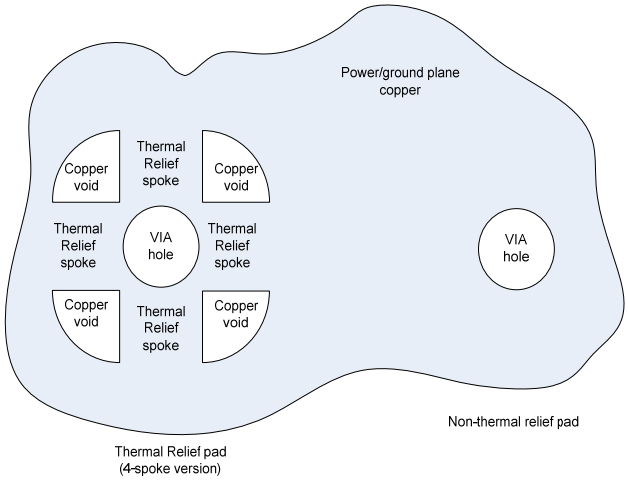
When connecting a pin to a power or ground plane, a thermal connection is often used.

In a thermal connection, the amount of heat necessary to de-solder or solder a component is much less than if the connection to the power or ground plane is solid or non-thermal relief style.

Figure 8 shows two power or ground interconnect styles, a thermal relief style and a non-thermal relief style. The thermal relief style connection has a general appearance of a wheel, where removal of small sections of the power or ground plane copper forms a small thermal isolation around the central connection hole. The remaining 'copper spokes' make the connection to the power or ground plane.

When using thermal relief connections, you must evaluate the size and quantity of spokes for power capacity just as you evaluate trace widths for power capacity.

Figure 8. Power or Ground Connection Styles



Power Guidelines

This section discusses power loss, power vias, current loops, and current flow.

Power and Voltage Loss

This section discusses trace resistance and the voltage or power loss associated with the resistance of the copper. Equation 6 is referred from the book, *High-Speed Digital Design.*

Trace Resistance (Ω/inch)

$$R = \frac{L * 0.65866 * 10^{-6}}{w * h}$$

Equation 6

R = trace resistance in ohms/inch.

L is the length in inches of the trace.

$0.65866*10^{-6}$ is resistivity of copper on a PCB.

w is the width in inches of the PCB trace.

h is the height in inches of the trace:

½-ounce copper is 0.000675 inches

1-ounce copper is 0.00135 inches

2-ounce copper is 0.0027 inches

Equation 6 is referred from the book, *High-Speed Digital Design.*

Trace Voltage Loss

$$V_{loss} = R * I$$ Equation 7

R is the resistance of the trace calculated using equation 6.

I is the current flowing through the trace.

Trace Power Loss

$$P_{loss} = V_{loss} * I$$ Equation 8

V_{loss} is the voltage loss calculated using equation 7.

I is the current flowing through the trace.An example of trace resistance, trace voltage loss, and trace power loss is:

Trace length = 2 inches, Copper weight = 2-ounces, Trace width = 10 mil. Current = 1A.

Use Equation 6 to calculate trace resistance in Ω/inch.

$$R = \frac{I * 0.65866 * 10^{-6}}{w * h}$$

$$R = \frac{2 * 0.65866 * 10^{-6}}{0.010 * 0.0027}$$

$$R = \frac{1.31732 * 10^{-6}}{27 * 10^{-6}}$$

$$R = 48.79 * 10^{-3}$$

Use Equation 7 to calculate the voltage loss in Volts.

$$V_{loss} = R * I$$

$$V_{loss} = 48.79 * 10^{-3} * 1$$

$$V_{loss} = 48.79 * 10^{-3}$$

Use Equation 8 to calculate the power loss in Watts.

$$P_{loss} = V_{loss} * I$$

$$P_{loss} = 48.79 * 10^{-3} * 1$$

$$P_{loss} = 48.79 * 10^{-3}$$

Multiple Via for Power

Use multiple vias when connecting from a surface-mount power component to a power or ground plane. Using one via to pass amps of current quickly burns out the via or has a very large voltage drop passing through it. This allows system noise to easily get into the power or ground plane. In this case, placing several vias in parallel provides many via paths for the current to flow from the power component to the power plane as shown in Figure 5 on page 5.

The following two sections walk you through calculating the current that a via can easily pass.

For a Thermal Relief Via

- Use Equation 4 to calculate via circumference
- Use Equation 5 to calculate the via cross sections.
- Use Equation 2 to calculate the maximum surface via current. Record this value for final comparison with 'Thermal via current'.
- Use Equation 1 to calculate the thermal spoke cross section.
- Multiply the thermal spoke cross section by the number of thermal spokes for that via.
- Use Equation 3 to calculate the maximum Thermal via current.
- Use the smaller value of 'surface via current' or 'Thermal via current' as the maximum via current.

For a Non Thermal Relief Via

- Use Equation 4 to calculate via circumference.
- Use Equation 5 to calculate the via cross section.
- Use Equation 2 to calculate the maximum via current.

Evaluate Current Loops

To understand ground current you need to understand how current changes with a signal.

Current flows in two paths: the path of least resistance and the path of least impedance. This does not mean that current selects one of the two paths and only flow in that path. Current constantly transitions between the two paths based upon system operation.

The path of least resistance is a straight line between two points. This is the path during DC or static operation shown in Figure 9.

The path of least impedance is the path directly below a signal during its transition. This is the path during AC or switching operation shown in Figure 9.

In Figure 9, the area between DC and AC is the transition time when current is changing paths between least resistance and least impedance. The transition time between DC and AC can be the most troublesome as there is minimal control over the return path.

Minimal control does not mean no control. Following section presents the control options and ground plane integrity.

Figure 9. Signal and Current Path

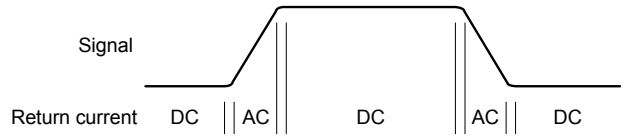
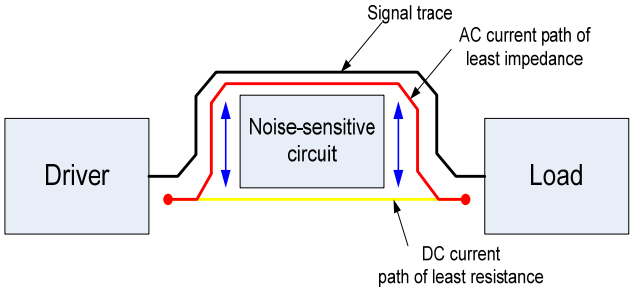


Figure 10 is an example of current flow path in a four-layer board. In the example, there are three blocks, Driver, Load, and Noise-sensitive circuit. Connecting the Driver and Load is a signal trace. Shown in the example are two other paths, an AC current path of least impedance and a DC current path of least resistance. Looking at this diagram, the current flow paths appear acceptable. What is not shown is as the signal (in Figure 9) changes state, the current passes through the noise-sensitive circuit, not once, but twice for every signal transition as shown by the transition space in Figure 9 on page 6.

Figure 10. Current Flow Path Diagram



Common (Ground) Guidelines

This section, discusses ground and ground planes.

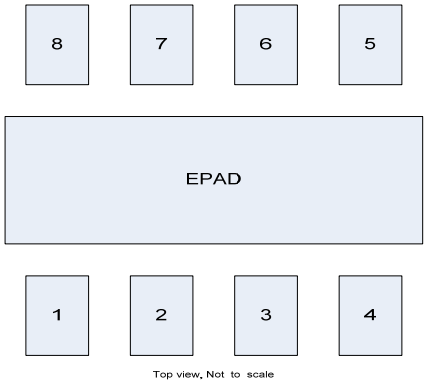
Generally, a large ground plane or copper area used for system ground is better than using copper tracks to interconnect all the ground pins. This is not saying once a ground plane is used, all system concerns about ground interconnect is solved.

When using a ground plane, it is still very necessary to evaluate the current flow between any two points. An example is a ground plane on a two layer PCB may also be used for some signals crossing other signals or components on the board. This is no better than using traces without considering the routing or current flow. When placing or embedding traces in a ground plane, the current in the plane has to flow around the embedded trace, this causes the current to flow in a longer path and cause system performance that may be efficiency or EMI issues.

Thermal Dissipation Guidelines

The electrical or thermal pad (EPAD) connection must connect to copper on the PCB for solid thermal dissipation. The fabrication of the PCB needs to specify filling these vias, if the vias are placed directly in the EPAD. The reason for filling the vias during fabrication is that during the assembly process, when the solder is reflowed for device attachment, if the vias are not filled, the solder is pulled away from the AC0x by the solder flowing into the non-filled vias. Filling the vias during the PCB fabrication process prevents the solder from flowing away and keeps a solid thermal connection between the AC0x EPAD and the PCB copper.

Figure 11. Vias Filling



The variety of power components is high and each component has its own power dissipation values. Refer to the device datasheets for recommended thermal dissipation.

Provided here are basic formulas to calculate power dissipation for key components. It is necessary to consult the datasheets for some of the parameters used during the power calculation.

FET Power dissipation = Switching + conduction power

Switching power = ½* V_{DS} * I_{AVG} * (Trise+Tfall)/(Ton+Toff)

Conduction power = I_{AVG} * I_{AVG} * R_{DS} * (duty cycle)

Diode power = $V_{FORWARD}$ * I_{AVG} *(1-duty cycle)

Inductor power = I_{AVG} * I_{AVG} * $Inductor_{DCR}$ + core loss

Sense resistor power = I_{AVG} * I_{AVG} * resistance

PCB Substrate

Normally, the PCB substrate material is FR4 epoxy-glass. An alternative is to use a metal-core PCB substrate. Metal-core PCB is useful for designs that are dense for power dissipation and requires extra metal core to remove the heat from critical components.

The AC0x does not require a metal-core PCB. An epoxy-glass material works well.

Encapsulation

Another method of improving the thermal dissipation of a system is encapsulation or potting of the final assembly. The encapsulation will significantly increase the thermal mass of the system. A larger thermal mass means more heat can dissipate before the system fails due to heat.

Additional advantage of using encapsulation is safety requirements for creepage and clearance is easier. The use of encapsulation provides a LED driver environment that is free of the typical contaminate buildup from pollution and dust in the air.

Safety

Safety requirements are based upon recommendations by Underwriters Laboratories (UL) and Comité Internationale Spécial des Perturbations Radioelectrotechnique (CISPR).

The safety requirements specify creepage and clearance standards that encompass the environment the LED driver operates in. The requirements list clearances based upon maximum voltage potential between any two adjacent device pins or traces on a PCB.

A low voltage (110 Vac) LED driver may have creepage and clearance requirements of 2.5 mm, while a high voltage (220 Vac) systems need 4.0 mm or greater. This creepage and clearance quickly increases the size of a PCB by a factor of 2 - 4. Just imagine the size of the PCB when any high voltage trace requires 4 mm clearance around it.

Layer Count and Usage

Although not required, an AC0x system can use more than two copper layers. The use of more than two layer can improve thermal, EMI, and safety of the system.

Thermal is improved by having additional copper connected to the ground and power signals.

EMI is improved by the closeness of a low-impedance plane limiting the radiated field associated with switching high-voltage and high-current signals.

Safety is improved by having the high voltage potentials completely enclosed by the PCB material except for where component connections are required.

Design Checklist

The following design checklist helps in considering the major concerns during the design and layout of a PCB.

- Schematic review successful
- Current loops
- Critical placement of components
- Copper weight
- Trace width
- Copper pour
- Copper thieving
- Via for power
- Via for power control
- Via for signal
- Via placement for power pin
- Via quantity for power plane
- Via quantity for power control
- Thermal connections sized
- Prioritized trace routing
- Test points located at signal of interest
- Test points have matching ground connections
- Voltage and power loss
- Multiple power vias used
- EPAD thermal
- PCB material
- Encapsulation
- Safety
- Layers

Example PCB Layout

The example used in this application note is Cypress's 17 W CY8CLEDAC02 PAR30 design and PCB layout. (Reference design 001-60473)

Schematic

The complete schematic is shown in Appendix A – Schematic on page 12. This one-page schematic is the entire AC02 circuit with all of the loops shown together. The loops detailed in this application note are all in the schematic.

Critical Loops

The first step in PCB layout for the AC02 is identifying the critical loops. A critical loop is one where the current is not constantly flowing. An example is a switch (FET in the AC02 circuit) forces the current to change path. The FET, when on, is low impedance and the current flows through it. When the FET turns off, the current continues to flow, only through the path of lowest impedance (no longer the FET switch). The section of current flow path that changes between FET on and FET off is the discontinuous path. The discontinuous path is critical and must be minimized.

Boost Circuit

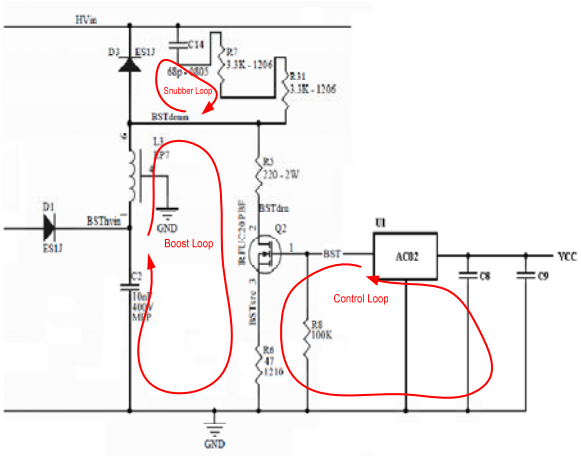
The Boost circuit is shown in the following figure. In the following circuit, there are three loops: Boost, Boost snubber, and Boost control.

The boost loop is comprised of D1 (power input from full-wave bridge rectifier), D3 (Boost power output), C2 (working power storage), L3 (Boost inductor), R5 (Impedance matching load for Dimmer operation), Q2 (Boost switching FET), and R6 (Boost power limiter).

The boost snubber loop is comprised of D3 (Boost output diode), C14 (Boost snubber capacitor), and R7 & R31 (Boost snubber resistors; two are shown for high-line operation).

The Boost control loop is comprised of Q2, R6, R8, U1 (AC02) and C8 & C9 (VCC capacitors).

Figure 12. Boost Circuit



Flyback Loop

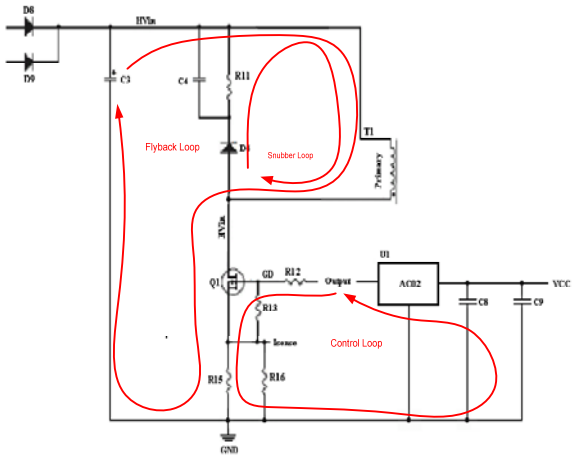
The Flyback circuit is shown in the following figure. In the following circuit, there are three loops: Flyback, Flyback snubber, and Flyback control.

The Flyback loop is comprised of D8 and D9 (power input), C3 (working power storage), T1 (Transformer inductor), Q1 (Flyback switching FET), and R15 &R16 (Current sense resistors: two resistors in parallel for improved current sense accuracy).

The Flyback snubber loop is comprised of D4 (Flyback snubber diode), C4 (Flyback snubber capacitor), and R11 (Flyback snubber resistor).

The Flyback control loop is comprised of Q1 (Flyback FET), R12 (FET gate resistor), R15 & R16 (Current sense resistors: two resistors are used in parallel for improved current sense accuracy), U1 (AC02) and C8 & C9 (VCC capacitors). R13 is not part of the control loop; the purpose of R13 is gate charge control.

Figure 13. Flyback Loop



Output Loop

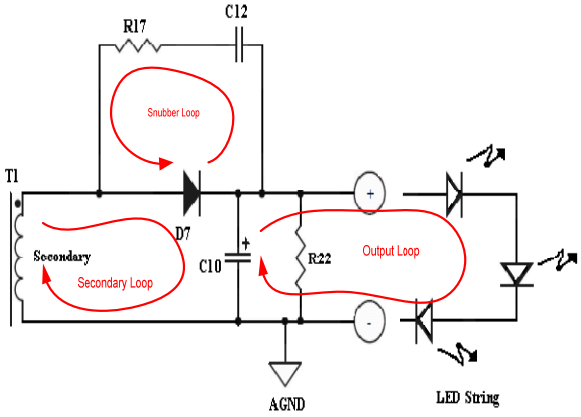
The Flyback circuit is shown in the following figure. In the following circuit, there are three loops: Secondary, Output snubber, and Output.

The Secondary loop is comprised of T1 (transformer: power source), D7 (half-bridge rectification of power source), and C10 (working power storage).

The Output snubber loop is comprised of D7 (Output rectification diode), C12 (Output snubber capacitor), and R17 (Output snubber resistor).

The Output loop is comprised of C10 (working power storage) and the LED string. R22 is not part of the Secondary or Output loops; the purpose of R22 is output charge removal if the LED string should fail as an open circuit.

Figure 14. Output Loop



V_{CC} Loop

The V_{CC} circuit is shown in the following figure. In the following circuit, there are two loops: Bias and V_{CC}.

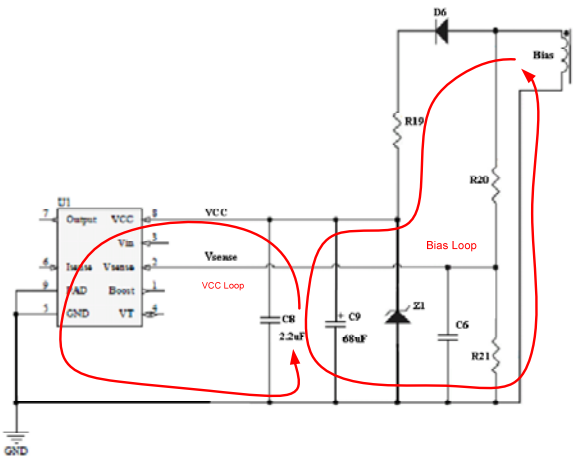
The Bias loop is comprised of T1 (transformer: power source), D6 (half-bridge rectification of power source), R19 (Current limiting resistor), and C8 and C9 (working power storage; C9 is the larger storage capacitor, so it will be the primary source to receive the working power; C8 is the smaller capacitor, so it will be the first power source used by U1).

The V_{CC} loop is comprised of U1 (off-line controller) and C8 and C9 (working power storage: C8 is closest to U1 as it provides the first power at time of use).

Z1 is not part of the Bias or V_{CC} loops; the purpose of Z1 is protection of U1 should the Bias voltage increase above 16 V.

R20, R21, and C6 are not part of any loop, as current flow is not switched during operation. The current flow through R20 and R21 is approximately 0.5 mA. C6 is present for noise filtering into the Vsense pin of U1.

Figure 15. V_{CC} Loop



Coupling of Nets

Two circuits contribute to crosstalk in the AC02 system. The two circuits are the Boost circuit and Flyback circuit.

The Boost circuit (AC02 only) high dV/dt net connects to the drain of FET Q2. This net is switching between approximately ground when the FET is on and approximately 200 V (HVin plus Boost ringing) when the FET is off. This gives us a dV of 200 V. The dt of the equation is 1 - 3 ns based upon the inductance and leakage capacitance of the Boost circuit for this system.

The Flyback circuit high dV/dt net connects to the drain of FET Q1. This net is switching between approximately ground when the FET is on and approximately 250 V (HVin plus Flyback ringing) when the FET is off. This gives us a dV of 250 V. The dt of the equation is 1 - 3 ns based upon the inductance and leakage capacitance of the Flyback circuit for this system.

Nets that may be sensitive to coupling are low-voltage nets Vin, Vsense, SD, and Isense.

The Vin pin controls the AC02 flyback switching frequency based upon the voltage present at the Vin pin. Coupling will cause regulation inconsistency and EMI problems.

The Vsense pin provides for control of the voltage feedback sensing. Coupling to the Vsense will cause output current inconsistency.

The SD net connects to the VT pin of the AC02. The VT pin input voltage provides over-temperature shutdown. Coupling the VT (SD) net causes the system to shutdown and restart.

The Isense pin determines the output current accuracy. Coupling to the Isense net causes output noise or current variance.

Design Example Database

The design example used in this application note can be downloaded at http://www.cypress.com/?rID=40923.

The database contains the Schematic, PCB layout, Gerber files, BOM, and PDF files allowing you to fully, evaluate the design.

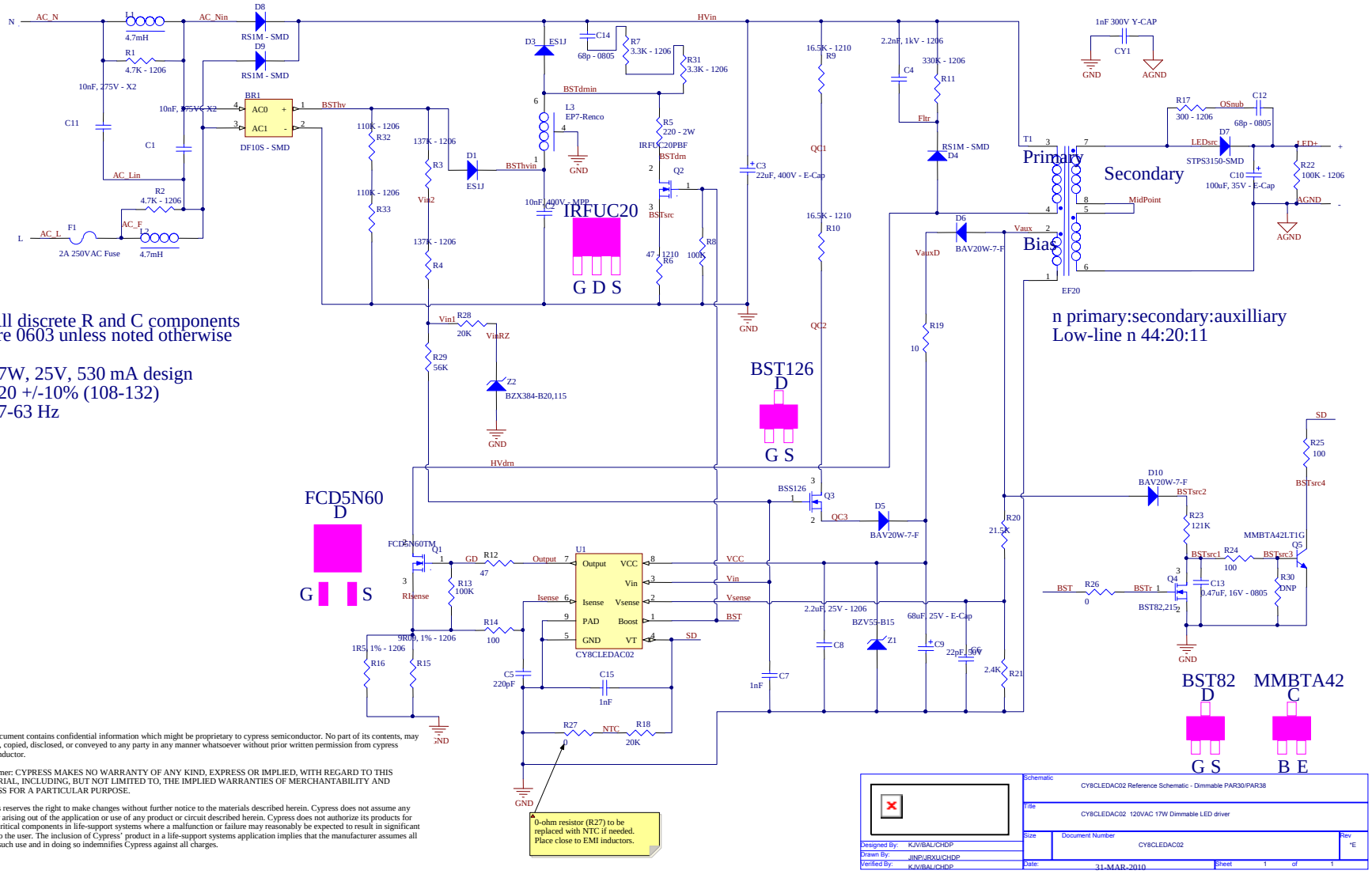
The database was created using Altium Designer Summer 09 release.

Summary

This application note provides expert advice, guidelines, and insights into PCB design for LED power drivers using CY8CLEDAC0x. It discusses component placement, signal routing, power routing, power paths, and thermal dissipation.

With the help of the PCB guidelines provided in this application note, it can be understood that an LED driver is similar to a switching power supply, many of the design guidelines provided are similar to other designs, and you are capable of designing your first off-line AC/DC LED driver system.

Appendix A – Schematic



Appendix B: Additional Information

- www.cypress.com

  Cypress's corporate website. This website covers all of Cypress's products and provides access to additional information.

- www.cypress.com/go/lighting

  Cypress's EZ-Color website. This website provides access to AC0x datasheets, AC0x reference designs, AC0x application documents, PowerPSoC data sheet, PowerPSoC technical reference manual, development kits, and Hi-Tech (third party C complier).

- www.cypress.com/psocdesigner

  Cypress's free development software. This website provides easy access to download the most current development software.

- www.cypress.com/psocprogrammer

  Cypress's free development programmer software. This website also provides information for Cypress's MiniProg 'CY3210-MiniProg1'. The MiniProg kit is an inexpensive evaluation kit for programming PSoC and PowerPSoC during system development.

- www.cypress.com/support

  Cypress's online technical support website. It includes, to list a few, knowledge base, application notes, technical documents, and user forums.

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Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2953701	CHDP	06/30/2010	New application note
*A	3009394	CHDP	08/17/2010	Updated Schematic diagram in Appendix. Changed the title from 'PCB Guidelines for AC0x as a LED Driver' to 'PCB Guidelines for AC-DC Controller as a LED Driver', added CY8CLEDAC02 under associated part family per Brian Moody's (XBM) suggestions.
*B	3182451	CHDP	02/25/11	Changed grammar and typographic for reading ease.

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