Amrita Vishwa Vidyapeetham
B.Tech. Degree CSE (AI) First Semester
Computational Engineering and Networking

19AIE101-Elements of Computing Systems-1 : Presentation Assignment 2 (Group-wise)

Max marks: 100

This evaluation aims at the following course coutcome
CO1: Explain the concept of Boolean Algebra and Digital Logic
CO2: Implement different combinational and sequential digital logic systems

Qn No	Question	Marks
1	Design a half adder and a Full adder (with logic circuit for sum and carry). Implement the gate level logic of both the chips in HDL and test the chip in hardware simulator. (The chips and supporting files are available in project folder of nand2tetris software suite. Use script based simulation during presentation to show the results. Note that XOR implemenation is required in prior).	20
2	Design a Full adder using two half adders and an OR gate. Justify the gate level logic obtained for sum and carry function. Implement the designed logic in HDL using half adder chip constructed in Question 3 and test the chip in the hardware simulator. Give the CHIP name as "FAusingHA". (Use script based simulation (by creating script and cmp files) during presentation to show the results)	20
3	Implement and test the following chips in the HACK platform (Use script based simulation during presentation to show the results). (a) NOT (chip name in project folder: Not16), which is 16-bit bitwise NOT (b) AND (chip name in project folder : And16), which is 16-bit bitwise AND (c) OR (chip name in project folder : Or16), which is 16-bit bitwise OR (d) Multi-way variant chip Or8way (ie, OR together all 8 bits of the input)	20
4	Design a 16-bit parallel adder. Implement the chip logic in HDL and test the chip using hardware simulator. (The chip (Name: Add16) and supporting files are available in project folder of nand2tetris software suite. Use script based simulation during presentation to show the results).	20
5	Design a 4-bit Carry Look-Ahead Adder circuit without full adder. Give the CHIP name as "CarryLookAheadAdder". Implement the chip logic in HDL and test the chip using hardware simulator (Use interactive simulation during presentation to show the results.)	20

***50 % weightage of marks for each question is for the quality of presentation and the ie., Out of the total 100 marks; Correctness of answers =50 Marks**	
Rubrics for Presentation (Max Marks: 50)	Marks
Nicely prepared slides and excellent oral presentation	50
Slides are good, presentation is not good or vice versa	40
Slides and presentation are of average quality	30
Slides and presentation are of below average quality	20