Project Topics for B.Tech CSE AI (2021-2025)

21AIE101 -Elements of Computing Systems-1
21AIE105 – Object-Oriented Programming

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Part A (compulsory for all teams)

- **Design and implement 16-bit HACK CPU (common to all groups)**
  - As a part of this project, the team is expected to study the architecture of a general-purpose central processing unit and how it can be programmed/implemented in hardware description language and Object-Oriented language.
  - The design of all the constituent elements such as logic gates, multiway chips, Multiplexers, Adders, Program counter, Register, etc, must be made from NAND gates.
  - **For 21AIE101- EOC-1**
    - The implementation must be shown in the Hack Platform. Moreover, the CPU built must be shown as a part of the Hack computer and tested using machine-level programs.
  - **For 21AIE105 – Object-Oriented Programming**
    - The constituent elements of the Hack CPU must be implemented in JAVA, starting from the implementation of NAND gates, calling all constituent elements as per the architecture, and finally delivering the functionality of CPU. You must give an input bit sequence and show the corresponding output.

Part B (specific to a Team)

As a part of this project, the team is expected to study the design of the digital logic systems and how it can be programmed/implemented in hardware description language and Object-Oriented language

1	Design and Implement a circuit which can perform multiplication by repeated addition
2	Design and implement 16-bit carry-select adder with a uniform block size of 4
3	Design and Implement a Sequence detector which detect bit pattern "0110'
4	Design and implement 16-bit carry-select adder with variable size (block sizes of 2-2-3-4-5)
5	Design and implement a 16-bit parallel adder/subtractor (a circuit which can perform both operation)
6	Design a synchronous counter that count down from decimal digit 9 onwards to 0
7	Design and implement a 16-bit Adder using 4-bit Carry Look Ahead Adder (CLA)
8	Design and Implement BCD to seven segment decoder
9	Design and Implement a 2-bit Serial Binary Adder using an SR flip flop
10	Design and Implement 4-bit Universal Shift register using D Flip flops
11	Design and implement a synchronous BCD counter using JK flip flop
12	Design and implement synchronous UP/DOWN counter circuit using JK Flip flops (up counting from 0 to 15 and downcounting 15 to 0 based on a control input)
13	Design and implement 4-bit ring counter and Jhonson counter.

Instructions

For 21AIE101- EOC-1

- The implementation must be shown in the Hack Platform. Built-in chips should not be used in any implementations except the D-flip flop. However, improvisation in any other platforms like CircuitVerse, Falstad, etc is allowed.

For 21AIE105 – Object-Oriented Programming

- The constituent elements of the design should be made from NAND gates. The functionality of the design should be shown as a JAVA program. You must give an input bit sequence and show the corresponding output, wherever applicable.

Project-Team Allocation for Part B

Project Number	1	2	3	4	5	6	7	8	9	10	11	12	13
Teams	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13
	B7	B6	B5	B4	B3	B2	B1	A19	A18	A17	A16	A15	A14
	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17	B18	B19	B20