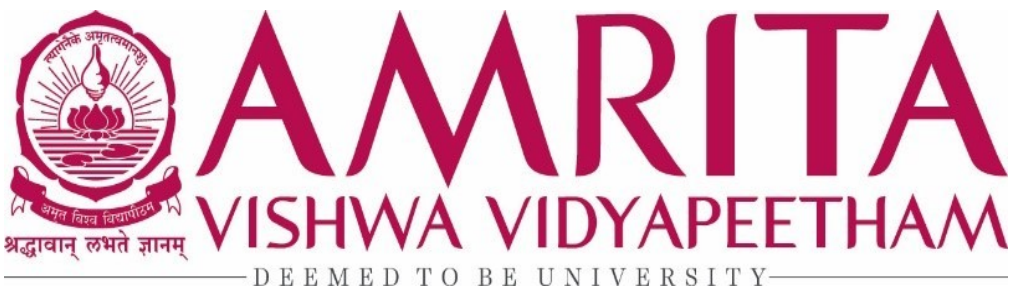
ASSIGNMENT-5

INTRODUCTION TO ELCTRICAL ENGINEERING

Professor-Dr. Neethu Mohan



Contributed By: -

BATCH-A	TEAM-7
GAJULA SRI VATSANKA	CB.EN.U4AIE.21010
GUNNAM HIMAMSH	CB.EN.U4AIE.21014
M.PRASANNA TEJA	CB.EN.U4AIE.21032
VIKHYAT BANSAL	CB.EN.U4AIE.21076

Question-1: -

Perform the experiment for demonstrating Common-Emitter Characteristics of an NPN transistor in Falstad circuit simulator

a) Explain the theory behind the experiment.

b) Draw the circuit diagrams, Mention the components used, and state the procedure of the experiment.

c) Plot the input and output characteristics.

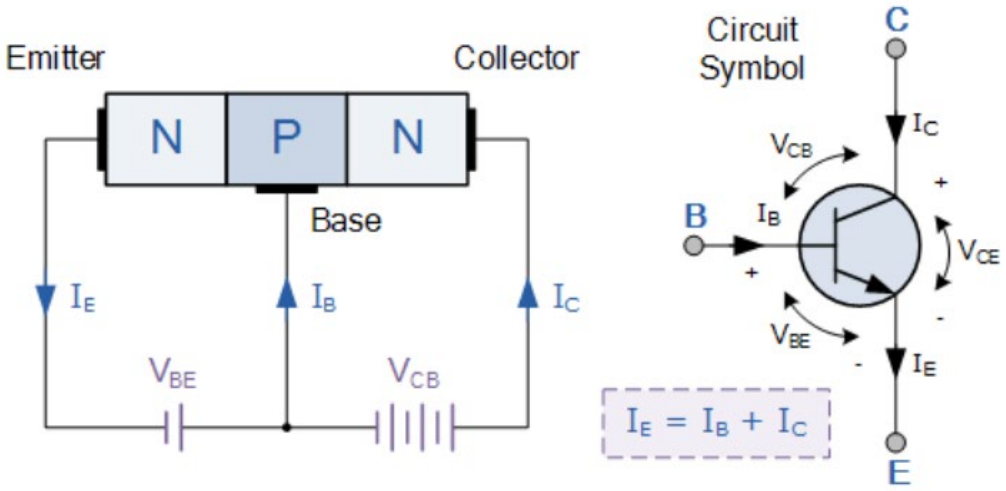
d) Calculate the following parameters –dynamic input resistance –dynamic output resistance –Common-base current gain

e) Comment on the values obtained in (d)

A) Explain the theory behind the experiment.

NPN Transistor: -

The voltage between the Base and Emitter (V_{BE}), is positive at the Base and negative at the Emitter because for an NPN transistor, the Base terminal is always positive with respect to the Emitter. Also the Collector supply voltage is positive with respect to the Emitter (V_{CE}). So for a bipolar NPN transistor to conduct the Collector is always more positive with respect to both the Base and the Emitter.



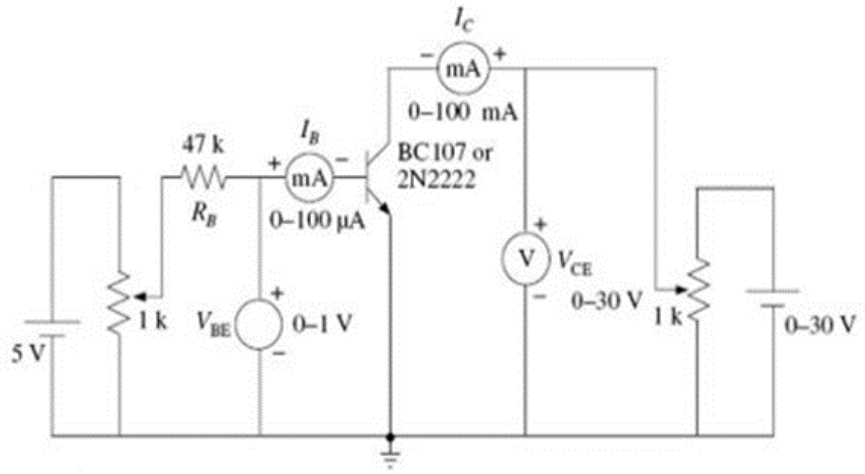
Then the voltage sources are connected to an NPN transistor as shown. The Collector is connected to the supply voltage V_{CC} via the load resistor, RL which also acts to limit the maximum current flowing through the device. The Base supply voltage V_B is connected to the Base resistor R_B, which again is used to limit the maximum Base current.

IE = IC + IB

- E represents Emitter.
- C represents collector.
- B represents Base.

Circuit diagram

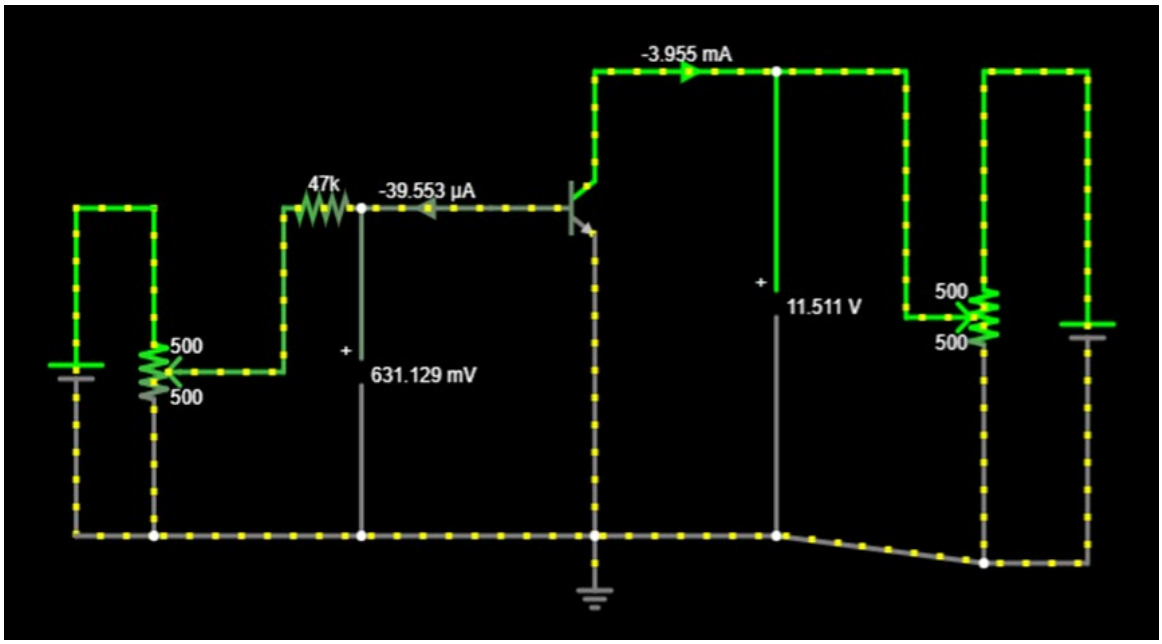
PROCEDURE



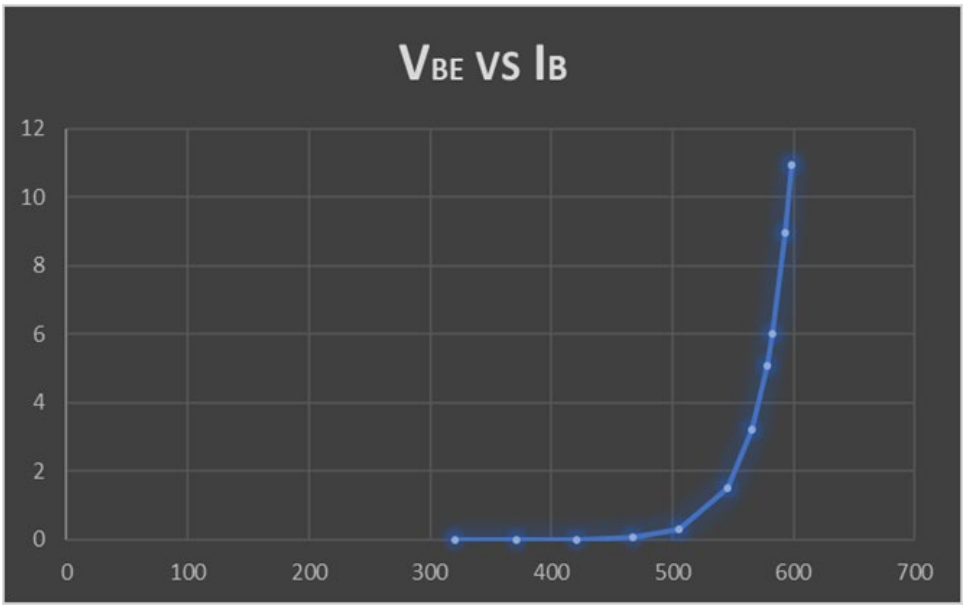
Procedure:

- A 2-terminal voltage source is connected to the potentiometer of 1kΩ resistance.
- To measure the current an ammeter is placed whose positive terminal is connected to the resistor of 47kΩ
- A voltmeter is connected to one terminal of the resistor and the ammeter to measure the voltage

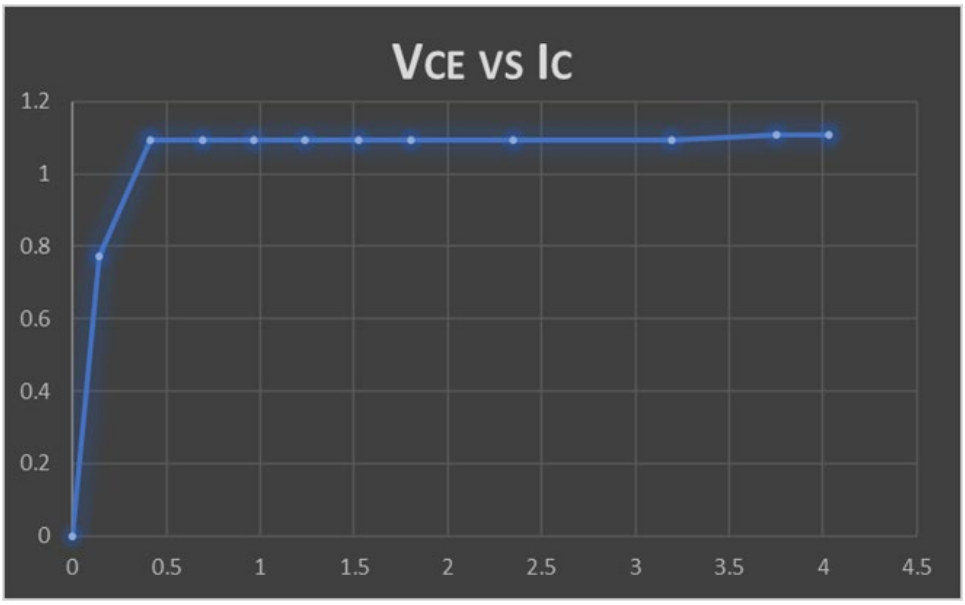
- The base of the npn transistor is connected to the ammeter while its collector is connected to the negative terminal of another ammeter.
- A potentiometer is connected to the positive terminal of the ammeter, voltmeter and the voltage source.



INPUT CHARACTERISTICS:



OUTPUT CHARACTERISTICS:



D) Dynamic output resistance: -

r= ΔVce/ΔIc , Ib is constant

Ro = (597.889 - 321) / (10.941 - 0)

= 25.307Ω where IB is 10A

Current Gain: -

$$\beta = \frac{I_C}{I_B}$$

= 4426 / 44.259 => 100.002

Dynamic input resistance: -

r= ΔVce/ΔIb ; Ic is constant.

Ri= (4.03 - 0.141) / (1.108 - 0)

=3.509Ω when VCE = 20V

E)

The Dynamic input resistance for a CE amplifier is low whereas the dynamic output resistance is high.

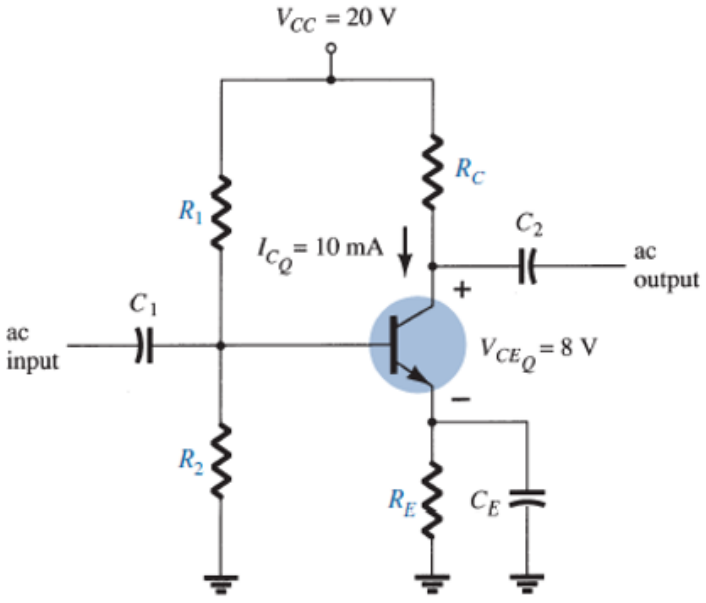
The current gain for the CE amplifier is high.

QUESTION-2

Design a BJT CE amplifier (in voltage-divider biasing configuration with an emitter Feedback resistor). Fix VCC=20V, and operating point as ICQ=10mA, VCEQ=8 V, and beta as 100 (Assume any values, if not given it). Plot the input and output waveforms. Calculate the input impedance, output impedance, voltage gain and current gain with respect to source. Comment on the values obtained.

BJT Amplifier

A BJT can be represented in an ac model circuit. Three amplifier configurations are the common-emitter, the common-base, and the common-collector. The common-emitter (CE) configuration has the emitter as the common terminal, or ground, to an ac signal. CE amplifiers exhibit high voltage gain and high current gain.



Transistor amplifier's amplify an AC input signals that alternates between some positive value and a corresponding negative value. Then some way of "presetting" the amplifier's circuit configuration is required so that the transistor can operate between these two maximum or peak values. This can be achieved using a process known as **Biasing**.

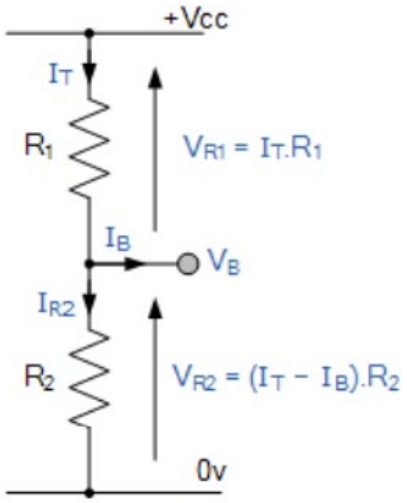
Biasing is very important in amplifier design as it establishes the correct operating point of the transistor amplifier ready to receive signals, thereby reducing any distortion to the output signal.

Also, the use of a static or DC load line drawn onto the output characteristics curves of an amplifier allows us to see all the possible operating points of the transistor from fully "ON" to fully "OFF", and to which the quiescent operating point or **Q-point** of the amplifier can be found.

The aim of any small signal amplifier is to amplify all of the input signal with the minimum amount of distortion possible to the output signal, in other words, the output signal must be an exact reproduction of the input signal but only bigger (amplified).

To obtain low distortion when used as an amplifier the operating quiescent point needs to be correctly selected. This is in fact the DC operating point of the amplifier and its position may be established at any point along the load line by a suitable biasing arrangement.

BJT Common Emitter Amplifier Circuit



The single stage common emitter amplifier circuit shown above uses what is commonly called "Voltage Divider Biasing". This type of biasing arrangement uses two resistors as a potential divider network across the supply with their centre point supplying the required Base bias voltage to the transistor. Voltage divider biasing is commonly used in the design of bipolar transistor amplifier circuits.

This method of biasing the transistor greatly reduces the effects of varying Beta, (β) by holding the Base bias at a constant steady voltage level allowing for best stability.

The quiescent Base voltage (Vb) is determined by the potential divider network formed by the two resistors, R1, R2 and the power supply voltage Vcc as shown with the current flowing through both resistors.

Then the total resistance R_T will be equal to R1 + R2 giving the current as $i = Vcc/R_T$. The voltage level generated at the junction of resistors R1 and R2 holds the Base voltage (Vb) constant at a value below the supply voltage.

The potential divider network used in the common emitter amplifier circuit divides the supply voltage in proportion to the resistance. This bias reference voltage can be easily calculated using the simple voltage divider formula below.

Amplifier Coupling Capacitors

In **Common Emitter Amplifier** circuits, capacitors C1 and C2 are used as **Coupling Capacitors** to separate the AC signals from the DC biasing voltage. This ensures that the bias condition set up for the circuit to operate correctly is not affected by any additional amplifier stages, as the capacitors will only pass AC signals and block any DC component. The output AC signal is then superimposed on the biasing of the following stages. Also, a bypass capacitor, C_E is included in the Emitter leg circuit.

This capacitor is effectively an open circuit component for DC biasing conditions, which means that the biasing currents and voltages are not affected by the addition of the capacitor maintaining a good Q-point stability.

However, this parallel connected bypass capacitor effectively becomes a short circuit to the Emitter resistor at high frequency signals due to its reactance. Thus, only R_L plus a very small internal resistance acts as the transistors load increasing voltage gain to its maximum. Generally, the value of the bypass capacitor, C_E is chosen to provide a reactance of at most, 1/10th the value of R_E at the lowest operating signal frequency.

Types of BJT Common Emitter Transistor amplifier

- Unloaded BJT Transistor Amplifier
- Loaded BJT Transistor Amplifier
- With Source and Load Transistor Amplifier

We can draw all the circuit on FALSTAD but we will do calculations only for transistor with Source and Load.

Formulae:

$$V_E = \frac{1}{10}V_{CC}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C}$$

$$V_B = V_{BE} + V_E$$

$$R_2 \leq \frac{1}{10}\beta R_E$$

$$V_B = \frac{R_2}{R_1 + R_2}V_{CC}$$

Input Impedance:

$$Z_i = R_1 \| R_2 \| \beta r_e$$

$$Z_i = R' \| \beta r_e$$

Output Impedance:

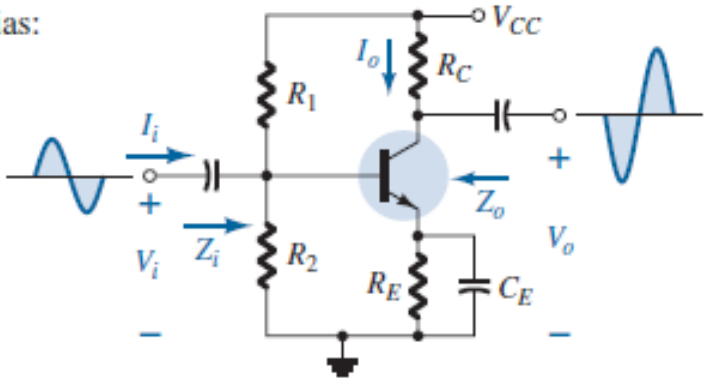
$$Z_o = R_C \| r_o$$

$$Z_o \cong R_C$$

$r_o \geq 10R_C$

We will consider Z_o as R_C only.

Voltage-divider bias:



Voltage Gain

- Loaded Voltage Gain

$$A_{v_L} = \frac{V_o}{V_i} = -\frac{R_C \| R_L}{r_e}$$

- Source with Load voltage gain

$$A_{v_S} = \frac{Z_i}{Z_i + R_S} A_{v_L}$$

For the same configuration $A_{v_{NL}} > A_{v_L} > A_{v_s}$.

Current Gain

$$A_{i_L} = -A_{v_L} \frac{Z_i}{R_L}$$

Calculation:

Common Calculation for all the type of amplifiers.

$V_E = 1/10 * V_{CC}$

$= 1/10 * 20\ V$

$R_E = V_E/I_E$

$= VE/IC$

$= 2\ V/10\ mA$

$= 200\ \Omega$

$R_C = V_{RC}/I_C$

$= VCC – VCE – VE/IC$

$= 20\ V – 8\ V – 2\ V/\ 10\ mA$

$= 1k\ \Omega$

$V_B = V_{BE} + V_E$

$= 0.7\ V + 2\ V$

$= 2.7\ V$

$$R_2 \leq \frac{1}{10}\beta R_E$$

$R2 = (1/10) * (100) * (0.2k\ \Omega)$

$= 2k\Omega$

V_B = 2.7V
= (2k Ω) * (20V) / (R1 + 2k Ω)

→(2.7V) * (R1 + 2000) Ω = 40k Ω
→2.7R1 + 5400 = 40,000

R_1 = 12.814k Ω

r_e = 26mV / 10mA
= 2.6

Values of C_1 and C_2

$$C_1 = \frac{1}{2\pi \times R_i \times f}$$

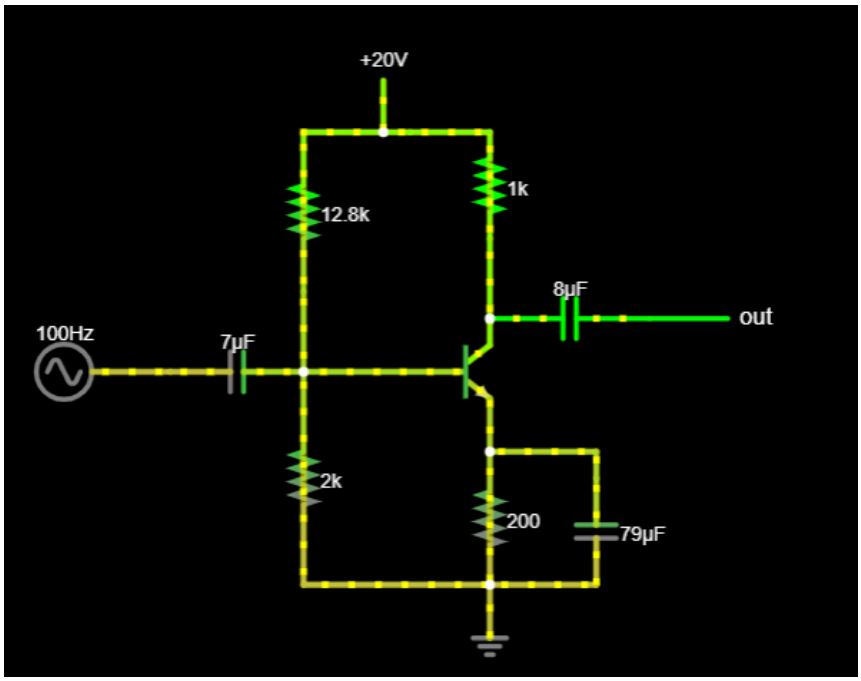
C_1 = 1/(2 * 3.14 * 226.025 * 100)
= 7.04 = 7(Approx.) μF

C_2 = 8 μF (Using value near to C1)

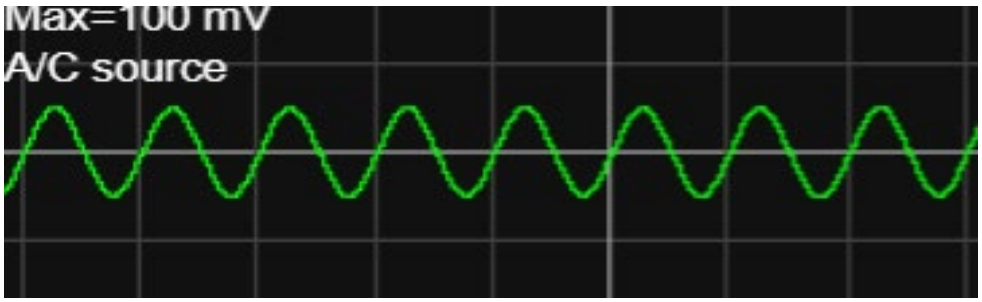
C_E = 1/(2 * 3.14 * 20 * 100)
= 79 μF

- Unloaded BJT Transistor Amplifier [FALSTAD] {LINK}

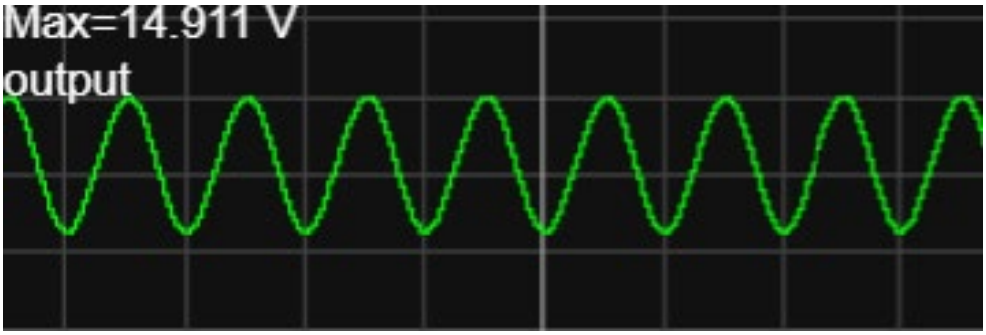
Circuit:



Input Waveform:

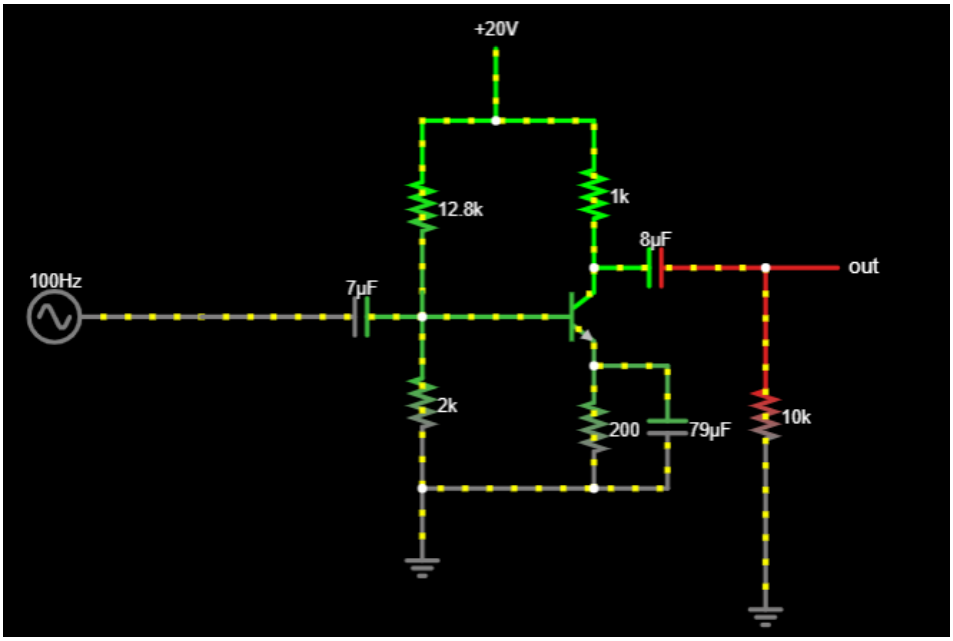


Output Waveform:

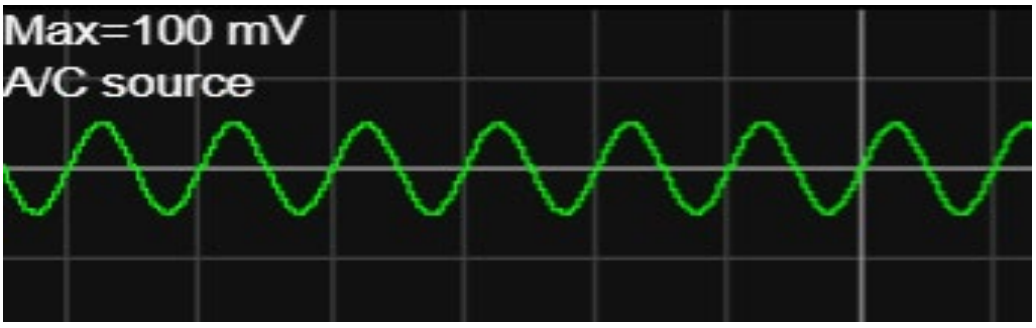


- Loaded BJT Transistor Amplifier [FALSTAD] {LINK}

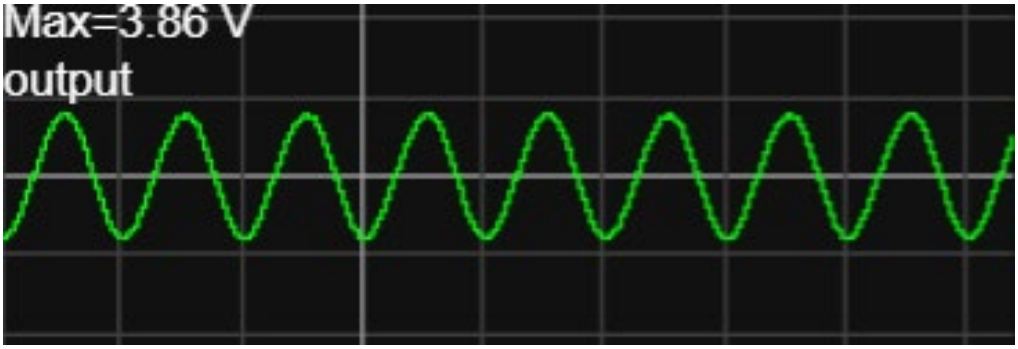
Circuit:



Input Waveform:

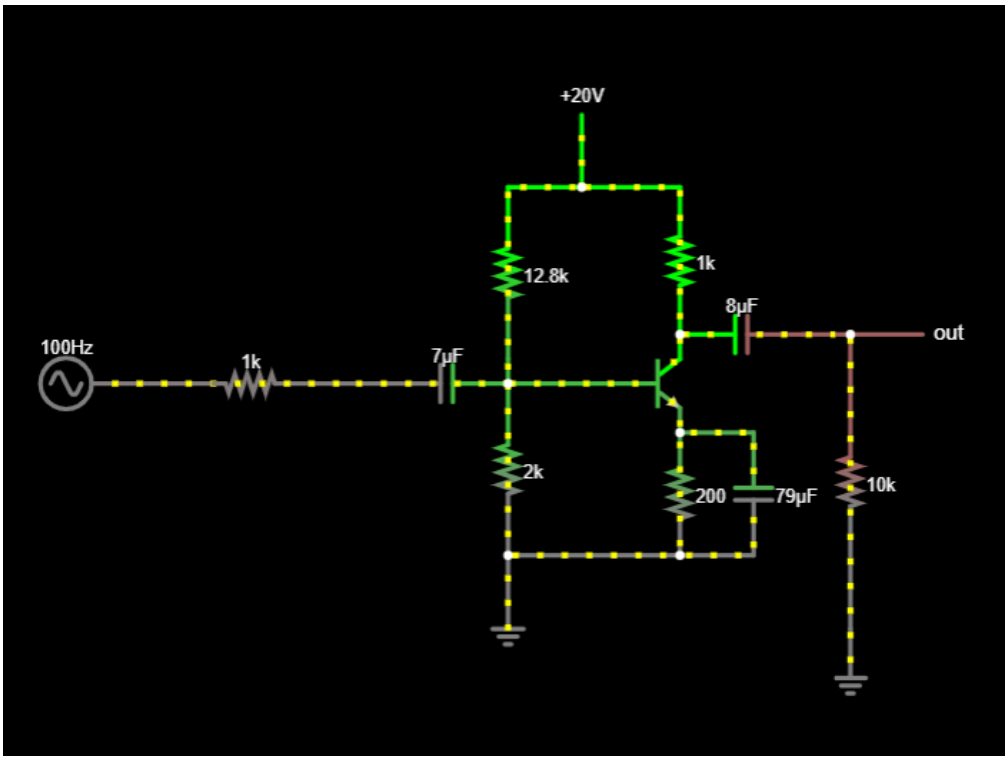


Output Waveform:



- With Source and Load Transistor Amplifier [FALSTAD] {LINK}

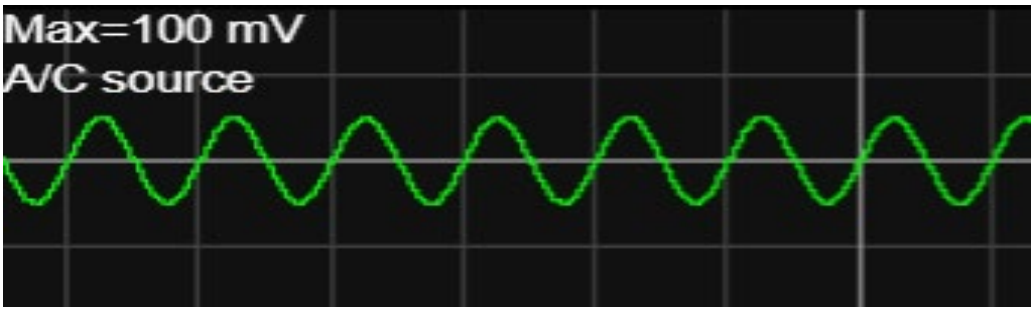
CIRCUIT:



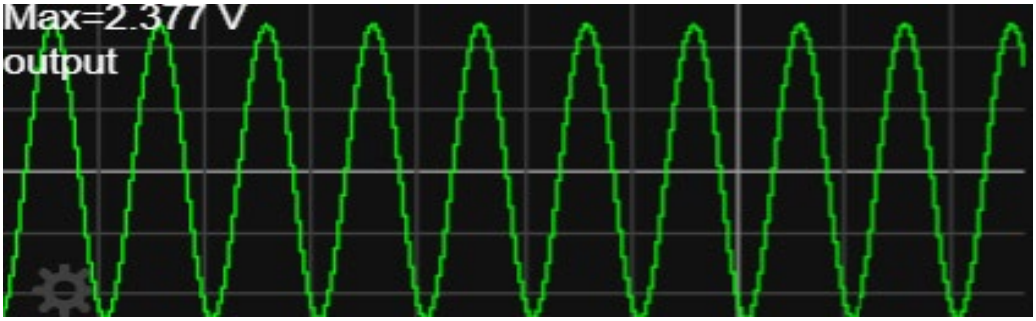
R_S : 1k Ω

R_L : 10k Ω

Input Waveform:



Output Waveform:



Calculation w.r.t Source

Input Impedance:

$$Z_i = R_1 \| R_2 \| \beta r_e \qquad Z_i = R' \| \beta r_e$$

R_1 = 12.8k Ω

R_2 = 2k Ω

Beta = 100

r_e = 2.6 Ω

= (12.8k) * (2k) * (100*2.6)/ (12.8k) * (2k) + (2k) * (100*2.6) + (12.8k) * (100*2.6)

= 226.025 Ω

Output Impedance:

$$Z_o = R_C \| r_o$$

$$Z_o \cong R_C \qquad r_o \geq 10R_C$$

$Z_o = R_c$

Z_o = 1k Ω

Voltage Gain:

- Loaded Voltage Gain

$$A_{v_L} = \frac{V_o}{V_i} = -\frac{R_C \| R_L}{r_e}$$

- Source with Load voltage gain

$$A_{v_S} = \frac{Z_i}{Z_i + R_S} A_{v_L}$$

Using formula:

A_{VL} = - (1k Ω) || (10k Ω) / (2.6 Ω)

= -(10k^2 Ω / (11k Ω) *(2.6 Ω))

= -349.65

A_{VS} = ((226.025 Ω) * (-349.65 V)) / (226.025 Ω + 100 Ω)

= -242.403

$A_{VL} > A_{VS}$

Current Gain:

$$A_{i_L} = -A_{v_L}\frac{Z_i}{R_L}$$

Using Formula:

A_{iL} (w.r.t load) = -(-349.65 V) * (226.025 Ω /10k Ω)
= 7.90

A_{iS} (w.r.t source) = $-A_{vs}$ * (Z_i / R_L)

A_{iS} (w.r.t source) = -(-242.043 V) * (226.025 Ω /10k Ω)
= 5.47

QUESTION-3

Design a BJT CE amplifier (in fixed-biasing configuration). Fix VCC=20V, and

operating point as ICQ=10mA, VCEQ=8 V, and beta as 100 (Assume any values, if

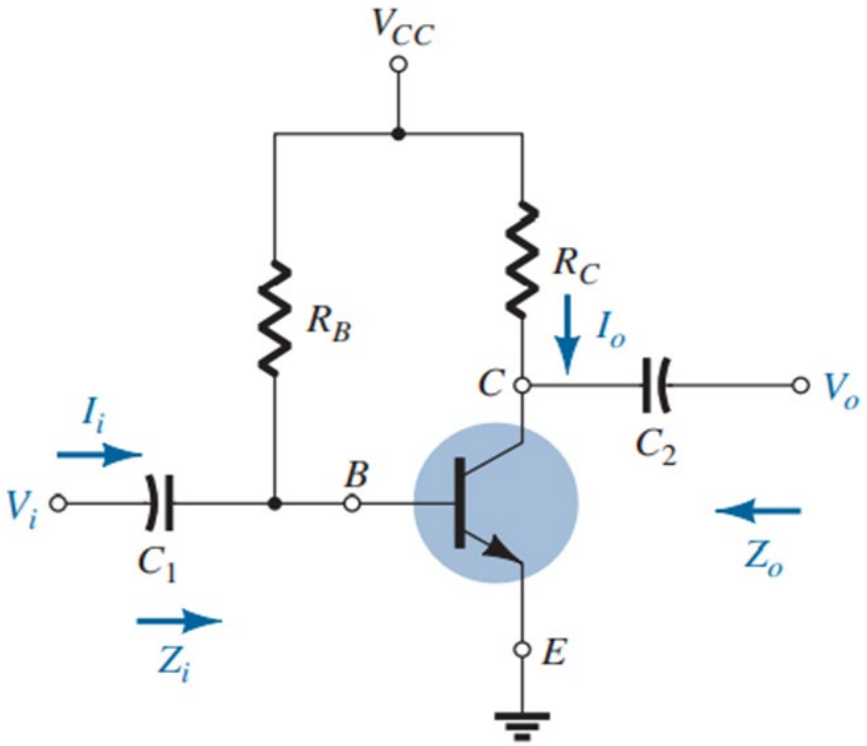
not given it). Plot the input and output waveforms. Calculate the input

impedance, output impedance, voltage gain and current gain with respect to

source. Comment on the values obtained

Common-emitter

Fixed-bias Configuration



Calculations

$$V_E = V_{CC} - V_{CE} = 12 - 6 = 6\,V$$

$$I_C = 2\,m\,A$$

$$R_E = \frac{V_E}{I_E} \approx \frac{V_E}{I_C} = 3k\,\Omega$$

$$V_B = V_{BE} + V_E = 6.7\,V$$

$$R_2 \leq \frac{\beta R_E}{10}$$

$$R_2 \leq 30\,k\Omega$$

$$V_B = \left(\frac{R_1}{R_1 + R_2}\right) V_{CC}$$

by solving above equation , we get R_1 =23.7$k\Omega$

$$C_1 = \frac{1}{2\pi Z_i f}$$

$$Z_i = R_1 \parallel R_2 \parallel \beta r_e$$

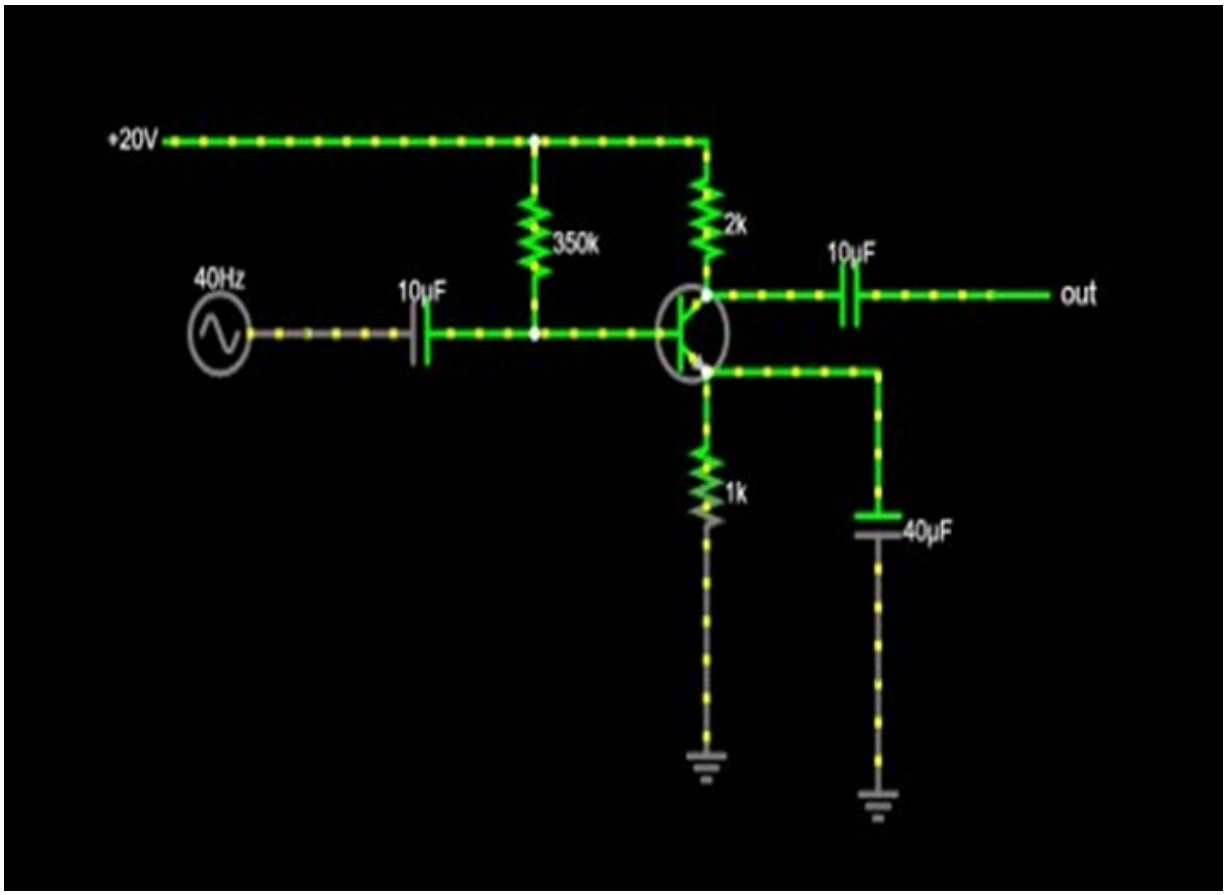
$$\beta r_e = 1.3\,k\Omega$$

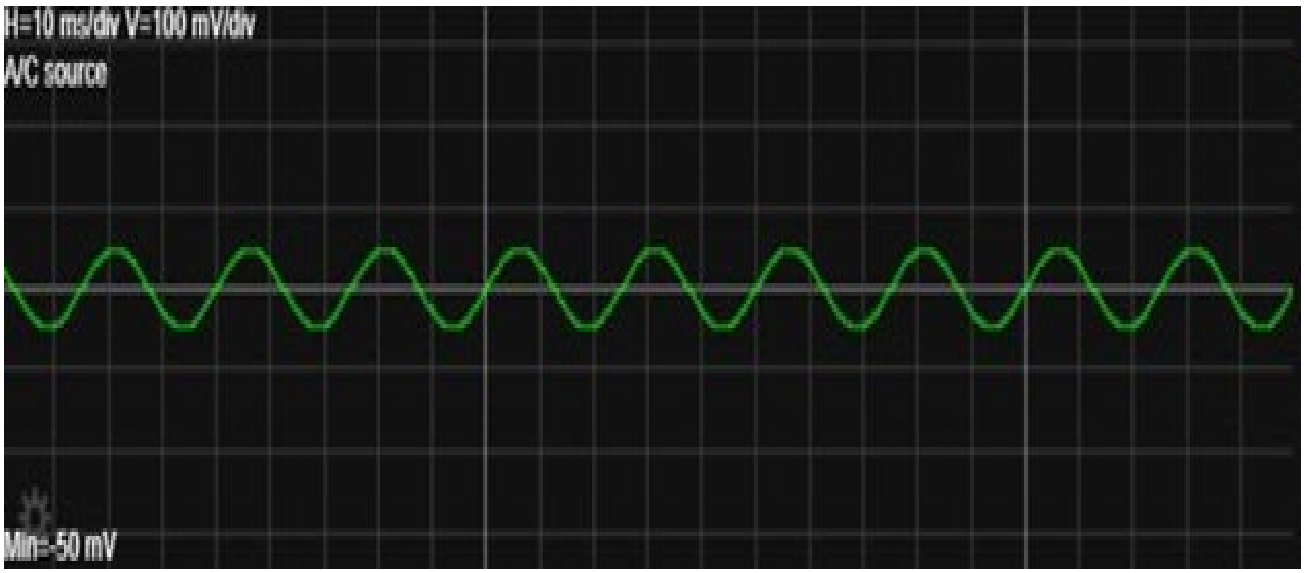
$$Z_i = 1.2k\Omega$$

for frequency $f = 50$ hz

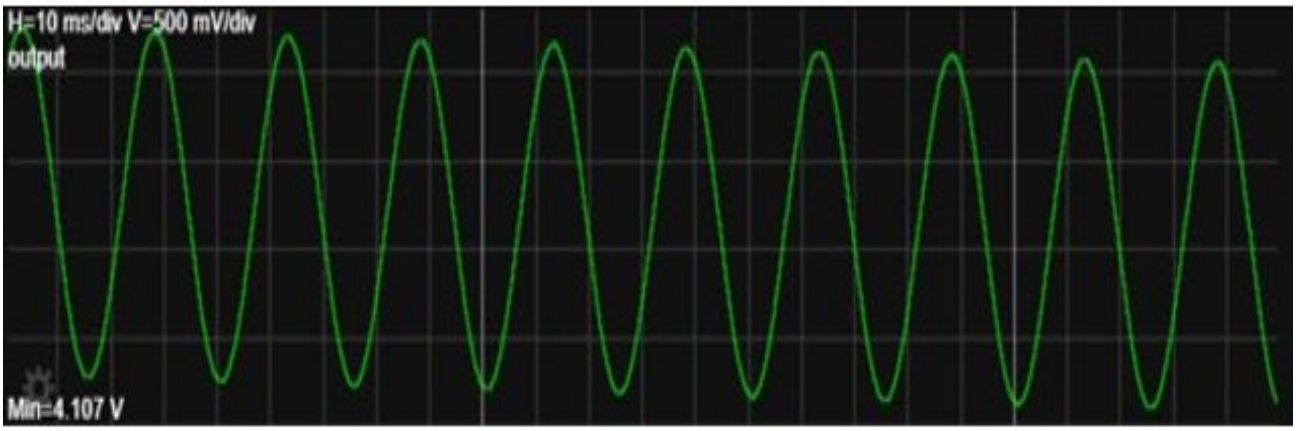
C_1 = 3.4 μF

CIRCUIT DIAGRAM





OUTPUT WAVEFORM

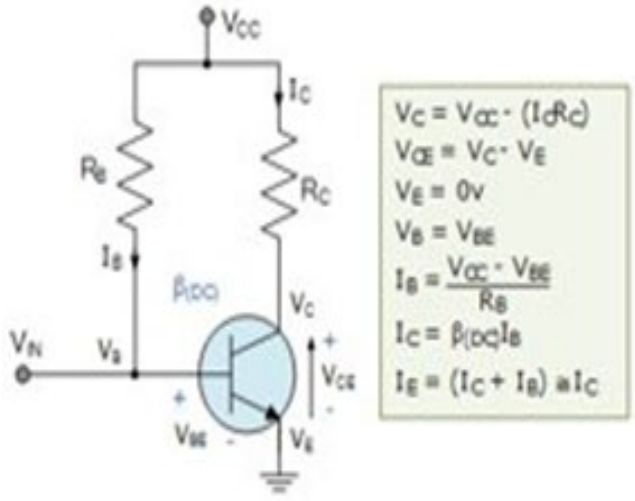


The circuit displayed is referred to as a "fixed base bias circuit" since the operating point of the transistors must also be stable because the base current of the transistors, IB, is constant for specific values of Vcc. Using a fixed current bias, this two resistor biassing network is utilized to create the transistor's initial functioning area

$$V_{CC} = I_B R_B + V_{BE}$$

$$\Rightarrow I_B = \frac{(V_{CC} - V_{BE})}{R_B}$$

- Thus, the base current may be changed to the required value simply by altering the resistor's value. Additionally, IC may be determined in accordance by applying the current gain () relationship. Therefore, it is possible to modify the Q point simply by altering the value of the resistor attached to the base.



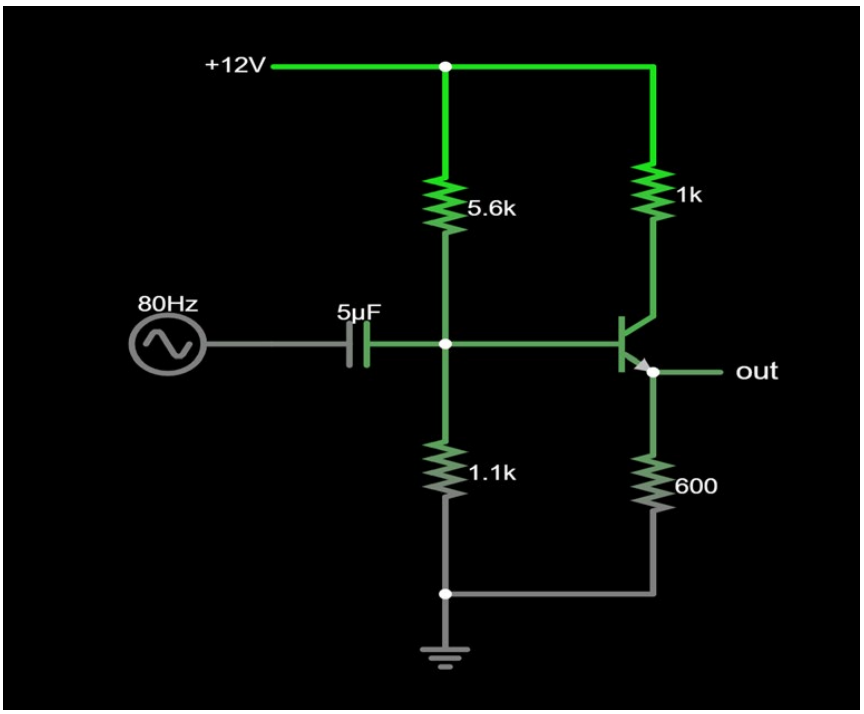
- The circuit displayed is referred to as a "fixed base bias circuit" since the operating point of the transistors must also be stable because the base current of the transistors, IB, is constant for specific values of Vcc. Using a fixed current bias, this two resistor biassing network is utilized to create the transistor's initial functioning area.

QUESTION-4

Design a unity gain amplifier (CC amplifier/ Emitter follower) using BJT (in voltage-divider biasing configuration with an emitter Feedback resistor). Fix VCC=12V, and operating point as ICQ=2mA, VCEQ=6 V, and beta as 100 (Assume any values, if not given). Plot the input and output waveform. Calculate the input impedance, output impedance, voltage gain and current gain with respect to source. Comment on the values obtained.

ANSWER: -

Circuit Diagram



Input graph:-

Output graph:-

Input impedance: -

Zi = R1 || R2 || beta*Re

Zi = 905.52 ohm

Output impedance: -

Zout = re = 13 ohm.

Current gain: -

$$A_I = \frac{I_{emitter}}{I_{base}}$$

$$A_I = \frac{I_{collector} + I_{base}}{I_{base}}$$

$$A_I = \frac{I_{collector}}{I_{base}} + 1$$

$$A_I = \beta + 1$$

Voltage gain: -

$$V_o = \frac{R_E V_i}{R_E + r_e} \qquad A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e} \qquad A_v = \frac{V_o}{V_i} \cong 1$$

Inference : -

- Input impedance is very high
- Output impedance is low
- The Voltage gain value is approximately equal to but less than 1
- From the properties of this circuit it is best applicable as a voltage buffer.

THANK YOU