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PROJECT	Design of 32-bit Dadda Multiplier using accurate 4:2 compressor, model in Verilog HDL	Design of 64-bit Dadda Multiplier using accurate 4:2 compressor, model in Verilog HDL	Design of 32-bit Dadda Multiplier using accurate 5:2 compressor, model in Verilog HDL	Design of 64-bit Dadda Multiplier using accurate 5:2 compressor, model in Verilog HDL	Design of 32-bit Dadda Multiplier using accurate 15:4 compressor, model in Verilog HDL