	Mentor and TA	Mentor and TA	Mentor and TA	Mentor and TA	Mentor and TA
Name	Mr Varma	Mr Dhayal	Ms Skanda	Ms Sameera	Mr Zubair
Experiments	coe16d001@iiitdm.ac.in	edm17d002@iiitdm.ac.in	edm17d001@iiitdm.ac.in	coe18d002@iiitdm.ac.in	coe20d003@iiitdm.ac.in
Exp9	XILINX Design Flow - store Imag1 in one block ram and image2 in another block ram, design image addition design and control logic to read each pixel from each image and perform addition resultant result store in another block ram.	XILINX Design Flow - store Imag1 in one block ram and image2 in another block ram, design image addition design and control logic to read each pixel from each image and perform addition resultant result store in another block ram.	XILINX Design Flow - store Imag1 in one block ram and image2 in another block ram, design image addition design and control logic to read each pixel from each image and perform addition resultant result store in another block ram.	XILINX Design Flow - store Imag1 in one block ram and image2 in another block ram, design image addition design and control logic to read each pixel from each image and perform addition resultant result store in another block ram.	XILINX Design Flow - store Imag1 in one block ram and image2 in another block ram, design image addition design and control logic to read each pixel from each image and perform addition resultant result store in another block ram.