

	Mentor and TA	Mentor and TA	Mentor and TA	Mentor and TA	Mentor and TA
Name	Mr Varma	Mr Dhayal	Ms Skanda	Ms Sameera	Mr Zubair
Experiments	coe16d001@iiitdm.ac.in	edm17d002@iiitdm.ac.in	edm17d001@iiitdm.ac.in	coe18d002@iiitdm.ac.in	coe20d003@iiitdm.ac.in
Exp6	Design 32-bit Adder - recursive doubling based carry lookahead adder using verilog HDL	Design 32-bit Adder - recursive doubling based carry lookahead adder using verilog HDL	Design 32-bit Adder - recursive doubling based carry lookahead adder using verilog HDL	Design 32-bit Adder - recursive doubling based carry lookahead adder using verilog HDL	Design 32-bit Adder - recursive doubling based carry lookahead adder using verilog HDL