	Mentor and TA	**Mentor and TA**	**Mentor and TA**	**Mentor and TA**	**Mentor and TA**
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Exp8	XILINX Design Flow practice - 16-bit Array Multiplier design using Verilog HDL. Implementation on target FPGA board. Design parameter estimation.	XILINX Design Flow practice - 16-bit Array Multiplier design using Verilog HDL. Implementation on target FPGA board. Design parameter estimation.	XILINX Design Flow practice - 16-bit Array Multiplier design using Verilog HDL. Implementation on target FPGA board. Design parameter estimation.	XILINX Design Flow practice - 16-bit Array Multiplier design using Verilog HDL. Implementation on target FPGA board. Design parameter estimation.	XILINX Design Flow practice - 16-bit Array Multiplier design using Verilog HDL. Implementation on target FPGA board. Design parameter estimation.