	Mentor and TA	**Mentor and TA**	**Mentor and TA**	**Mentor and TA**	**Mentor and TA**
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Exp4	Design 8-bit shift Register using Bottom-up approach using Verilog HDL	Design 8-bit shift Register using Bottom-up approach using Verilog HDL	Design 8-bit shift Register using Bottom-up approach using Verilog HDL	Design 8-bit shift Register using Bottom-up approach using Verilog HDL	Design 8-bit shift Register using Bottom-up approach using Verilog HDL