	Mentor and TA	**Mentor and TA**	**Mentor and TA**	**Mentor and TA**	**Mentor and TA**
Name	Mr Varma	Mr Dhayal	Ms Skanda	Ms Sameera	Mr Zubair
Experiments	coe16d001@iiitdm.ac.in	edm17d002@iiitdm.ac.in	edm17d001@iiitdm.ac.in	coe18d002@iiitdm.ac.in	coe20d003@iiitdm.ac.in
Exp7	XILINX Design Flow practice- Modeling 8-bit parity generator circuit on target fpga. Model parity generator circuit in verilog HDL	XILINX Design Flow practice- Modeling 8-bit parity generator circuit on target fpga. Model parity generator circuit in verilog HDL	XILINX Design Flow practice- Modeling 8-bit parity generator circuit on target fpga. Model parity generator circuit in verilog HDL	XILINX Design Flow practice- Modeling 8-bit parity generator circuit on target fpga. Model parity generator circuit in verilog HDL	XILINX Design Flow practice- Modeling 8-bit parity generator circuit on target fpga. Model parity generator circuit in verilog HDL