Unique Gate Bias Dependence of Dynamic ON-Resistance in MIS-Gated AlGaN/GaN HEMTs and Its Dependence on Gate Control Over the 2-DEG

Sayak Dutta Gupta, *Graduate Student Member, IEEE*, Vipin Joshi, Rajarshi Roy Chaudhuri, *Graduate Student Member, IEEE*, and Mayank Shrivastava, *Senior Member, IEEE*

***Abstract*— This work reports a unique gate bias dependence of dynamic ON-resistance in metal–insulator–semiconductor (MIS)-gated AlGaN/GaN high-electron-mobility transistors (HEMTs). The absence of such dependence in Schottky HEMTs confirms that the phenomenon is unique to MISHEMTs. Based on the observations, the weakening of gate control over GaN channel by the insertion of the gate insulator is proposed as the phenomenon responsible for the observed behavior. The proposal is verified by incorporating high-κ (25) $Al_{0.5}Ti_{0.5}O_y$ as the gate oxide, which successfully mitigated the gate bias dependence of dynamic ON-resistance by improving the gate control.**

***Index Terms*— AlGaN/GaN high-electron-mobility transistors (HEMTs), AlTiO, dynamic ON-resistance, high-κ oxide, metal–insulator–semiconductor HEMTs (MISHEMTs).**

I. Introduction

DYNAMIC ON-resistance (dynamic R_{ON}) is one of the major challenges encountered by the promising AlGaN/GaN high-electron-mobility transistor (HEMT) technology for power applications [1]–[22]. The increase in HEMT's R_{ON} after HEMT either experiencing a high drain voltage stress (in OFF-state) or after undergoing switching cycles is referred to as dynamic R_{ON}. This OFF-state stressing-induced increase in R_{ON} has been attributed to charge trapping at the surface [1]–[7] as well as GaN buffer [8]–[20]. Development of novel surface passivation techniques, such as AlN [1], [2], SiN_x [3], GaN cap [4], NH_3 plasma pretreatment [5], has been able to mitigate any impact of surface traps on the device performance. On the other hand, buffer design to resolve dynamic R_{ON} degradation in GaN HEMTs is still a major design challenge [8]–[14]. Furthermore, the requirement of carbon-doping (C-doping) in GaN buffer, which is to enhance the buffer breakdown voltage [23], makes the device engineering rather complex due to introduced traps in the C-doped GaN buffer [24]. This further affects the dynamic performance of HEMTs by participating in electron capture [15], [16] or hole emission processes [17], [18]. Physical insights into different processes affecting dynamic R_{ON} is therefore necessary to address this device design challenge.

In this context, our recent work revealed an OFF-state stress time and device design-dependent critical drain voltage ($V_{DS\text{-}Stress} = V_{cr}$), beyond which dynamic R_{ON} of the devices increased considerably [15], [16]. Observed V_{cr} was found to be dependent on carrier trapping in the C-doped GaN buffer [15], [16]. While the impact of OFF-state drain stress voltage was discussed in detail in these works, any impact of gate bias conditions was not discussed. Previous studies on gate bias dependence of dynamic R_{ON} were limited to lower stress voltages (~50 V) and shorter stress times (few μs) [20]–[22]. Given our recent studies showing peculiar dynamic R_{ON} behavior under higher voltage and longer stress times [15], [16], it is imperative to extend it to study the influence of gate bias. In this work, we report a unique OFF-state gate bias ($V_{GS\text{-}Stress}$) dependence of dynamic R_{ON} and V_{cr} in AlGaN/GaN metal–insulator–semiconductor (MIS) HEMTs. The observed phenomenon is absent in Schottky-gated devices, indicating it to be unique to MISHEMTs. This study thus presents an additional design challenge for developing reliable AlGaN/GaN MISHEMTs, which have gained significant prominence due to lower gate leakage offered by these devices. Through detailed experiments and simulations, the observed $V_{GS\text{-}Stress}$ dependence is proposed to be related to gate control over 2-D electron gas (2-DEG), which is validated by demonstrating mitigation of the observed phenomenon by using high-κ $Al_{0.5}Ti_{0.5}O_y$ as gate oxide.

II. Device Fabrication and Experimentation

AlGaN/GaN HEMTs, as seen in Fig. 1(a) and (b), were fabricated on a 6″ commercial-grade C-doped GaN

Manuscript received December 28, 2021; revised January 13, 2022; accepted January 15, 2022. Date of publication January 31, 2022; date of current version February 24, 2022. This work was supported by the Department of Science and Technology (DST), Government of India, under their Core Research Grant (CRG) and Advanced Manufacturing Technology (AMT) Programs. The review of this brief was arranged by Editor K. Alam. *(Sayak Dutta Gupta and Vipin Joshi contributed equally to this work.) (Corresponding author: Sayak Dutta Gupta.)*

The authors are with the Department of Electronic Systems Engineering, Indian Institute of Science, Bengaluru 560012, India (e-mail: sayakgupta@iisc.ac.in; mayank@iisc.ac.in).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2022.3144378.

Digital Object Identifier 10.1109/TED.2022.3144378

0018-9383 © 2022 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See https://www.ieee.org/publications/rights/index.html for more information.

Authorized licensed use limited to: GITAM University. Downloaded on July 25,2022 at 13:15:31 UTC from IEEE Xplore. Restrictions apply.

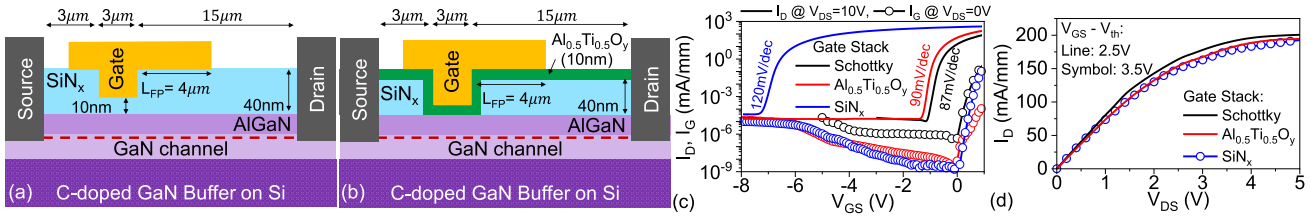

Fig. 1. Schematic of (a) SiN_x-gated and (b) $Al_{0.5}Ti_{0.5}O_y$-gated AlGaN/GaN MISHEMTs on carbon-doped GaN buffer, fabricated for this work. (c) Transfer ($I_D - V_{GS}$), gate leakage ($I_G - V_{GS}$), and (d) output ($I_D - V_{DS}$) characteristics of the fabricated HEMTs. A higher gate overdrive was provided for the $I_D - V_{DS}$ characteristics of the SiN_x-gated MISHEMTs to ensure similar ON-resistance, despite their weaker gate control.

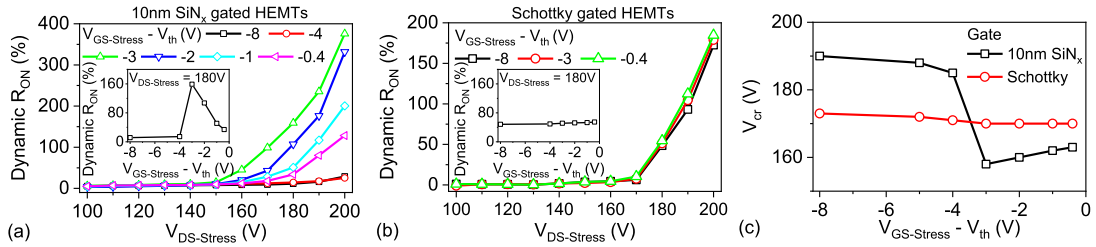

Fig. 2. Dependence of dynamic R_{ON} on $V_{DS\text{-}Stress}$ for GaN HEMTs with (a) SiN_x and (b) Schottky gate, as a function of $V_{GS\text{-}Stress}$. Inset in the figures shows the dependence of dynamic R_{ON} on $V_{GS\text{-}Stress}$ for a constant $V_{DS\text{-}Stress}$ of 180 V. (c) Impact of OFF-state gate bias condition ($V_{GS\text{-}Stress}$) on critical voltage ($V_{DS\text{-}Stress} = V_{cr}$) for SiN_x– and Schottky-gated GaN HEMTs.

on Si epi-stack (650 V Class) using a well-optimized process [15], [16], [25]. Three device variants were fabricated on the same epi-stack, viz. (a) Schottky-gated HEMTs, (b) MISHEMTs with 10-nm SiN_x gate [see Fig. 1(a)], and Fig. 1(c) MISHEMTs with 10-nm $Al_{0.5}Ti_{0.5}O_y$ (AlTiO) gate [see Fig. 1(b)]. The well-optimized processes [15], [16], [25] ensured superior surface quality of the HEMTs. The transfer, gate leakage, and output characteristics of the fabricated devices are shown in Fig. 1(c) and (d), respectively. The HEMTs show high ON-current, low R_{ON}, and high ON to OFF ratio, irrespective of the gate-stack. The threshold voltage (V_{th}) of the Schottky-, SiN_x-, and AlTiO-gated HEMTs were −0.9, −7, and −1.1 V, respectively, V_{th} being defined as the V_{GS} for I_D of 1 μA/mm. While proper surface cleaning before deposition of the Schottky gate resulted in the low V_{th} of the Schottky HEMTs [15], use of high-κ ($\kappa\sim25$), and p-type AlTiO as gate oxide led to V_{th} of −1.1 V for these devices [16], [25], [26]. Moreover, the significantly negative V_{th} of −7 V for the SiN_x-gated HEMTs can be attributed to reduced channel control due to the use of 10-nm-thick low-κ ($\kappa\sim5$) SiN_x as the gate dielectric [16].

The HEMTs were subjected to a measure-stress-measure-relax cycle, with substrate grounded, to evaluate dynamic R_{ON} [14]–[16]. After pristine R_{ON} ($R_{Pristine}$) measurement, devices were subjected to an OFF-state stress for 100 μs. Immediately after the stress, post-stress R_{ON} ($R_{Post\text{-}Stress}$) was measured to evaluate dynamic R_{ON} of the device as: $\text{Dynamic}R_{ON} = (R_{Post\text{-}Stress} - R_{Pristine})/R_{Pristine} \times 100\%$. Here, R_{ON} is calculated from the inverse slope of the output characteristics for V_{DS} ranging from 0.25 to 0.5 V. Devices were also allowed to relax for ∼180 s in between two stress cycles, to completely recover to the pristine condition.

III. Experimental Observations and Discussion

A. Impact of OFF-State Stress Conditions on Dynamic R_{ON}

Fig. 2(a) depicts the impact of $V_{DS\text{-}Stress}$ and $V_{GS\text{-}Stress}$ on the dynamic R_{ON} performance of the SiN_x-gated HEMTs.

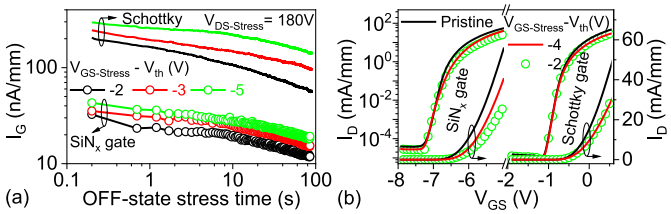

Fig. 3. (a) Gate leakage with OFF-state stress time of the SiN_x-gated and Schottky HEMTs, as a function of $V_{GS\text{-}Stress}$. (b) $I_D - V_{GS}$ sweeps at V_{DS} = 10 V, of SiN_x-gated and Schottky HEMTs, measured immediately after $V_{DS\text{-}Stress}$ of 180 V, as a function of $V_{GS\text{-}Stress}$. The measurements were done under dark conditions with V_{GS} swept from positive to negative.

Devices show a V_{cr} beyond which dynamic R_{ON} degrades significantly. Moreover, the value of dynamic R_{ON} [depicted in the inset of Fig. 2(a)] and V_{cr} are observed to be significantly dependent on the value of $V_{GS\text{-}Stress}$. On the other hand, V_{cr} and dynamic R_{ON} are found to be independent of $V_{GS\text{-}Stress}$ for Schottky HEMTs, as seen in Fig. 2(b). This dependence of V_{cr} on $V_{GS\text{-}Stress}$ is further highlighted in Fig. 2(c). Unlike the Schottky HEMT, V_{cr} of the SiN_x-gated HEMT reduced from ∼190 to ∼150 V, when $V_{GS\text{-}Stress}$ was marginally reduced from $V_{th} - 4$ V to $V_{th} - 3$ V. Any increase or decrease in $V_{GS\text{-}Stress}$ from these bias points results in a marginal increase in V_{cr}. It is worth highlighting here that though the gate bias was varied, it was ensured that the device remained in OFF-state by keeping $V_{GS\text{-}Stress} < V_{th}$. Above observations make determining operating conditions and performance of MISHEMTs a strong function of gate bias conditions.

B. Source of $V_{GS\text{-}Stress}$ Dependence

The SiN_x and Schottky-gated devices, discussed in Fig. 2, were processed simultaneously on the same GaN buffer stack and similar SiN_x passivation, with the only difference in gate-stack. This establishes the observed dependence on $V_{GS\text{-}Stress}$ to be a gate-stack-dependent phenomenon. MIS gate-stack affects three major device parameters, (a) gate leakage, (b) V_{th} modulation due to traps in the gate-stack, and (c) gate's control over the 2-DEG.

Authorized licensed use limited to: GITAM University. Downloaded on July 25,2022 at 13:15:31 UTC from IEEE Xplore. Restrictions apply.

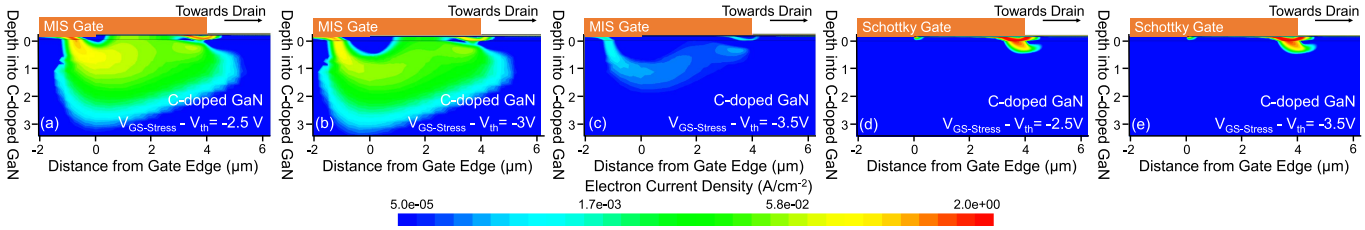

Fig. 4. Electron current density extracted in SiN_x-gated HEMTs at a $V_{GS\text{-}Stress} - V_{th}$ of (a) −2.5 V, (b) −3 V, (c) −3.5 V, and in Schottky HEMTs at a $V_{GS\text{-}Stress} - V_{th}$ of (d) −2.5 V, and (e) −3.5 V. A $V_{DS\text{-}Stress}$ of 200 V was taken with $L_{GD} = 15$ μm, $L_{FP} = 4$ μm, and 40 nm SiN_x passivation.

Fig. 1(c) shows the gate leakage of the SiN_x-gated HEMTs to be significantly lower than the Schottky HEMTs due to the presence of the gate dielectric. If gate leakage is considered to play a major role in determining the dynamic R_{ON} performance of the GaN HEMTs, a lower gate leakage should reduce the dynamic R_{ON} of MISHEMTs. However, the phenomenon as depicted in Fig. 2(c) is observed only in MIS-gated devices (with lower gate leakage) but is absent in Schottky devices (with comparatively higher gate leakage). This suggests that gate leakage plays a minimal role in determining the unique gate bias-dependent dynamic R_{ON} in the MISHEMTs. It is also worth highlighting that when $V_{GS\text{-}Stress}$ was increased in the negative direction, the gate current increased monotonously for both SiN_x- and Schottky HEMTs, as shown in Fig. 3(a). On the other hand, V_{cr} and dynamic R_{ON} of the SiN_x-gated MISHEMTs showed a different dependence on $V_{GS\text{-}Stress}$ [see Fig. 2(a) and (c)], wherein V_{cr} initially reduced, showed a considerable increase and then remained constant as $V_{GS\text{-}Stress}$ was reduced below V_{th}. This observation further validates that the mechanism responsible for $V_{GS\text{-}Stress}$ dependence of dynamic R_{ON} is not attributed to gate leakage. Furthermore, it should also be noted that no V_{th} shift was observed for these devices, immediately after $V_{DS\text{-}Stress}$ of 180 V for different $V_{GS\text{-}Stress}$ values, as shown in Fig. 3(b). This indicates negligible trapping at the gate insulator–semiconductor interface or the gate-stack, which would otherwise result in an observable V_{th} shift. Therefore, the observed phenomenon can also not be attributed to trapping at the gate insulator–semiconductor interface or the gate-stack. This further indicates trapping in the access region as the source of dynamic R_{ON} degradation in these devices.

To investigate the third aspect, that is, the role of gate control modulation due to dielectric insertion, Fig. 4(a)–(c) compare the simulated source–drain leakage path for SiN_x-gated devices with different $V_{GS\text{-}Stress}$. Fig. 4(a) and (b) shows that the leakage path extends deeper into the C-doped GaN buffer as $V_{GS\text{-}Stress}$ is reduced below V_{th}. This exposes a larger concentration of C-doping-induced traps to the injected carriers. This in turn leads to a higher dynamic R_{ON} with reduced V_{cr}, as seen experimentally for $V_{GS\text{-}Stress} - V_{th} \geq -3$ V [see Fig. 2(c)]. On the other hand, Fig. 4(c) shows a significant reduction in electron current density, as the electron current path follows a longer trajectory in C-doped GaN buffer, when $V_{GS-Stress}$ was lowered further. This reduces the carrier injection and hence carrier trapping in the GaN buffer, which in turn results in lower dynamic R_{ON} and higher V_{cr} as seen experimentally for $V_{GS\text{-}Stress} - V_{th} \leq -4$ V in Fig. 2(c).

To investigate how this carrier injection into the GaN buffer is affected by the gate's control over the 2-DEG,

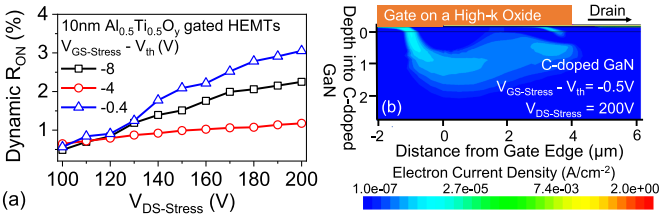

Fig. 5. (a) Dynamic R_{ON} characteristics of $Al_{0.5}Ti_{0.5}O_y$-gated HEMTs as a function of $V_{GS\text{-}Stress}$ and $V_{DS\text{-}Stress}$. (b) Electron current density extracted in high-κ ($\kappa = 25$)-gated HEMTs at $V_{GS\text{-}Stress} - V_{th}$ of −0.5 V. The only difference in the device was the gate dielectric's κ value.

Schottky-gated devices were analyzed. Fig. 1(c) shows better gate control in Schottky HEMTs (subthreshold slope (SS) = 87 mV/dec), when compared with SiN_x-gated HEMTs (SS = 120 mV/dec). Simulated electron current density for Schottky HEMTs, as shown in Fig. 4(d), shows that the improved gate control effectively suppresses the source–drain leakage path for Schottky HEMTs. However, electron injection into the C-doped GaN buffer now occurs near the field plate (FP) edge due to significant gate leakage current observed in the Schottky devices. This leads to dynamic R_{ON} in Schottky HEMTs with a V_{cr}, as seen in Fig 2(b). However, given the leakage path in the C-doped GaN buffer originates near the FP edge, it is not affected by gate control and is independent of $V_{GS\text{-}Stress}$, as seen in Fig. 4(d) and (e). This explains the $V_{GS\text{-}Stress}$ independence of V_{cr} in Schottky HEMTs, as seen in Fig. 2(b).

The above discussion indicates weaker gate control in MISHEMTs to be responsible for the observed $V_{GS\text{-}Stress}$ dependence of dynamic R_{ON}. To validate the proposed phenomenon AlTiO-gated ($\kappa = 25$) [25] devices, as shown in Fig. 1(b), were fabricated. The AlTiO-gated devices, with an SS of 90 mV/dec, demonstrated a gate control similar to that of Schottky HEMTs, as seen in Fig. 1(c), and resulted in $V_{GS\text{-}Stress}$ independent dynamic R_{ON}, as seen in Fig. 5(a). The simulated leakage current path for GaN HEMTs with a high-κ ($\kappa = 25$) gate oxide is shown in Fig. 5(b). It establishes a significant reduction in source–drain leakage through C-doped GaN buffer for devices with a high-κ gate oxide, even for a lower $V_{GS\text{-}Stress} - V_{th}$. The improved gate control [see Fig. 1(c)] and associated reduction in leakage current [see Fig. 5(b)] results in $V_{GS\text{-}Stress}$ independence of dynamic R_{ON} in high-κ AlTiO-gated GaN MISHEMTs, as seen in Fig. 5(a). The above discussions thus establish degraded channel control, due to incorporation of gate dielectric, to result in a $V_{GS\text{-}Stress}$-dependent dynamic R_{ON} in AlGaN/GaN MISHEMTs.

IV. Conclusion

This work reports a unique gate bias-dependent critical OFF-state drain stress voltage, beyond which dynamic R_{ON}

Authorized licensed use limited to: GITAM University. Downloaded on July 25,2022 at 13:15:31 UTC from IEEE Xplore. Restrictions apply.

of AlGaN/GaN MISHEMTs on C-doped buffer degrades significantly. Experiments were conducted on Schottky-gated and MIS-gated HEMTs; both realized using the same epi-stack and passivation. Schottky-gated HEMTs reveal the critical voltage in dynamic R_{ON} to be independent of gate bias condition. The same, however, was a strong function of gate bias in the case of MIS-gated devices. This unique dependence is caused by reduced gate control in MIS-gated devices, which modifies the source–drain leakage path through the GaN buffer. This, in turn, modulates carrier injection into the C-doped GaN buffer leading to gate bias-dependent dynamic R_{ON}. The proposed phenomenon is further validated using high-κ $Al_{0.5}Ti_{0.5}O_y$ gate oxide-based HEMTs, which relaxed the dependence of dynamic R_{ON} on the gate bias conditions due to superior channel control. This study thus establishes gate bias conditions and channel control to play a major role in determining the dynamic R_{ON} of AlGaN/GaN MISHEMTs.

Acknowledgment

The authors would like to acknowledge the National Nanofabrication Center (NNFC) at the Indian Institute of Science, Bengaluru, funded by MeitY and DST, Government of India. Besides, Sayak Dutta Gupta and Rajarshi Roy Chaudhuri would also like to thank DST INSPIRE for their fellowship.

References

[1] Z. Tang, S. Huang, Q. Jiang, S. Liu, C. Liu, and K. J. Chen, "High-voltage (600-V) low-leakage low-current-collapse AlGaN/GaN HEMTs with AlN/SiNx passivation," *IEEE Electron Device Lett.*, vol. 34, no. 3, pp. 366–368, Mar. 2013, doi: 10.1109/LED.2012.2236638.

[2] Z. Tang, S. Huang, X. Tang, B. Li, and K. J. Chen, "Influence of AlN passivation on dynamic ON-resistance and electric field distribution in high-voltage AlGaN/GaN-on-Si HEMTs," *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2785–2792, Aug. 2014, doi: 10.1109/TED.2014.2333063.

[3] A. D. Koehler *et al.*, "Impact of surface passivation on the dynamic on-resistance of proton-irradiated AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 545–548, May 2016, doi: 10.1109/LED.2016.2537050.

[4] G.-Y. Lee, P.-T. Tu, and J.-I. Chyi, "Improving the off-state characteristics and dynamic on-resistance of AlInN/AlN/GaN HEMTs with a GaN cap layer," *Appl. Phys. Exp.*, vol. 8, no. 6, Jun. 2015, Art. no. 064102, doi: 10.7567/APEX.8.064102.

[5] A. P. Edwards, J. A. Mittereder, S. C. Binari, D. S. Katzer, D. F. Storm, and J. A. Roussos, "Improved reliability of AlGaN-GaN HEMTs using an NH_3 plasma treatment prior to SiN passivation," *IEEE Electron Device Lett.*, vol. 26, no. 4, pp. 225–227, Apr. 2005, doi: 10.1109/LED.2005.844694.

[6] P.-C. Chou, T.-E. Hsieh, S. Cheng, J. A. del Alamo, and E. Y. Chang, "Comprehensive dynamic on-resistance assessments in GaN-on-Si MIS-HEMTs for power switching applications," *Semicond. Sci. Technol.*, vol. 33, no. 5, Apr. 2018, Art. no. 055012, doi: 10.1088/1361-6641/aabb6a.

[7] D. Jin and J. A. D. Alamo, "Methodology for the study of dynamic ON-resistance in high-voltage GaN field-effect transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3190–3196, Oct. 2013, doi: 10.1109/TED.2013.2274477.

[8] G. Verzellesi *et al.*, "Influence of buffer carbon doping on pulse and AC behavior of insulated-gate field-plated power AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 443–445, Apr. 2014, doi: 10.1109/LED.2014.2304680.

[9] M. J. Uren *et al.*, "'Leaky dielectric' model for the suppression of dynamic R_{ON} in carbon-doped AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 64, no. 7, pp. 2826–2834, Jul. 2017, doi: 10.1109/TED.2017.2706090.

[10] H.-S. Kang, C.-H. Won, Y.-J. Kim, D.-S. Kim, Y. J. Yoon, I. M. Kang, Y. S. Lee, and J.-H. Lee, "Suppression of current collapse in AlGaN/GaN MISHFET with carbon- doped GaN/undoped GaN multi-layered buffer structure," *Phys. Status Solidi A*, vol. 212, no. 5, pp. 1116–1121, 2015, doi: 10.1002/pssa.201431668.

[11] V. Joshi, S. P. Tiwari, and M. Shrivastava, "Part I: Physical insight into carbon-doping-induced delayed avalanche action in GaN buffer in alGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 561–569, Jan. 2019, doi: 10.1109/TED.2018.2878770.

[12] V. Joshi, S. P. Tiwari, and M. Shrivastava, "Part II: Proposals to independently engineer donor and acceptor trap concentrations in GaN buffer for ultrahigh breakdown AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 570–577, Jan. 2019, doi: 10.1109/TED.2018.2878787.

[13] Y. Saito, R. Tsurumaki, N. Noda, and K. Horio, "Analysis of reduction in lag phenomena and current collapse in field-plate AlGaN/GaN HEMTs with high acceptor density in a buffer layer," *IEEE Trans. Device Mater. Rel.*, vol. 18, no. 1, pp. 46–53, Mar. 2018, doi: 10.1109/TDMR.2017.2779429.

[14] W. M. Waller, M. Gajda, S. Pandey, J. J. T. M. Donkers, D. Calton, J. Croon, J. Šonský, M. J. Uren, and M. Kuball, "Control of buffer-induced current collapse in AlGaN/GaN HEMTs using SiNx deposition," *IEEE Trans. Electron Devices*, vol. 64, no. 10, pp. 4044–4049, Oct. 2017, doi: 10.1109/TED.2017.2738669.

[15] S. D. Gupta, V. Joshi, R. R. Chaudhuri, and M. Shrivastava, "Part I: Physical insights into dynamic R_{ON} behavior and a unique time-dependent critical stress voltage in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 11, pp. 5720–5727, Nov. 2021, doi: 10.1109/TED.2021.3109847.

[16] S. D. Gupta, V. Joshi, R. R. Chaudhuri, and M. Shrivastava, "Novel surface passivation scheme by using p-type AlTiO to mitigate dynamic ON resistance behavior in AlGaN/GaN HEMTs—Part II," *IEEE Trans. Electron Devices*, vol. 68, no. 11, pp. 5728–5735, Nov. 2021, doi: 10.1109/TED.2021.3064531.

[17] N. Zagni *et al.*, "'Hole redistribution' model explaining the thermally activated R_{ON} stress/recovery transients in carbon-doped AlGaN/GaN power MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 2, pp. 697–703, Feb. 2021, doi: 10.1109/TED.2020.3045683.

[18] A. Chini *et al.*, "Experimental and numerical analysis of hole emission process from carbon-related traps in GaN buffer layers," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3473–3478, Sep. 2016, doi: 10.1109/TED.2016.2593791.

[19] C. Tang and J. Shi, "Influence of acceptor-like traps in the buffer on current collapse and leakage of E-mode AlGaN/GaN MISHFETs," *Semicond. Sci. Technol.*, vol. 28, no. 11, Oct. 2013, Art. no. 115011, doi: 10.1088/0268-1242/28/11/115011.

[20] M. Meneghini *et al.*, "Buffer traps in Fe-doped AlGaN/GaN HEMTs: Investigation of the physical properties based on pulsed and transient measurements," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 4070–4077, Dec. 2014, doi: 10.1109/TED.2014.2364855.

[21] M. Wang *et al.*, "Investigation of surface- and buffer-induced current collapse in GaN high-electron mobility transistors using a soft switched pulsed $(I - V)$ measurement," *IEEE Electron Device Lett.*, vol. 35, no. 11, pp. 1094–1096, Nov. 2014, doi: 10.1109/LED.2014.2356720.

[22] M. Meneghini *et al.*, "Trapping in GaN-based metal-insulator-semiconductor transistors: Role of high drain bias and hot electrons," *Appl. Phys. Lett.*, vol. 104, no. 14, Apr. 2014, Art. no. 143505, doi: 10.1063/1.4869680.

[23] E. Bahat-Treidel, F. Brunner, O. Hilt, E. Cho, J. Wurfl, and G. Trankle, "AlGaN/GaN/GaN:C back-barrier HFETs with breakdown voltage of over 1 kV and low $R_{ON} \times A$," *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 3050–3058, Nov. 2010, doi: 10.1109/TED.2010.2069566.

[24] J. L. Lyons, A. Janotti, and C. G. Van de Walle, "Effects of carbon on the electrical and optical properties of InN, GaN, and AlN," *Phys. Rev. B, Condens. Matter*, vol. 89, no. 3, Jan. 2014, Art. no. 035204, doi: 10.1103/PhysRevB.89.035204.

[25] S. D. Gupta *et al.*, "Positive threshold voltage shift in AlGaN/GaN HEMTs and e-mode operation by al_xti_{1-x} o based gate stack engineering," *IEEE Trans. Electron Devices*, vol. 66, no. 6, pp. 2544–2550, Jun. 2019, doi: 10.1109/TED.2019.2908960.

[26] S. D. Gupta, V. Joshi, R. R. Chaudhuri, and M. Shrivastava, "Observations regarding deep-level states causing p-type doping in AlTiO gate and positive threshold voltage shift in AlGaN/GaN high electron mobility transistors," *J. Appl. Phys.*, vol. 130, no. 1, Jul. 2021, Art. no. 015701, doi: 10.1063/5.0053982.

Authorized licensed use limited to: GITAM University. Downloaded on July 25,2022 at 13:15:31 UTC from IEEE Xplore. Restrictions apply.