LM74610-Q1 Zero IQ Reverse Polarity Protection Smart Diode Controller

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Exceeds HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Maximum reverse voltage of 45 V
- No Positive Voltage limitation to Anode Terminal
- Charge Pump Gate Driver for External N-Channel MOSFET
- Lower Power Dissipation than Schottky Diode/PFET Solutions
- Low Reverse Leakage Current
- Zero IQ
- Fast 2-µs Response to Reverse Polarity
- -40°C to +125°C Operating Ambient Temperature
- Can be Used in OR-ing Applications
- Meets CISPR25 EMI Specification
- Meets Automotive ISO7637 Transient Requirements with a Suitable TVS Diode
- No Peak Current Limit

2 Applications

- ADAS
- Infotainment Systems
- Power Tools (Industrial)
- Transmission Control Unit (TCU)
- Battery OR-ing Applications

3 Description

The LM74610-Q1 is a controller device that can be used with an N-Channel MOSFET in a reverse polarity protection circuitry. It is designed to drive an external MOSFET to emulate an ideal diode rectifier when connected in series with a power source. A unique advantage of this scheme is that it is not referenced to ground and thus has Zero Iq.

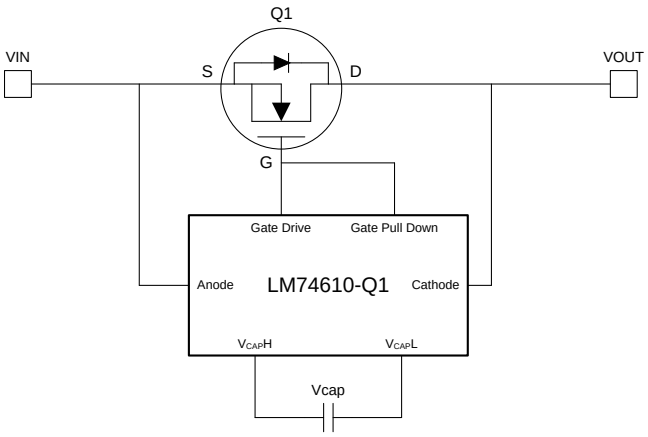
The LM74610-Q1 controller provides a gate drive for an external N-Channel MOSFET and a fast response internal comparator to discharge the MOSFET Gate in the event of reverse polarity. This fast pull-down feature limits the amount and duration of reverse current flow if opposite polarity is sensed. The device design also meets CISPR25 Class 5 EMI specifications and automotive ISO7637 transient requirements with a suitable TVS diode.

Device Information(1)

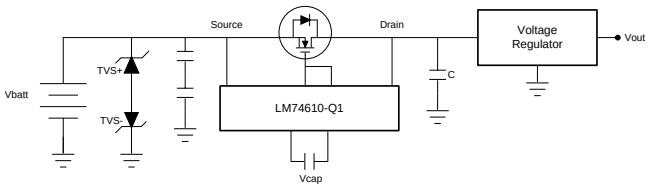
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM74610-Q1	VSSOP (8)	3.00 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Smart Diode Configuration



Application Diagram



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Changes from Revision A (October 2015) to Revision B **Page**

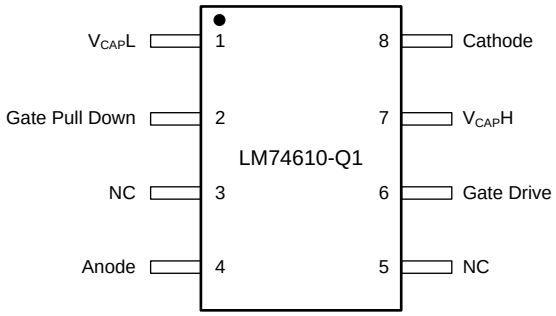
- Added *No Peak Current Limit* to *Description* ... 1
- Added *Simplified Application Diagram* to page 1 ... 1
- Added *Voltage Across Body Diode vs Vcap Charging Current* to *Typical Characteristics* ... 7
- Updated *Gate Drive Pin* ... 10
- Corrected *Startup Relative to VIN* figure ... 15
- Corrected typo of *revere* to *reverse* in *Response to Reverse Polarity* ... 15
- Updated *Layout Guidelines* ... 22

Changes from Original (July 2015) to Revision A **Page**

- Product Preview to Production Data Release ... 1

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	VcapL	Charge Pump Output, connect to an external charge pump capacitor
2	Gate Pull Down	Connect to the gate of the external MOSFET for fast turn OFF in the case of reverse polarity
3	NC	No connect. Leave floating or connect to Anode pin
4	Anode	Anode of the diode, connect to source of the external MOSFET
5	NC	No connect. Leave floating or connect to gate drive pin
6	Gate Drive	Gate Drive output, Connect to the Gate of the external MOSFET
7	VcapH	Charge Pump Output, connect to an external charge pump capacitor
8	Cathode	Cathode of the diode, connect to Drain of the external MOSFET

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Cathode to Anode (for a 2-ms time duration) (2), (3)	-3	45	V
Cathode to Anode (continuous)(3)	-3	42	V
VcapH to VcapL	-0.3	7	V
Anode to VcapL	-0.3	3	V
Gate drive, gate pull down to VcapL	-0.3	7	V
Ambient temperature, TA-MAX(4)	-40	125	°C
Case temperature, TC-MAX	-40	125	°C
Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) 42V continuous (and 45V transients for 2ms) absmax condition from Cathode to Anode. Suitable to use with TVS SMBJ28A and SMBJ14A at the anode.
(3) Reverse voltage rating only. There is no positive voltage limitation for the LM74610-Q1 Anode terminal.
(4) The device performance is ensured over this Ambient Temperature range as long the Case Temperature does not exceed the MAX value.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human body model (HBM), per AEC Q100-002(2)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Cathode To Anode			42	V
Ambient temperature, TA-MAX	-40		125	°C
Case temperature, TC-MAX			125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM74610-Q1 VSSOP (DGK) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	181	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	102	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11	°C/W
ψ_{JB}	Junction-to-board characterization parameter	100	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A= 25°C unless otherwise noted. Minimum and maximum limits are specified through test, design, validation or statistical correlation. Typical values represent the most likely parametric norm at T_A= 25°C and are provided for reference purpose only. $V_{Anode\text{-}Cathode}$= 0.55 V for all tests.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{Anode\ to\ Cathode}$	Minimum startup voltage across external MOSFET's body diode	External MOSFET V_{GS} = 0V	0.48			V
$V_{cap\ Threshold}$	Charge pump capacitor drive thresholds	Vcap Upper Threshold		6.3		V
		Vcap Lower Threshold		5.15		V
$I_{Gate\ up}$	Gate drive pull up current	$V_{Gate\ to\ Anode}$ = 2 V	8.9	9.4		µA
$I_{Gate\ down}$	Gate drive pull down current during forward voltage	$V_{Gate\ to\ Anode}$ = 4 V	6.35	6.8		µA
$I_{Gate\ pull\ down}$	Gate drive pull down current when reverse voltage is sensed	$V_{Gate\ Pull\ Down}$ = V_{Anode} + 2 V		160		mA
$I_{Charge\ Current}$	Charging current for the charge pump capacitor	$V_{Anode\ to\ Cathode}$ = 0.55 V	40	46		µA
$I_{Discharge\ Current}$	VCAP current consumption to power the controller when MOSFET is ON	V_{cap} = 6.6 V		0.95		µA
$T_{Recovery}$	Time to shut off MOSFET when voltage is reversed (Equivalent to diode reverse recovery time)	$V_{Anode\ to\ Cathode}$ = -20 mV Cgate = 4 nF		2.2	5(2)	µs
D	Duty cycle	Iload = 3 A, T_A = 25°C		98%		
		Iload = 3 A, T_A = 125°C		92%		
I_{LKG}	Reverse leakage current	$V_{Anode\ to\ Cathode}$ = -13.5 V		60	110(2)	µA
Iq	Quiescent current to GND			0		µA
I_{Anode}	Current into Anode pin	Current into Anode pin when $V_{Anode\ -\ Cathode}$ = 0.3V.		30		µA

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the table of Electrical Characteristics.
(2) Limit applies over the full Operating Temperature Range T_A = -40°C to +125°C.

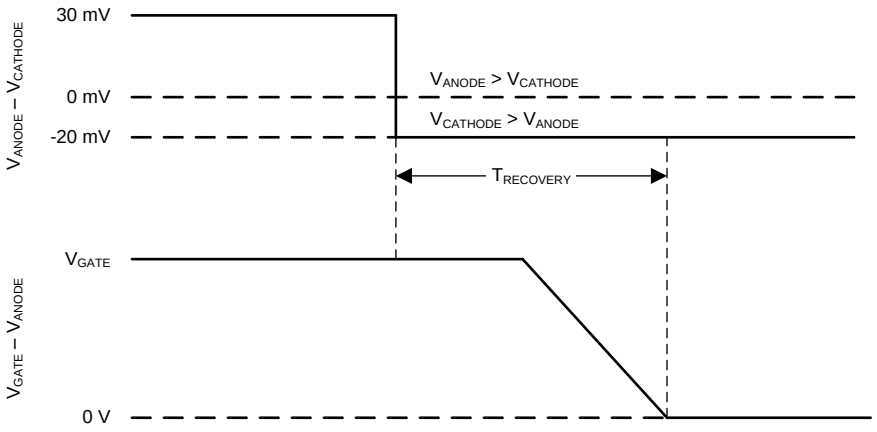


Figure 1. Gate Shut Down Timing in the Event of Reverse Polarity

6.6 Typical Characteristics

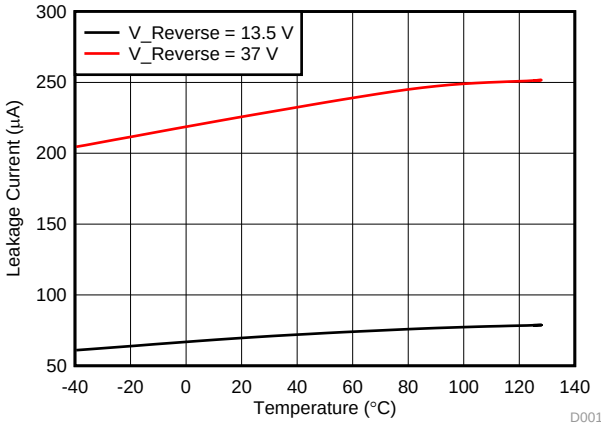


Figure 2. Reverse Leakage at Negative Voltages

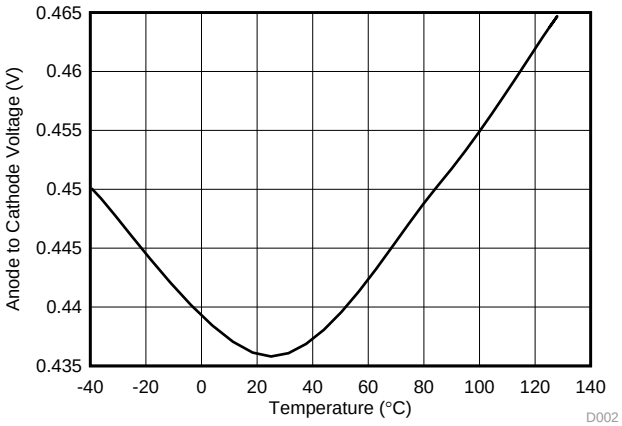


Figure 3. Anode to Cathode Startup Voltage

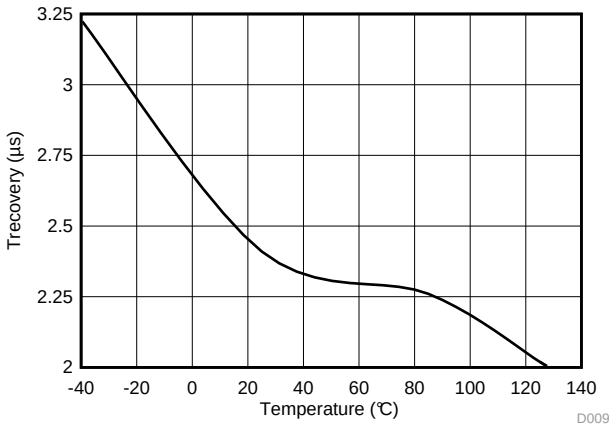


Figure 4. Reverse Recovery Time ($T_{Recovery}$)

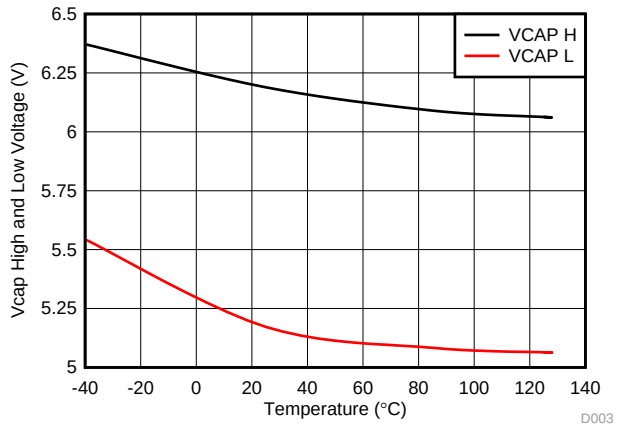


Figure 5. VcapH and VcapL Voltage Threshold

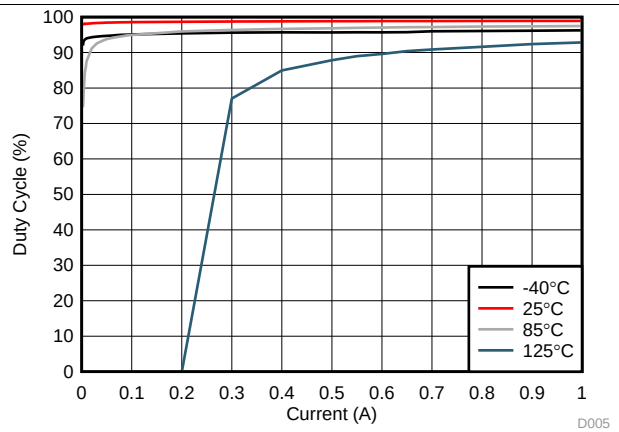


Figure 6. Duty Cycle of the Output Voltage at Startup

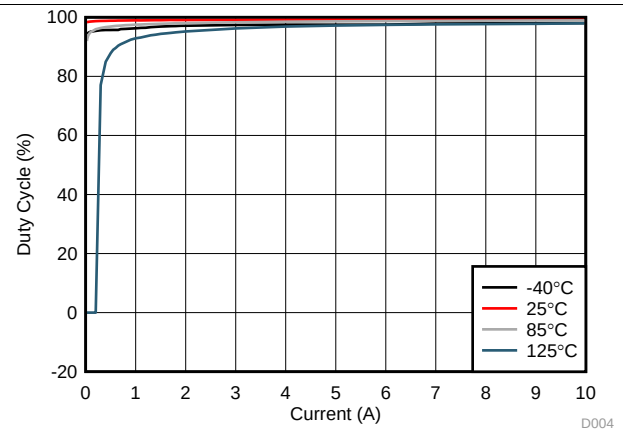


Figure 7. Duty Cycle of the Output Voltage

Typical Characteristics (continued)

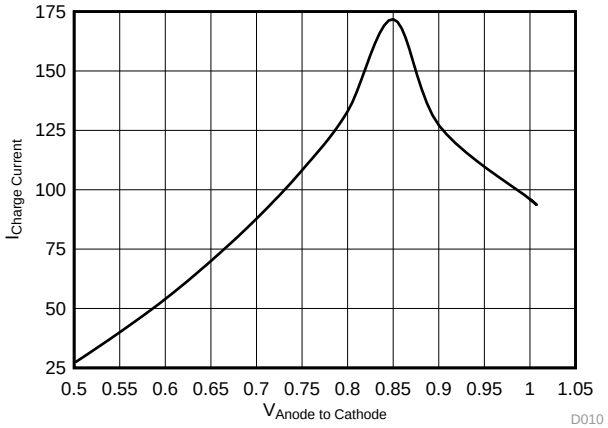


Figure 8. Voltage Across Body Diode vs Vcap Charging Current

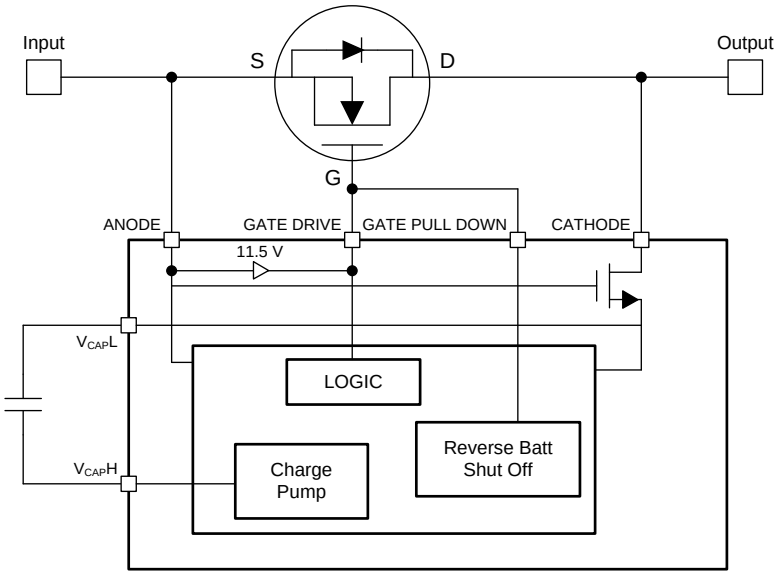
7 Detailed Description

7.1 Overview

Most systems in automotive or industrial applications require fast response reverse polarity protection at the input stage. Schottky diodes or P-Channel MOSFETs are typically used in most power systems to protect the load in the case of negative polarity. The main disadvantage of using diodes is voltage drop during forward conduction, which reduces the available voltage and increases the associated power losses. PFET solutions are inefficient for handling high load current at low input voltage.

The LM74610-Q1 is a zero Iq controller that is combined with an external N-channel MOSFET to replace a diode or PFET reverse polarity solution in power systems. The voltage across the MOSFET source and drain is constantly monitored by the LM74610-Q1 ANODE and CATHODE pins. An internal charge pump is used to provide the GATE drive for the external MOSFET. . This stored energy is used to drive the gate of MOSFET. The voltage drop depends on the R_{DSON} of a particular MOSFET in use, which is significantly smaller than a PFET. The LM74610-Q1 has no ground reference which makes it identical to a diode.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 During T0

When power is initially applied, the load current (I_D) will flow through the body diode of the MOSFET and produce a voltage drop (V_f) during T0 in Figure 9. This forward voltage drop (V_f) across the body diode of the MOSFET is used to charge up the charge pump capacitor Vcap. During this time, the charge pump capacitor Vcap is charged to a higher threshold of 6.3V (typical).

Feature Description (continued)

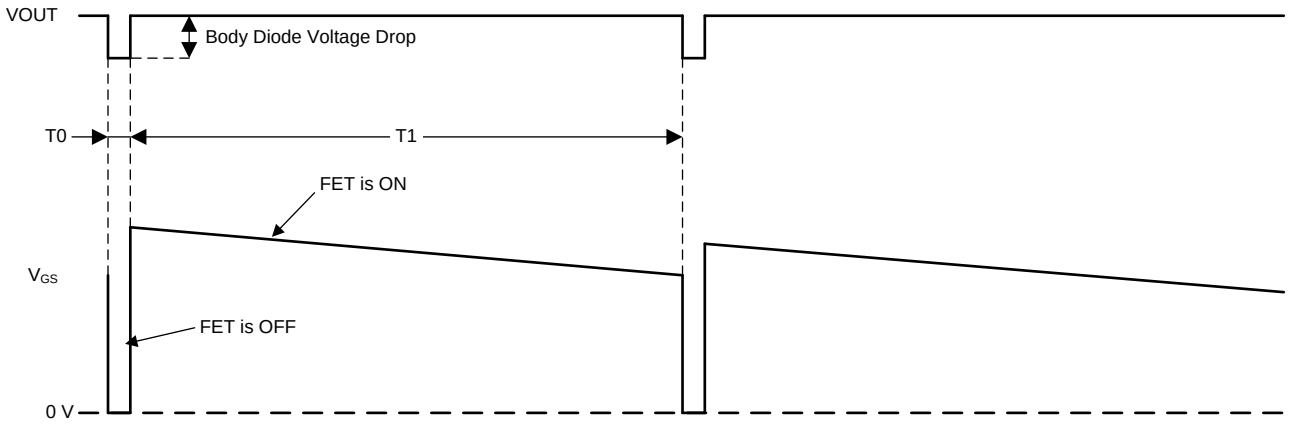


Figure 9. Output Voltage and V_{GS} Operation at 1A Output Current

7.3.2 During T1

Once the voltage on the capacitor reaches the higher voltage level of 6.3V (typical), the charge pump is disabled and the MOSFET turns ON. The energy stored in the capacitor is used to provide the gate drive for the MOSFET (T1 in Figure 9). When the MOSFET is ON, it provides a low resistive path for the drain current to flow and minimizes the power dissipation associated with forward conduction. The power losses during the MOSFET ON state depend primarily on the R_{DSON} of the selected MOSFET and load current. At the time when the capacitor voltage reaches its lower threshold VcapL 5.15V (typical), the MOSFET gate turns OFF. The drain current I_D will then begin to flow through the body diode of the MOSFET, causing the MOSFET body diode voltage drop to appear across Anode and Cathode pins. The charge pump circuitry is re-activated and begins charging the charge pump capacitor. The LM74610-Q1 operation keeps the MOSFET ON at approximately 98% duty cycle (typical) regardless of the external charge pump capacitor value. This is the key factor to minimizing the power losses. The forward voltage drop during this time is determined by the R_{DSON} of the MOSFET.

7.3.3 Pin Operation

7.3.3.1 Anode and Cathode Pins

The LM74610-Q1 Anode and Cathode pins are connected to the source and drain of the external MOSFET. The current into the Anode pin is 30 µA (typical). When power is initially applied, the load current flows through the body diode of the external MOSFET, the voltage across Anode and Cathode pins is equal to the forward diode drop (V_f). The minimum value of V_f required to enable the charge pump circuitry is 0.48V. Once the MOSFET is turned ON, the Anode and Cathode pins constantly sense the voltage difference across the MOSFET to determine the magnitude and polarity of the voltage across it. When the MOSFET is on, the voltage difference across Anode and Cathode pins depends on the R_{DSON} and load current. If voltage difference across source and drain of the external MOSFET becomes negative, this is sensed as a fault condition by Anode and Cathode pins and gate is turned off by Gate Pull Down pin as shown in Figure 1. The reverse voltage threshold across Anode and Cathode to detect the fault condition is -20 mV. The consistent sensing of voltage polarity across the MOSFET enables the LM74610-Q1 to provide a fast response to the power source failure and limit the amount and duration of the reverse current flow.

7.3.3.2 VcapH and VcapL Pins

VcapH and VcapL are high and low voltage thresholds respectively that the LM74610-Q1 uses to detect when to turn the charge pump circuitry ON and OFF. The capacitor charging and discharging time can be correlated to the duty cycle of the MOSFET gate. Figure 10 shows the voltage behavior across the Vcap. During the time period T0, the capacitor is storing energy from the charge pump. The MOSFET is turned off and current flow is only through the body diode during this time period. The conduction though body diode of the MOSFET is for a

Feature Description (continued)

very small period of time (2% typical) which rules out the chances of overheating the MOSFET, regardless of the output current. Once the capacitor voltage reaches its high threshold, the MOSFET is turned ON and charge pump circuity is deactivated until the Vcap reaches its lower voltage threshold again (T1). The voltage difference between Vcap high and low threshold is typically 1.15V. The LM74610-Q1 charge pump has 46µA charging capability with 5-8MHz frequency.

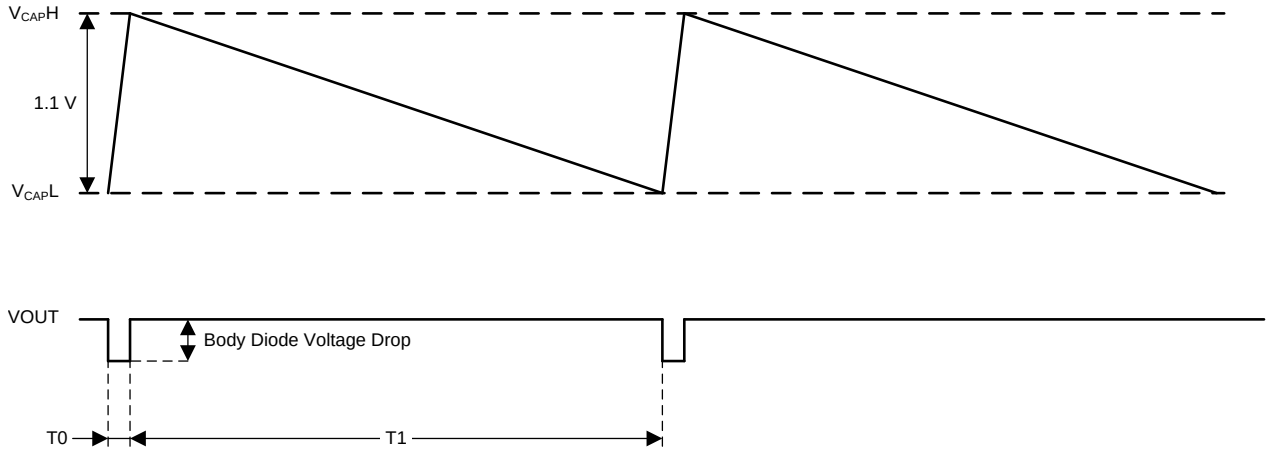


Figure 10. Vcap Charging and Discarding by the Charge Pump

The Vcap current consumption is 1 µA (typical) to drive the gate. The MOSFET OFF time (T0) and ON time (T1) can be calculated using the following expression

$$\Delta T = C\frac{dV}{dI} \quad (1)$$

Where:

- C = Vcap Capacitance
- dV = 1.15V
- dI = 46 µA for charging
- dI = 0.95 µA for discharging

Note: Temperature dependence of these parameters – The duty cycle is dependent on temperature since the capacitance variation over temperature has a direct correlation to the MOSFET OFF and ON periods and the frequency. If the capacitor varies 20% the periods and the frequency will also vary by 20% so it is recommended to use a quality X7R/COG cap and not to place the cap in close proximity to high temperature devices. The variation of the capacitor does not have a thermal impact in the application as the duty cycle does not change.

7.3.3.3 Gate Drive Pin

When the charge pump capacitor is charged to the high voltage level of 6.3 V (typical), the Gate Drive pin provides a 6.8 µA (typical) of drive current. When the charge pump capacitor reaches its lower voltage threshold of 5.15 V (typical), Gate is pulled down to the Anode voltage (Vin). During normal operation, the gate turns ON and OFF with a slow 2msec slew rate in order to avoid switching noise and EMI issues. To protect the gate of the MOSFET, a built-in internal 11.5V Zener clamp the maximum gate to source voltage ($V_{GS(MAX)}$).

7.3.3.4 Gate Pull Down Pin

The Gate Pull Down pin is connected to the Gate Drive pin in a typical application circuit. When the controller detects negative polarity, possibly due to failure of the input supply or voltage ripple, the Pull-Down quickly discharges the MOSFET gate through a discharge transistor. The Gate Pull Down pin can discharge the MOSFET gate capacitance with 160-mA pull down current to speed up the MOSFET turn OFF time. This fast pull down reacts regardless of the Vcap charge level. If the input supply abruptly fails, as would happen if the supply gets shorted to ground, a reverse current will temporarily flow through the MOSFET. This reverse current can be due to parallel connected supplies and load capacitance and is dependent upon the R_{DSON} of the MOSFET.

Feature Description (continued)

When the negative voltage across the Anode and Cathode pins reaches -20mV (typical), the LM74610-Q1 immediately reacts and discharges the MOSFET gate capacitance as shown in Figure 11 . A MOSFET with 5nF of effective gate capacitance can be turned off by the LM74610-Q1 within 2µs (typical). The fast turnoff time minimizes the reverse current flow from MOSFET drain by opening the circuit. The reverse leakage current does not exceed 110µA for a constant 13.5V reverse voltage across Anode and Cathode pins. The reverse leakage current for a Schottky diode is 15mA under the same voltage and temperature conditions.

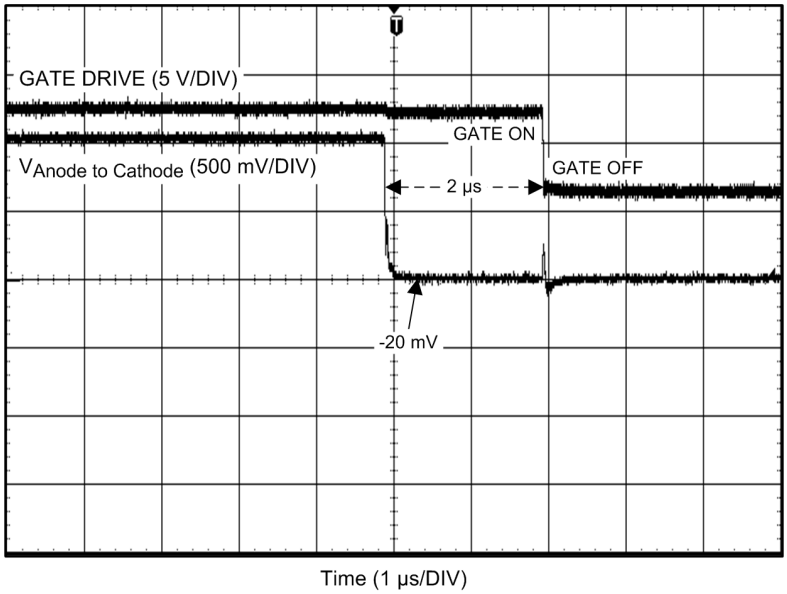


Figure 11. Gate Pull Down in the Event of Reverse Polarity

7.4 Device Functional Modes

The LM74610-Q1 operates in two modes:

- **Body Diode Conduction Mode**

  The LM74610-Q1 solution works like a conventional diode during this time with higher forward voltage drop. The power dissipation during this time can be given as:

$$P_{Dissipation} = \left(V_{Forward\,Drop}\right) \times \left(I_{Drain\,Current}\right) \quad (2)$$

  However, the current only flows through the body diode while the MOSFET gate is being charged to $V_{GS(TH)}$. This conduction is only for 2% duty cycle, therefore it does not cause any thermal issues.

$$\text{Body Diode ON Time} = \frac{C \times (VcapH - VcapL)}{I_{Charge\,Current}} \quad (3)$$

- **The MOSFET Conduction Mode**

  The MOSFET is turned on during this time and current flow is only through the MOSFET. The forward voltage drop and power losses are limited by the R_{DSON} of the specific MOSFET used in the solution. The LM74610-Q1 solution output is comprised of the MOSFET conduction mode for 98% of its duty cycle. This time period is given by the following expression:

$$\text{MOSFET ON Time} = \frac{C \times (VcapH - VcapL)}{I_{Discharge\,Current}} \quad (4)$$

Device Functional Modes (continued)

7.4.1 Duty Cycle Calculation

The LM74610-Q1 has an operating duty cycle of 98% at 25 ℃ and >90% at 125 ℃. The duty cycle doesn't depend on the Vcap capacitance value. However, the variation in capacitance value over temperature has direct correlation to the switching frequency between the MOSFET and body diode. If the capacitance value decreases, the charging and discharging time will also decrease, causing more frequent switching between body diode and the MOSFET condition. The following expression can be used to calculate the duty cycle of the LM74610-Q1:

$$\text{Duty Cycle (\%)} = \frac{\text{(MOSFET ON Time)}}{\text{(MOSFET ON Time} + \text{Body Diode ON Time)}} \times 100 \quad (5)$$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM74610-Q1 is used with N-Channel MOSFET controller in a typical reverse polarity protection application. This device is connected to the N-Channel MOSFET as shown in Figure 12 . The schematic for the typical application is shown in Figure 13 where the LM74610-Q1 is used in series with a battery to drive the MOSFET Q1. The TVS+ and TVS- are not required for the LM74610-Q1. However, they are typically used to clamp the positive and negative voltage surges respectively. The output capacitor Cout is recommended to protect the immediate output voltage collapse as a result of line disturbance.

8.2 Typical Application

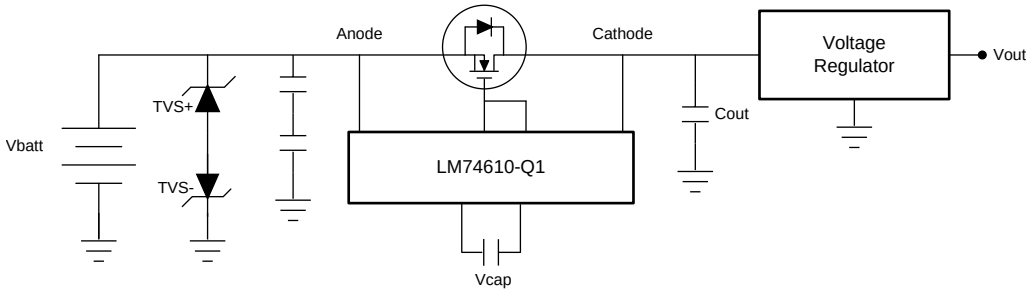


Figure 12. Typical System Application

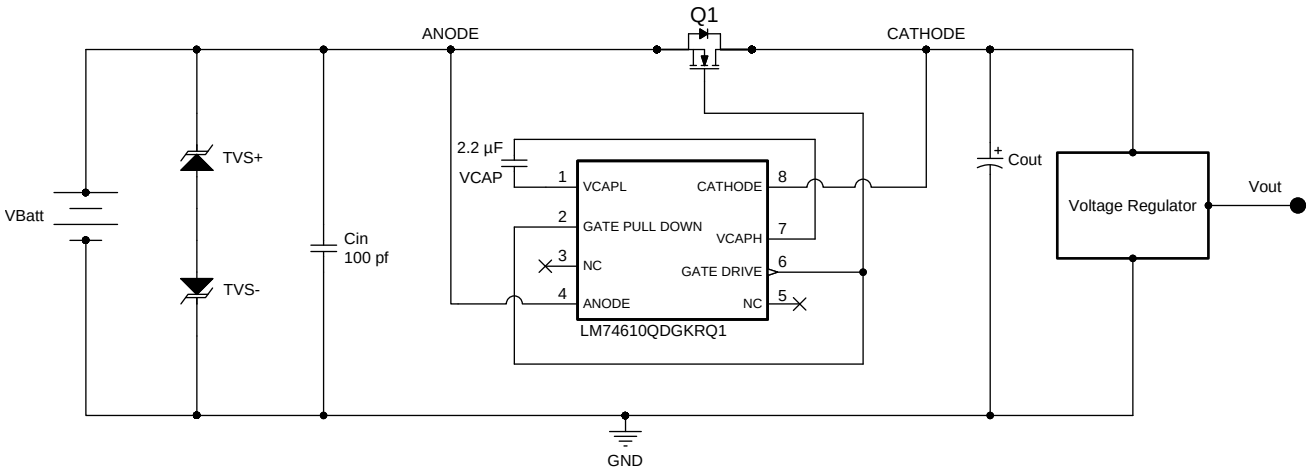


Figure 13. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	Max V_{DS} of the MOSFET
Output Voltage	Max V_{DS} of the MOSFET
Maximum Negative Voltage	-45V
Output Current Range	Maximum drain current
Output Capacitance	47µF
Transient Response, 3A Load Step	ΔV_o = ± 5%

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

8.2.2.1 Design Considerations

- Input voltage range
- Output current range
- Body Diode forward voltage drop for the selected MOSFET
- MOSFET Gate threshold voltage

8.2.2.2 Startup Voltage

The LM74610-Q1 will not initiate the charge pump operation if a closed loop system is in standby mode or the drain current is smaller than 1mA (typical). This is due to a minimum body diode voltage requirement of the LM74610-Q1 controller. If the drain current is too small to produce a minimum voltage drop of 0.48V at 25℃, the charge pump circuitry will remain off and the MOSFET will act just like a diode. It is very important to know the body diode voltage parameter of a MOSFET before implementing it into the Smart Diode solution. Some N-channels MOSFETs have very low body diode voltage at higher temperature. This makes their drain current requirement higher to achieve 0.48V across the body diode in order to initiate the LM74610-Q1 controller at higher temperatures.

8.2.2.3 Capacitor Selection

A ceramic capacitor should be placed between VcapL and VcapH. The capacitor acts as a holding tank to power up the control circuitry when the MOSFET is on.

When the MOSFET is off, this capacitor is charged up to higher voltage threshold of ~6.3 V. Once this voltage is reached, the Gate Drive of LM74610-Q1 will provide drive for the external MOSFET. When the MOSFET is ON, the voltage across its body diode is collapsed because the forward conduction is through the MOSFET. During this time, the capacitor acts as a supply for the Gate Drive to keep the MOSFET ON.

The capacitor voltage will gradually decay when the MOSFET is ON. Once the capacitor voltage reaches a lower voltage threshold of 5.15V, the MOSFET is turned off and the capacitor gets recharged again for the next cycle.

A capacitor value of 220nF to 4.7uF with X7R/COG characteristic and 16V rating or higher is recommended for this application. A higher value capacitor sets longer MOSFET ON time and OFF time; however, the duty cycle remains at ~98% for MOSFET ON time irrespective of capacitor value.

If the Vcap value is 2.2µF, the MOSFET ON time and OFF time can be calculated using Equation 1 :

$$\textbf{MOSFET ON Time = (2.2 µF × 1.15 V)/0.95 µA = 2.66 seconds} \quad (6)$$

$$\textbf{Body Diode ON Time = (2.2 µF × 1.15 V)/46 µA = 55 miliseconds} \quad (7)$$

The duty cycle can be calculated using Equation 5 :

$$\textbf{Duty Cycle \% = 2.66 sec / (2.66 sec + 0.055 sec) = 98\%} \quad (8)$$

8.2.2.4 MOSFET Selection

The LM74610-Q1 can provide up to 5V of gate to source voltage (V_{GS}). The important MOSFET electrical parameters are the maximum continuous Drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, and the drain-to-source On resistance R_{DSON}. The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The rating for the maximum current through the body diode, I_S, is typically rated the same as, or slightly higher than the drain current, but body diode current only flows for a small period when the charge pump capacitor is being charged.

The voltage across the MOSFET's body diode must be higher than 0.48 V at low current. The body diode voltage for a MOFET typically decreases as the ambient temperature increases. This will increase the source current requirement to achieve the minimum body diode drain-to-source voltage for the charge pump to initiate. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions. The LM74610-Q1 does not have positive voltage limitation, however, it is recommended to use MOSFETs with voltage rating up to 45 V for automotive applications. Table 2 shows the examples of recommended MOSFETs to be used with the LM74610-Q1.

8.2.3 Application Curves

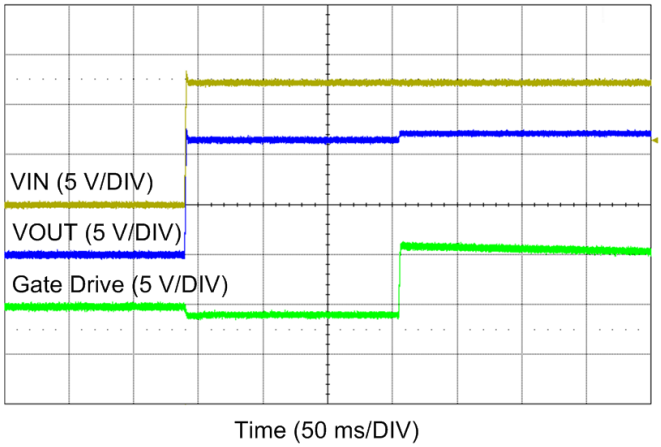


Figure 14. Startup Relative to VIN

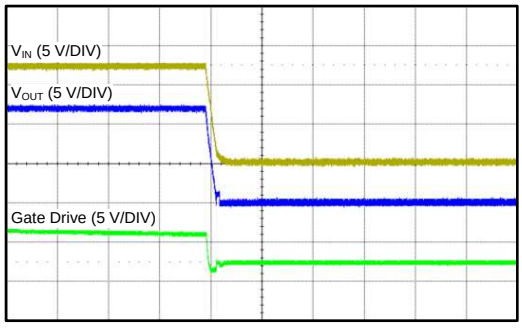


Figure 15. Shutdown Relative to VIN

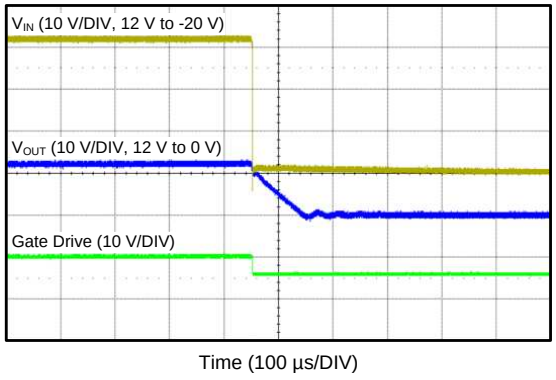


Figure 16. Response to Reverse Polarity

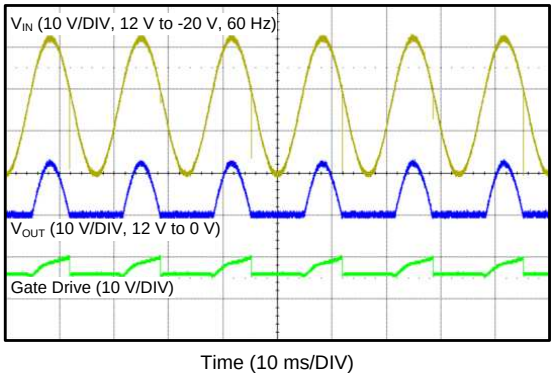


Figure 17. Response to a 60Hz AC Input

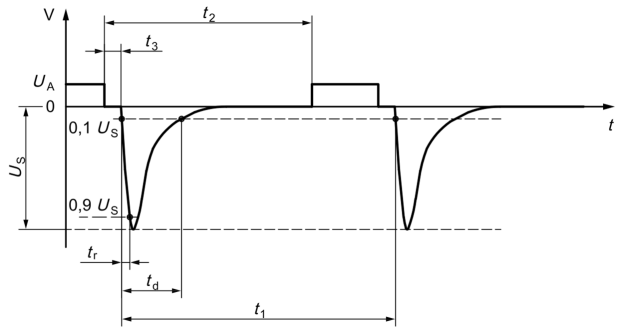


Figure 18. ISO Pulse 1 Test Setup

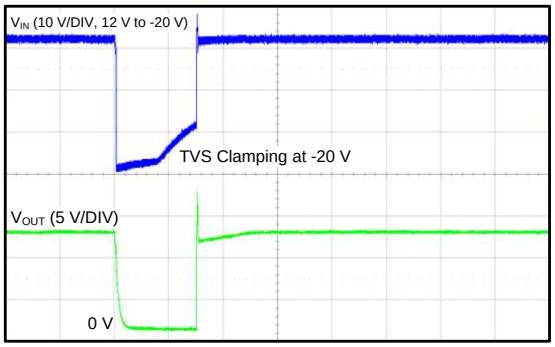


Figure 19. Response to ISO 1 Pulse

8.2.4 Selection of TVS Diodes in Automotive Reverse Polarity Applications

TVS diodes can be used in automotive systems for protection against transients. There are 2 types of TVS diode, one that offers bi-directional clamping and one that is uni-directional. In the application circuit show in Figure 12, 2 unidirectional TVS diodes are used. TVS + does the clamping for positive pulses as seen in load dump and TVS- does the clamping for negative pulses such as seen in the ISO specs.

There are two important specs to be aware of: breakdown voltage and clamping voltage. Breakdown voltage is the voltage at which the TVS diode goes into avalanche similar to a zener diode and is specified at a low current value typ 1mA. Clamping voltage is the voltage the TVS diode clamps to in high current pulse situations.

In the case of an ISO 7637-2 pulse 1, the voltages go to -150V with a generator impedance of 10Ω. This translates to 15A flowing through the TVS - and the voltage across the TVS would be close to its clamping voltage. A rule of thumb with TVS diode voltage selection is that the breakdown voltage should be higher than worst case steady state voltages seen in the system. TVS diodes are meant to clamp pulses and not meant for steady state voltages.

The value of the TVS + is selected such that the breakdown voltage of the TVS is higher than 24V which is a commonly used battery for jump start. LM74610-Q1 does not have a positive voltage limit so the selection of the voltage rating of TVS + is determined by the max voltage tolerated by the downstream electronics. If the downstream parts can withstand at least 37V (suppressed load dump) then there is no need to use the TVS+. In this case it can be replaced with a diode as seen in Figure 20. A 1A diode with a 30A surge current rating and at least 40V reverse voltage rating is recommended. In case positive clamping voltage is desired then SMBJ24A/SMBJ26A is recommended for TVS + as seen in Figure 12.

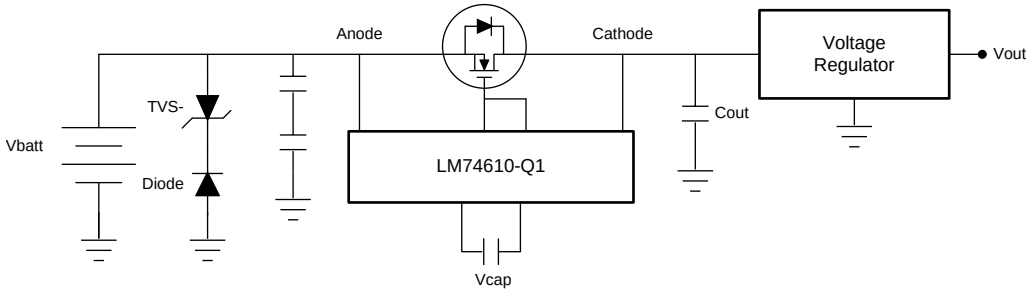


Figure 20. Typical Application without Positive Voltage Clamping

The value of the TVS – is selected such that 2 criteria are met. The breakdown voltage of the TVS should be higher than the max reverse battery voltage which is typically 15V. The second criterion is that the abs max rating for reverse voltage of the LM74610 is not exceeded (-45V).

In case of reverse voltage pulses such as in ISO specs, the LM74610 turns the MOSFET off. When the MOSFET turns off the voltage seen by the LM74610, Anode to Cathode is - (clamping voltage of TVS- (plus) the output capacitor voltage). If the max voltage on output capacitors is 16V, then the clamping voltage of the TVS- should not exceed, 45V – 16V = 29V.

SMBJ14A/SMBJ15A/SMBJ16A TVS diodes can be used for TVS-. The breakdown voltage of SMBJ14A is 15.6V and SMBJ16A is 17.8V. This meets criteria one. The clamping voltage of SMBJ14A is 23.2V and SMBJ16A is 26V. This meets the second criteria.

Bi-directional TVS diodes are not recommended due to their symmetrical clamping specs. SMBJ24CA has a breakdown voltage of 26.7V and a clamping voltage of 38.9V. The breakdown voltage meets the criteria for being higher than 24V. However the clamping voltage is 38.9V. The high clamping voltage is not an issue for the positive pulses however for a negative ISO pulse, the abs max of the LM74610 can be violated. Voltage across Anode to Cathode in this case is –(38.9V + 16V) = -54.9V which violates abs max rating of -45V.

As far as power levels for TVS diodes the 'B' in the SMBJ stands for 600W peak power levels. This is sufficient for ISO 7637-2 pulses and suppressed load dump case (ISO-16750-2 pulse B). For unsuppressed load dumps (ISO-16750-2 pulse A) higher power TVS diodes such as SMCJ or SMDJ may be required.

8.2.5 OR-ing Application Configuration

Basic redundant power architecture comprises of two or more voltage or power supply sources driving a single load. In its simplest form, the OR-ing solution for redundant power supplies consists of Schottky OR-ing diodes that protect the system against an input power supply fault condition. A diode OR-ing device provides effective and low cost solution with few components. However, the diodes forward voltage drops affects the efficiency of the system permanently, since each diode in an OR-ing application spends most of its time in forward conduction mode. These power losses increase the requirements for thermal management and allocated board space.

The LM74610-Q1 ICs combined with external N-Channel MOSFETs can be used to in OR-ing Solution as shown in Figure 21 . The source to drain voltage V_{DS} for each MOSFET is monitored by the Anode and Cathode pins of the LM74610-Q1. The forward conduction is through MOSFETs 98% of the time which avoids the diode forward voltage drop. The body diode of each MOSFET only conducts the remaining 2% of the time to allow the charge pump capacitor to be fully charged.

This is essential for an OR-ing device to quickly detect the reverse current and instantly pull-down the MOSFET gate to block the reverse current flow. An effective OR-ing solution needs to be extremely fast to limit the reverse current amount and duration. The LM74610-Q1 devices in OR-ing configuration constantly sense the voltage difference between Anode and Cathode pins, which are the voltage levels at the power sources (PS1, PS2) and the common load point respectively. When either of the power sources operates at lower voltage, the LM74610-Q1 detects a negative polarity and shuts down the Gate Drive through a fast Pull-Down within 2µsec (typical).

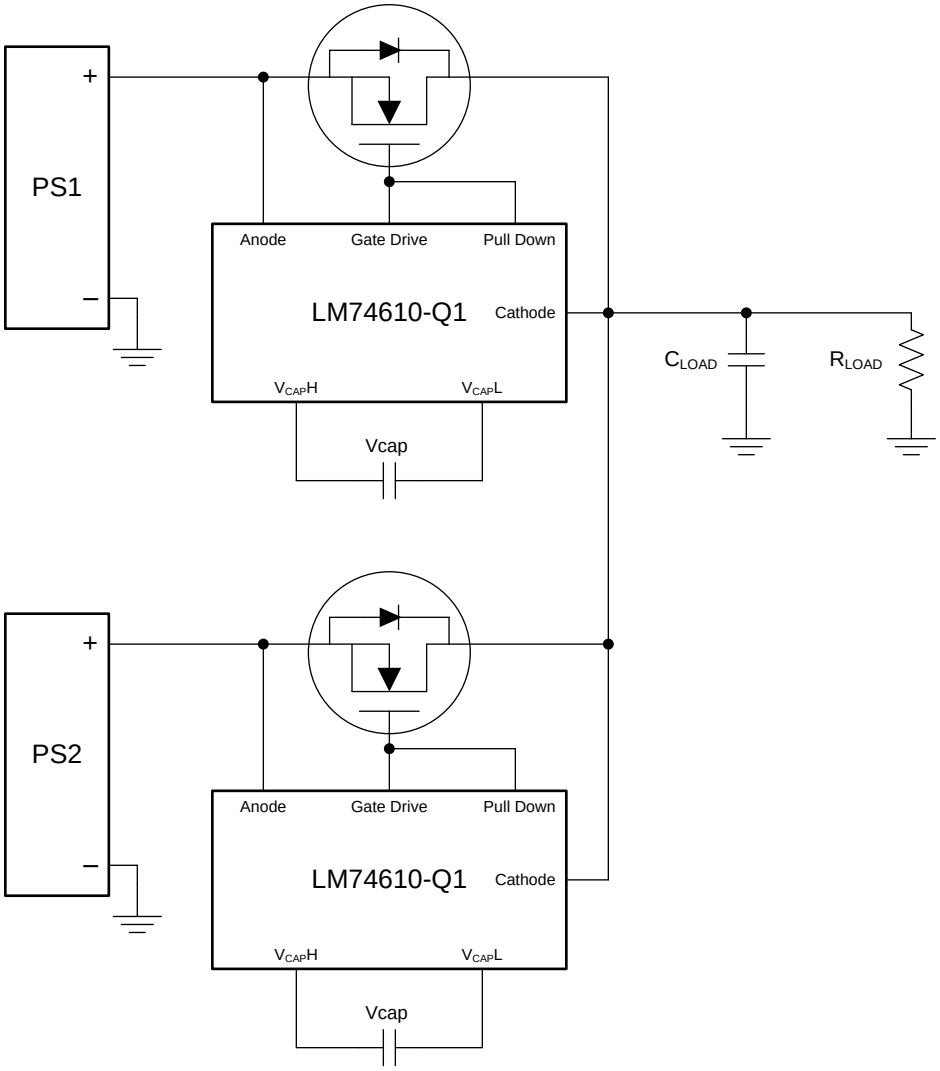


Figure 21. Typical OR-ing Application

If one of the power supplies fails in LM74610-Q1 OR-ing controller application, the output remains uninterrupted. This behavior is similar to diode OR-ing. Figure 22

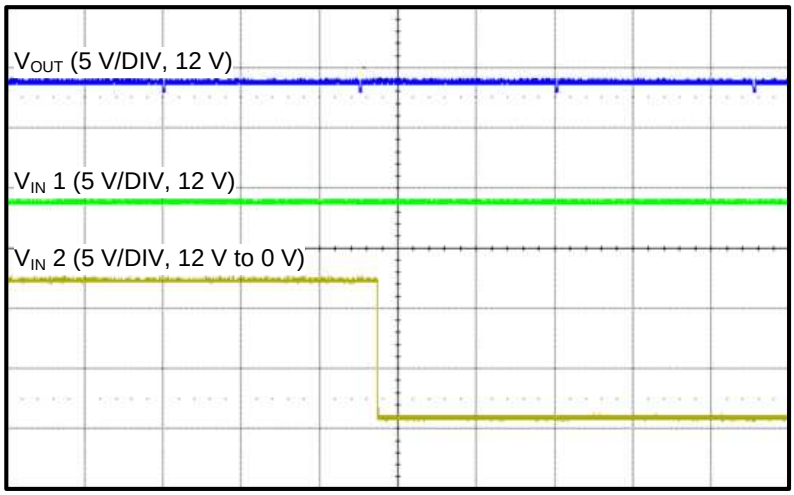


Figure 22. LM74610-Q1 OR-ing waveform

8.2.6 Design Requirements

NOTE

Startup voltage is the voltage drop is needed for the controller to turn ON. It directly influences the Minimum output current at which the MOSFET turns ON.

Table 2. Recommended MOSFET Examples(1)

Part No	Voltage (V) Current	Drain Current at 25C	Rdson mΩ @ 4.5V	Vgs Threshold(V)	Diode voltage @ 2A at 125C/175C	Package; Footprint	Qual
CSD17313Q2Q1	30	5	26	1.8	0.65	SON; 2 x 2	Auto
SQJ886EP	40	60	5.5	2.5	0.5	PowerPAK SO-8L; 5 x 6	Auto
SQ4184EY	40	29	5.6	2.5	0.5	SO-8; 5 x 6	Auto
Si4122DY	40	23.5	6	2.5	0.5	SO-8; 5 x 6	Auto
RS1G120MN	40	12	20.7	2.5	0.6	HSOP8; 5 x 6	Auto
RS1G300GN	40	30	2.5	2.5	0.5	HSOP8; 5 x 6	Auto
CSD18501Q5A	40	22	3.3	2.3	0.53	SON; 5 x 6	Industrial
SQD40N06-14L	60	40	17	2.5	0.5	TO-252; 6 x 10	Auto
SQ4850EY	60	12	31	2.5	0.55	SO-8; 5 x 6	Auto
CSD18532Q5B	60	23	3.3	2.2	0.53	SON;5 x 6	Industrial
IPG20N04S4L-07A	40	20	7.2	2.2	0.48	PG-TDSON-8-10; 5 x 6	Auto
IPB057N06N	60	45	5.7	3.3	0.55	PG-TO263-3; 10 x 15	Auto
IPD50N04S4L	40	50	7.3	2.2	0.50	PG-TO252-3-313; 6 x10	Auto

(1) The LM74610-Q1 solution is not limited to the MOSFETs included in this table. It only shows examples of compatible MOSFETs.

Table 2. Recommended MOSFET Examples(1) (continued)

Part No	Voltage (V) Current	Drain Current at 25C	Rdson mΩ @ 4.5V	Vgs Threshold(V)	Diode voltage @ 2A at 125C/175C	Package; Footprint	Qual
BUK9Y3R5-40E	40	100	3.8	2.1	0.48	LFPAK56; Power-SO8 (SOT669); 5 x 6	Auto
IRF7478PbF-1	60	7	30	3	0.55	SO-8; 5 x 6	Industrial
SQJ422EP	40	75	4.3	2.5	0.50	PowerPAK SO-8L; 5 x 6	Auto
IRL1004	40	130	6.5	1	0.60	TO-220AB	Auto
AUIRL7736	40	112	2.2	3	0.65	DirectFET®; 5 x 6	Auto

Table 3. Recommended TVS Combination to meet ISO7637 Specifications (Note 4)

TVS +	TVS-
SMA6T33AY	SMBJ14A/ SMA6T15AY
SMA6T30AY	SMBJ14A/ SMA6T15AY
SMA6T28AY	SMBJ14A/ SMA6T15AY

9 Power Supply Recommendations

While testing the LM74610-Q1 solution, it is important to use low impedance power supply which allows current sinking. If the power supply does not allow current sinking, it would prevent the current flow in the reverse direction in the event of reverse polarity. The MOSFET gate won't get pulled down immediately due to the absence of reverse current flow.

10 Layout

10.1 Layout Guidelines

- The VIN terminal is recommended to have a low-ESR ceramic bypass-capacitor. The typical recommended bypass capacitance is a 10-µF ceramic capacitor with a X5R or X7R dielectric.
- The VIN terminal must be tied to the source of the MOSFET using a thick trace or polygon.
- The Anode pin of the LM74610-Q1 is connected to the Source of the MOSFET for sensing.
- The Cathode pin of the LM74610-Q1 is connected to the drain of the MOSFET for sensing.
- The high current path of for this solution is through the MOSFET, therefor it is important to use thick traces for source and drain of the MOSFET.
- The charge pump capacitor Vcap must be kept away from the MOSFET to lower the thermal effects on the capacitance value.
- The Gate Drive and Gate pull down pins of the LM74610-Q1 must be connected to the MOSFET gate without using vias. Avoid excessively thin traces to the Gate Drive.
- Obtaining acceptable performance with alternate layout schemes is possible, however this layout has been shown to produce good results and is intended as a guideline.
- Keep the Drive pin close to the MOSFET to avoid further reduce MOSFET turn-on delay.

10.2 Layout Example

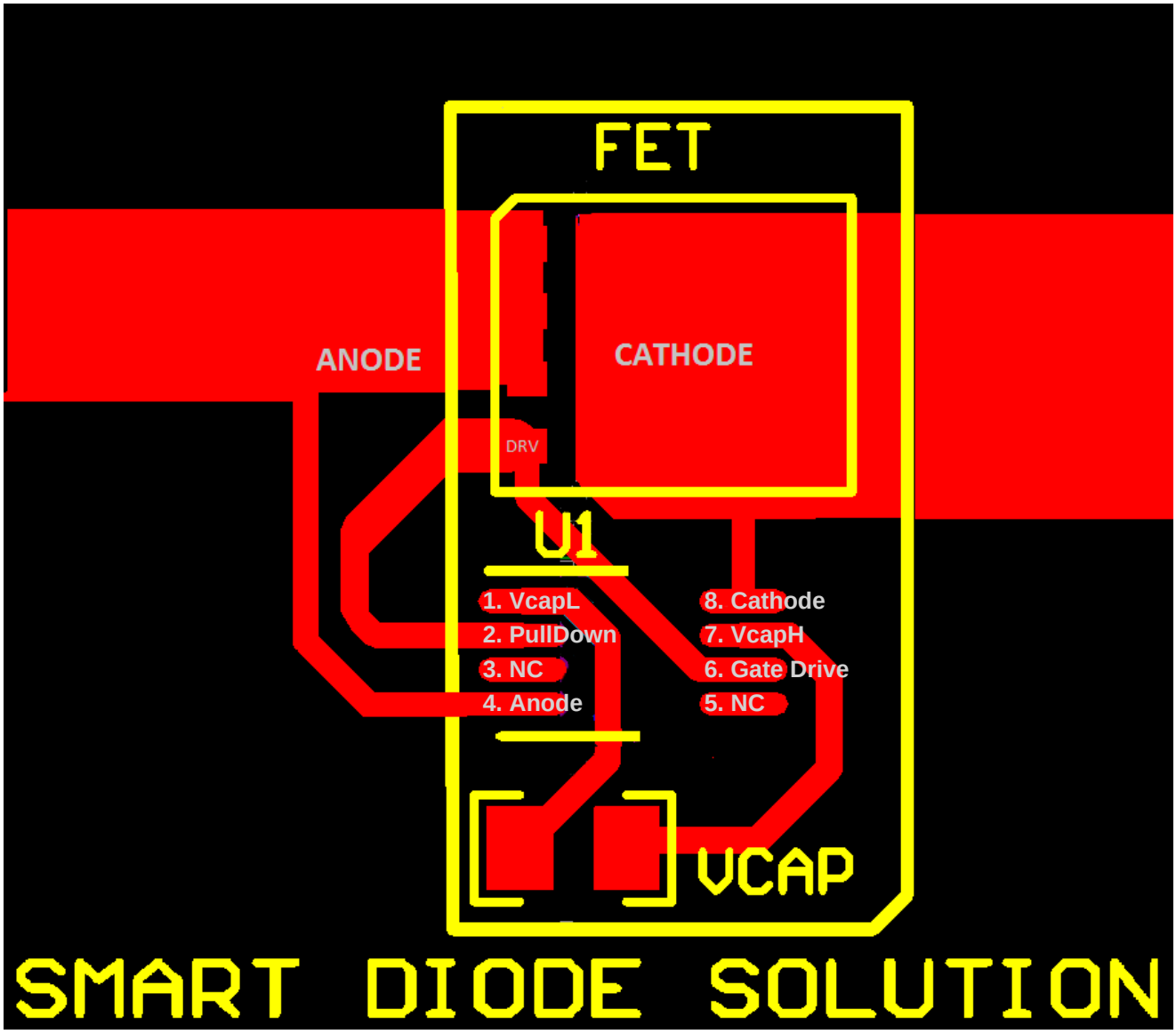


Figure 23. Layout Example

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74610QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDSK	Samples
LM74610QDGKTQ1	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDSK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

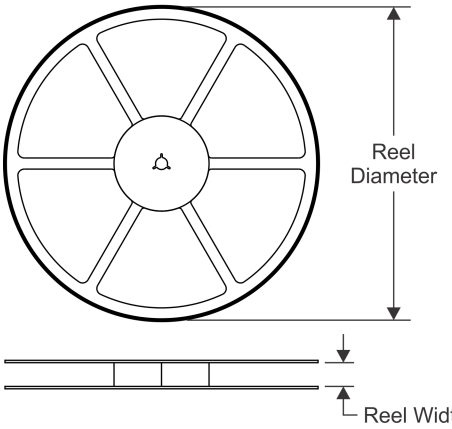
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

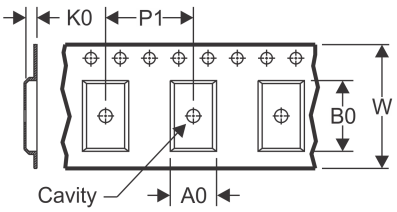
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

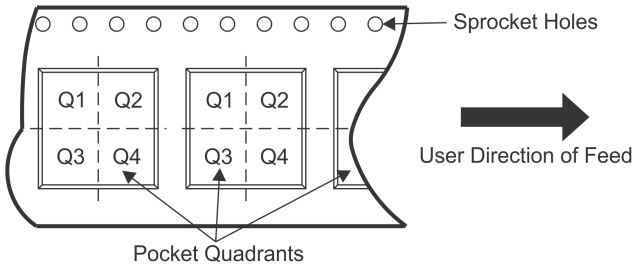


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

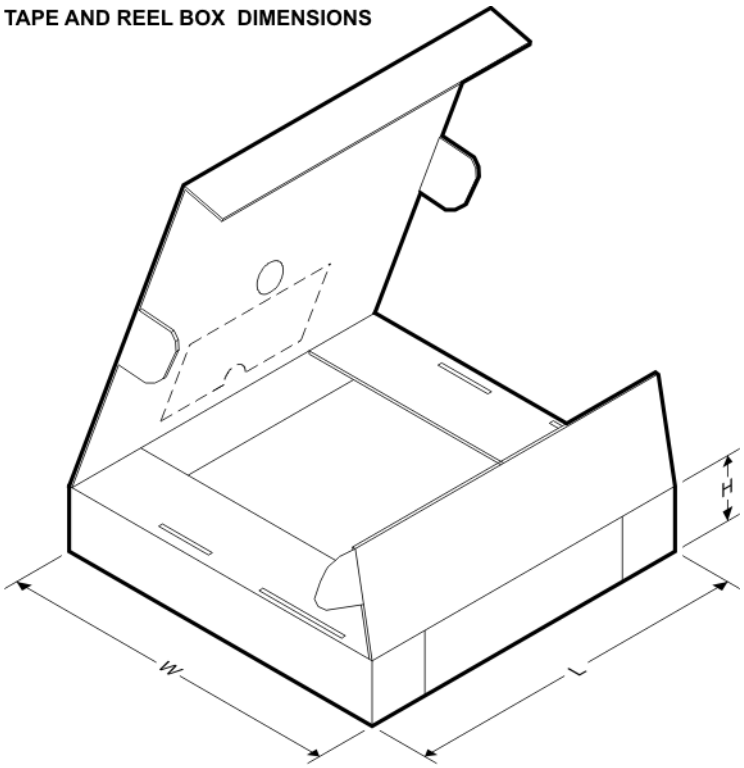
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74610QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM74610QDGKTQ1	VSSOP	DGK	8	250	178.0	13.4	5.3	3.4	1.4	8.0	12.0	Q1

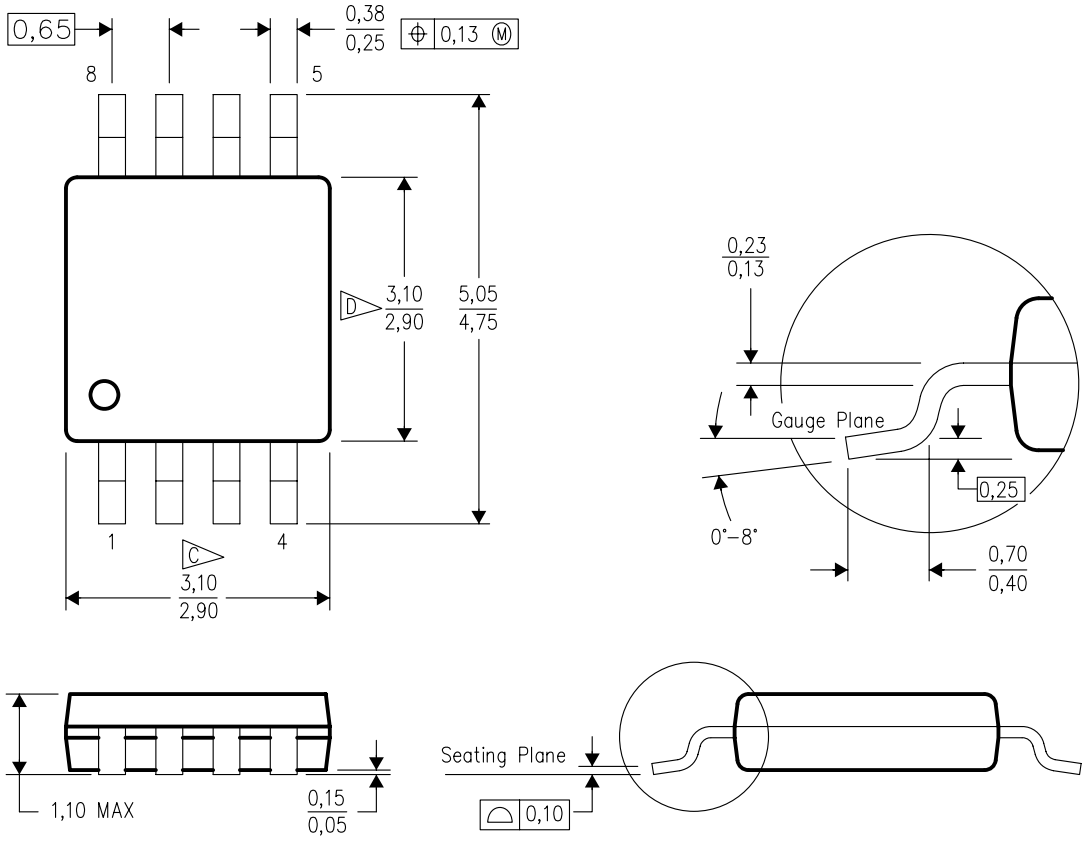
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74610QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM74610QDGKTQ1	VSSOP	DGK	8	250	213.0	191.0	50.0

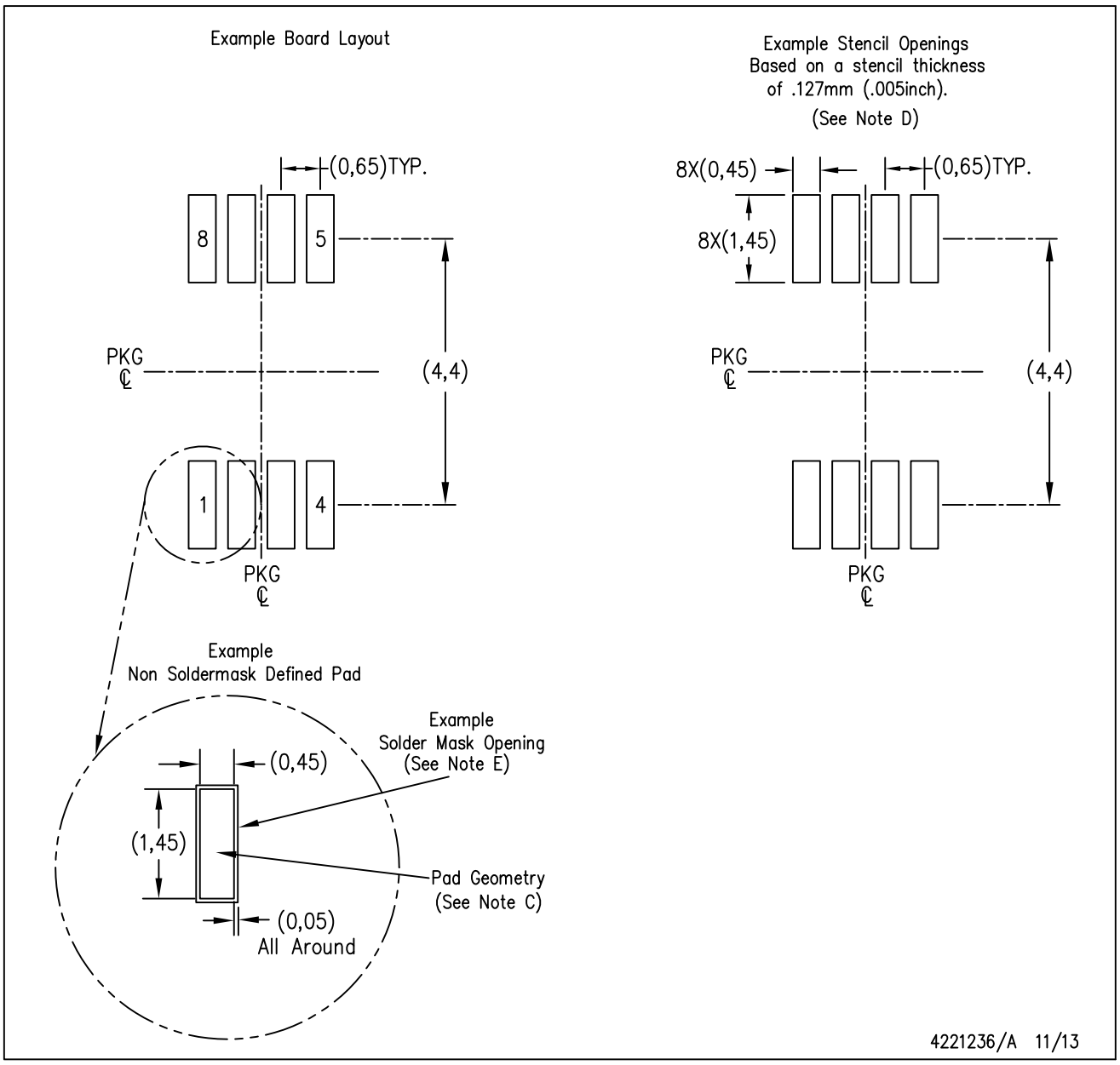
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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