Worksheet 5

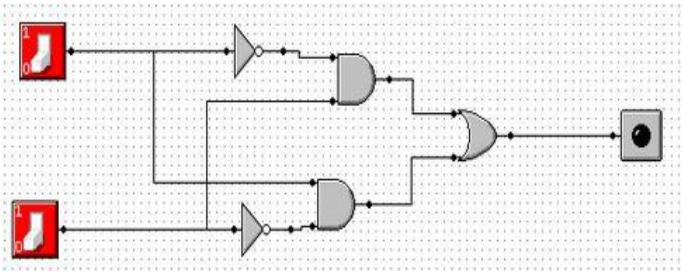
Objectives:

(1) Understand the behavior of Adder circuits.

(2) Understand the design combinational circuits for different real-world scenarios.

1) Design the following circuit and write the truth tables for them.

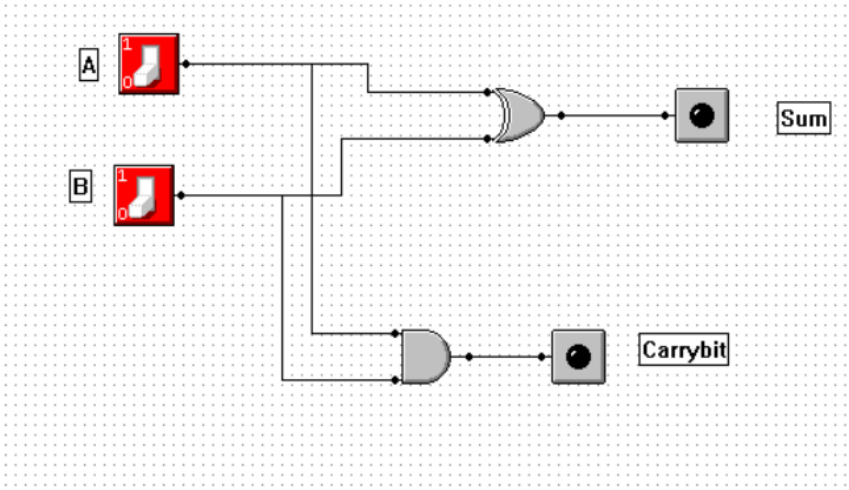
(i)



a) Draw the circuit for A XOR B and write the truth table for them. Identify the similarity between XOR circuit and circuit (i)

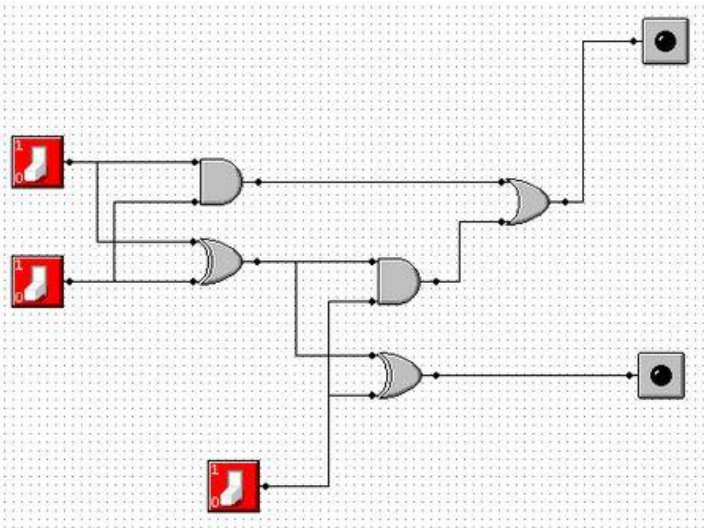
(ii)

Half Adder



(iii)

Full Adder



Discuss with your friends and lecturer, for what purpose these circuits can be used.

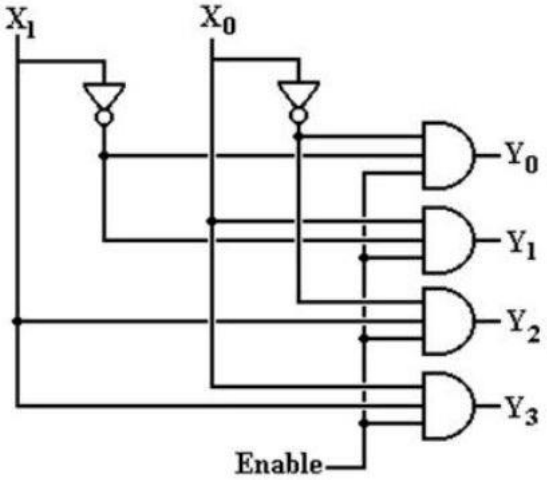
2) Parallel Adder

a. Modify your Full Adder implementation to conduct addition of two 3-bit binary numbers. The new implementation should give the summation of two numbers and any overflow carry out. You can use the full_adder.lgi that you have drawn in **1)** as the starting point. Save your new files as parallel_adder.lgi

3) Binary Decoder: A binary decoder is a combinational logic circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs. They are used in a wide variety of applications, including data demultiplexing, seven segment displays, and memory address decoding.

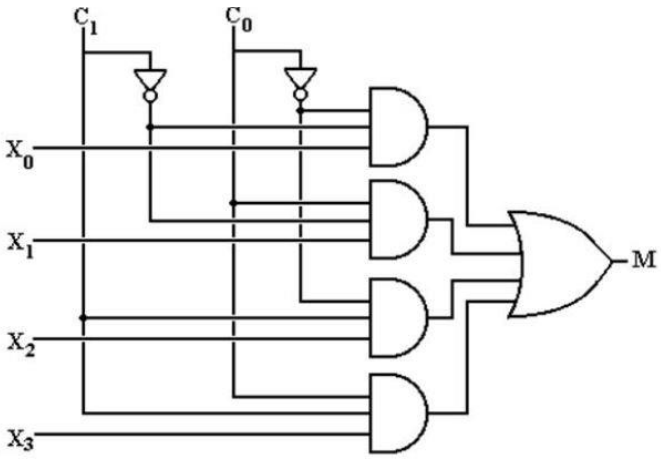
Implement the following decoder circuit in MM Logic and observe its behavior.

Worksheet 5



4) Multiplexer: A multiplexer (or mux) is a device that combines several analog or digital input signals and forwards them into a single output line. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output.

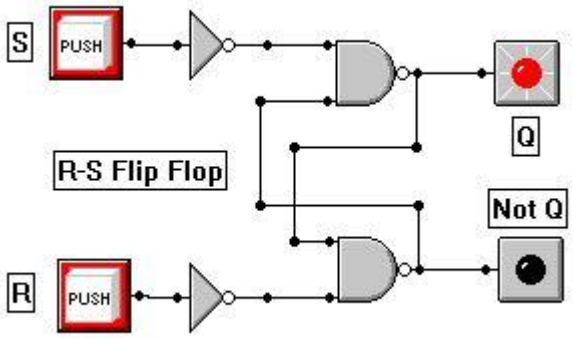
Implement the following mux circuit in MM Logic and observe its behavior.



5) Use 4 to 1 mux and 2 to 4 De-mux available in MM Logic and draw truth tables to recognize their behavior.

6) Design the following circuit using MM Logic and observe its behavior using a truth table.

Worksheet 5



What is the main difference between circuits in 1) – 5) and above circuit.

Activities:

7) Learn how to use multiplexer circuits to design decoders and different Boolean functions.

Ex: Use a Mux to implement following Boolean function

$$F = AB\bar{C} + \bar{B}C + AC$$

8) Design Circuit to generate the parity bit using even parity scheme for a 3 bit message. Discuss the steps you need to follow. Design the circuit using MML and verify the output. Save your file as even_parity.lgi.

9) Design a circuit to output whether the decimal numbers 0-7(including 0-7), is a prime number or not. Save your file as prime_number.lgi.

a. If the requirement is only to check decimal numbers 2-7(including 2 and 7), design a new circuit. Save your file as prime_number_2.lgi