INTRODUCTION TO COMPUTER SYSTEMS (IT1020)

Year 1, Semester 1

Work Sheet 05

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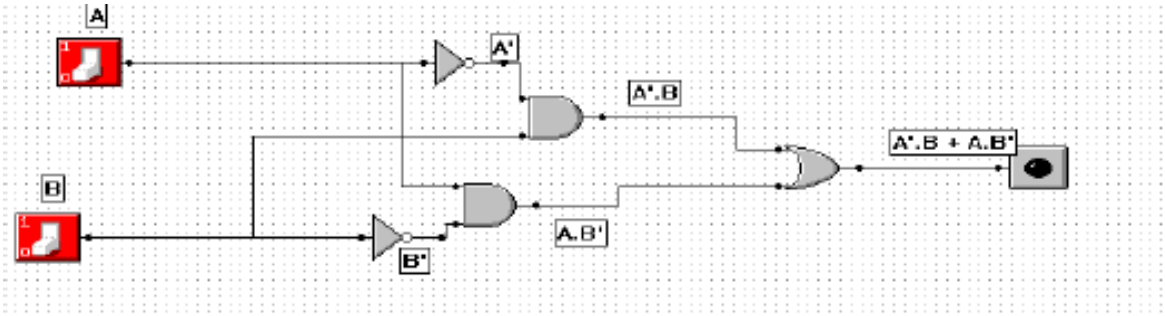
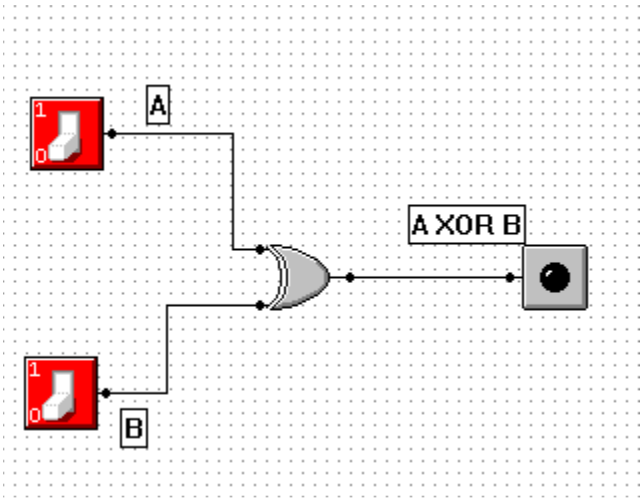
1.



i)

A	B	A’	B’	A’. B	A.B’	F
0	0	1	1	0	0	0
0	0	1	1	0	0	0
0	1	1	0	1	0	1
0	1	1	0	1	0	1
1	0	0	1	0	1	1
1	0	0	1	0	1	1
1	1	0	0	0	0	0
1	1	0	0	0	0	0

a.)

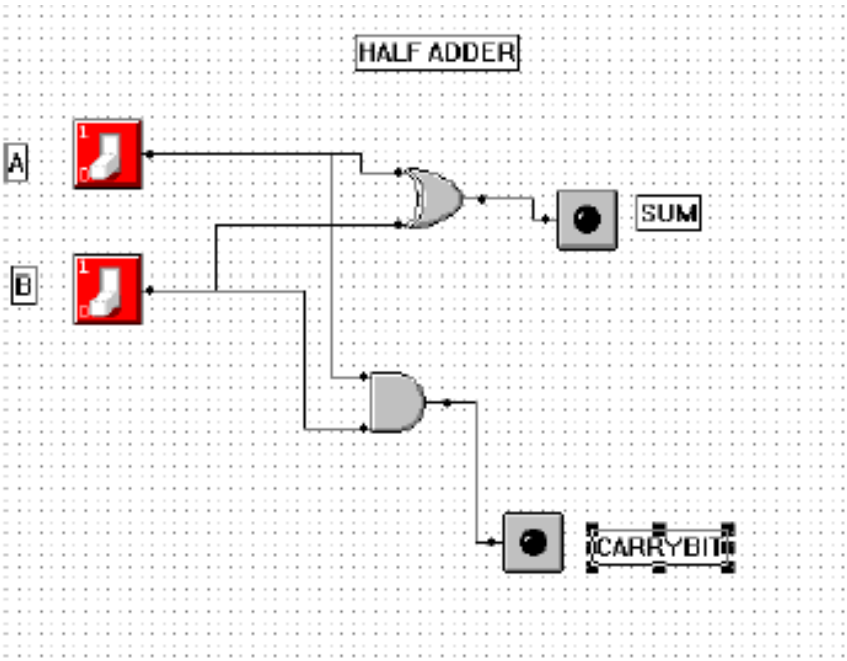


A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

i) The resemblance of the XOR circuit to the circuit

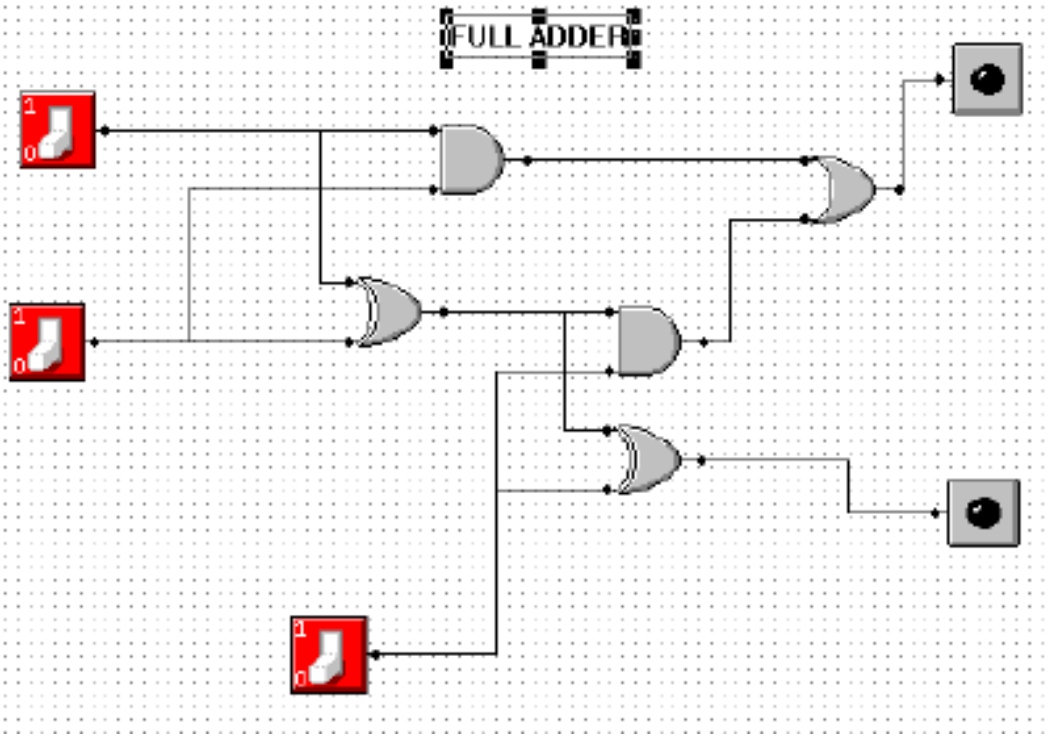
- Light is turned on when one switch is turned on.
- Off when both switches are turned on and off when both switches are turned off.

ii) Half adder



A	B	SUM	CARRYBIT
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

iii) Full adder

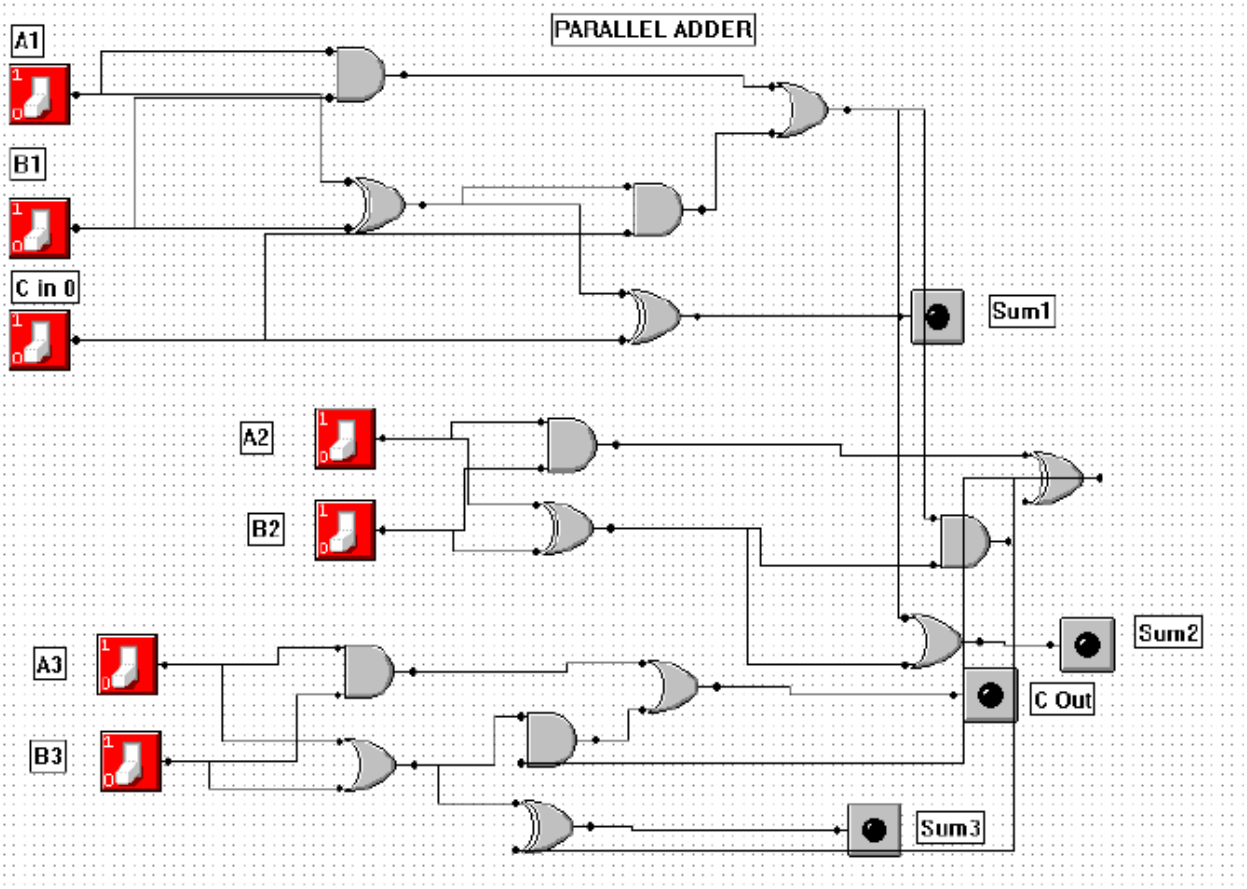


A	B	C	SUM	CARRYBIT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

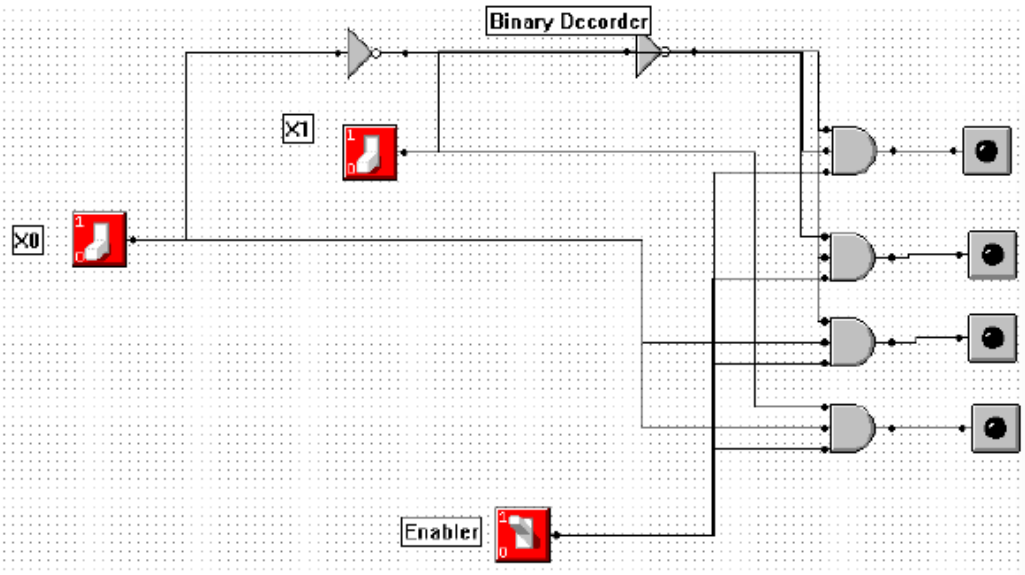
The purpose of these circuits is,

• The Half Adder class of combinational logic circuits adds two 1-bit binary digits. Both the carry and the total of the two inputs are produced. Another type of combinational logic is the Full Adder, which performs addition operations by adding three 1-bit binary digits.

2. Parallel adder

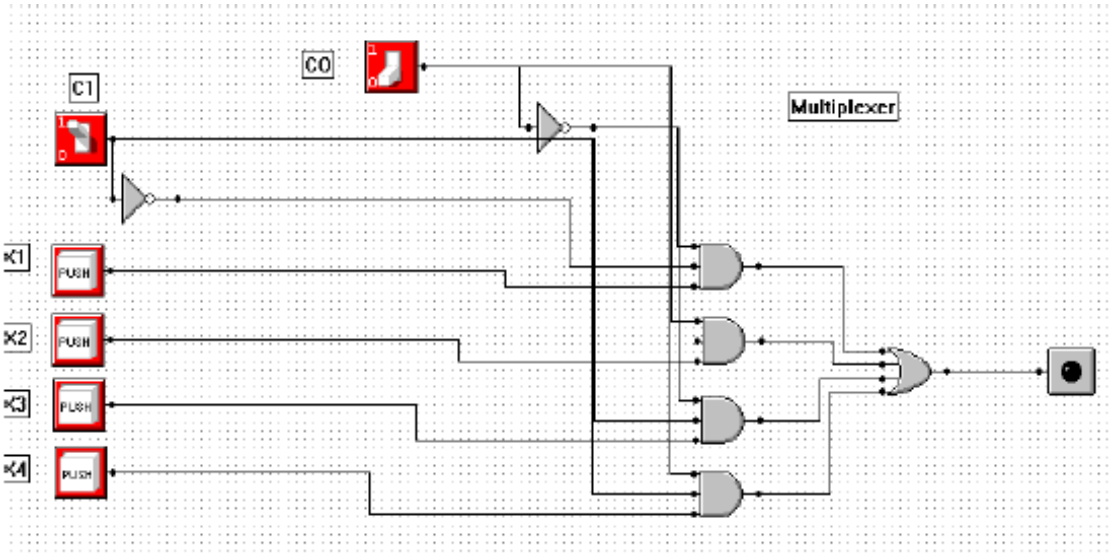


3. Binary decoder



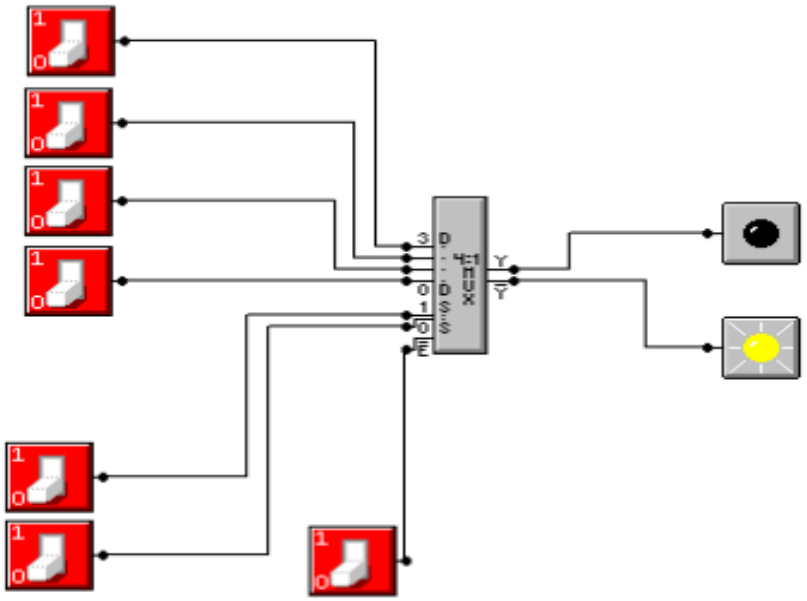
X0	X1	ENABLER	Y0	Y1	Y2	Y3
0	0	1	1	0	0	0
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	1

4. Multiplexer



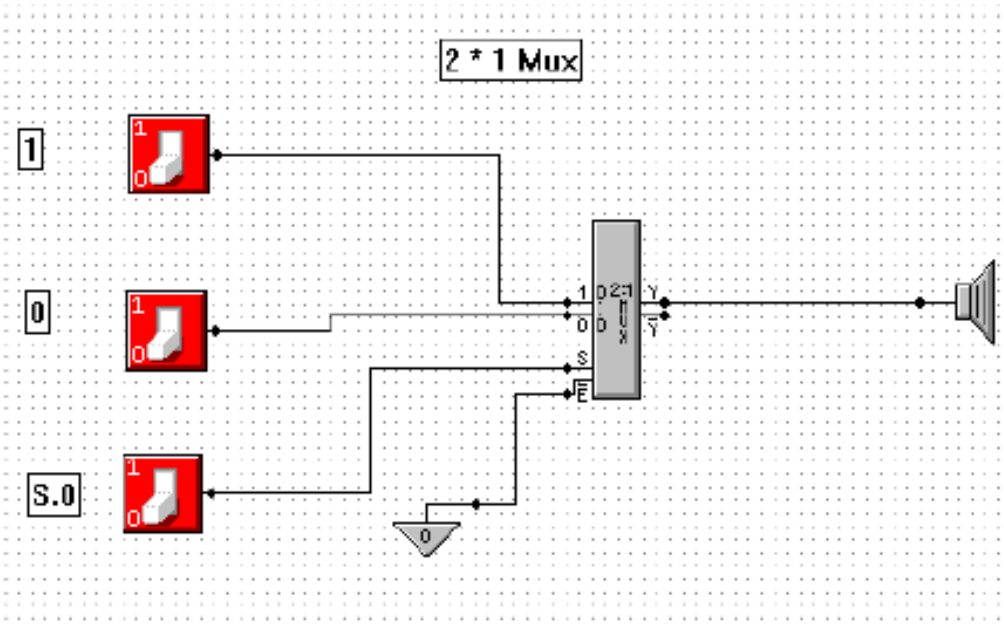
C1	C2	X	M
0	1	0 X1 1	0 1
0	0	0 X2 1	0 1
1	1	0 X3 1	0 1
1	0	0 X4 1	0 1

5. 4 to 1 mux



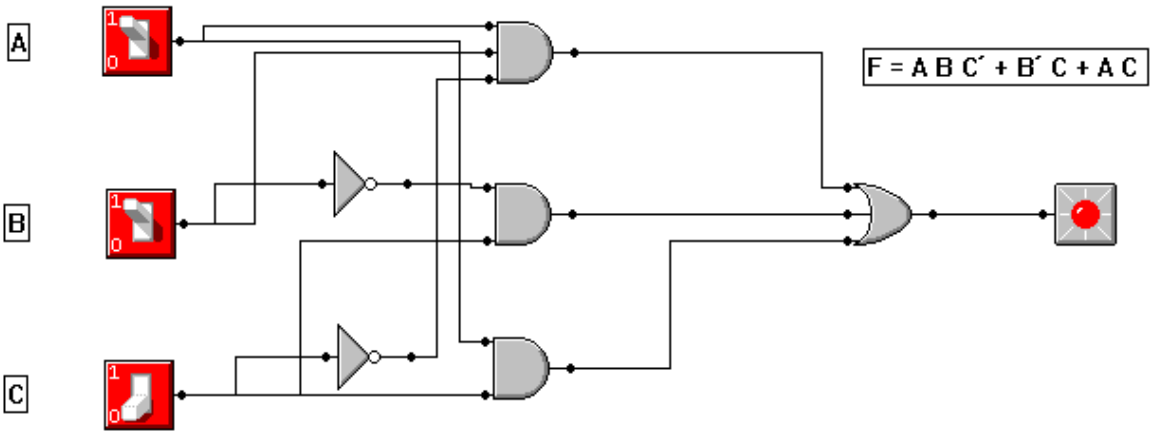
S0	S1	D0	D1	D2	D3	Y
0	0	0	X	X	X	0
0	0	1	X	X	X	1
0	1	X	0	X	X	0
0	1	X	1	X	X	1
1	0	X	X	0	X	0
1	0	X	X	1	X	1
1	1	X	X	X	0	0
1	1	X	X	X	1	1

6. 2 to 1 mux



1	0	S0	Y
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

7. F = A B C’ + B’ C + A C



Input			Output
A	B	C	F = A B C’ + B’ C + A C
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

8.