INTRODUCTION TO COMPUTER SYSTEM (IT1020)

YEAR 1, SEMISTER 1

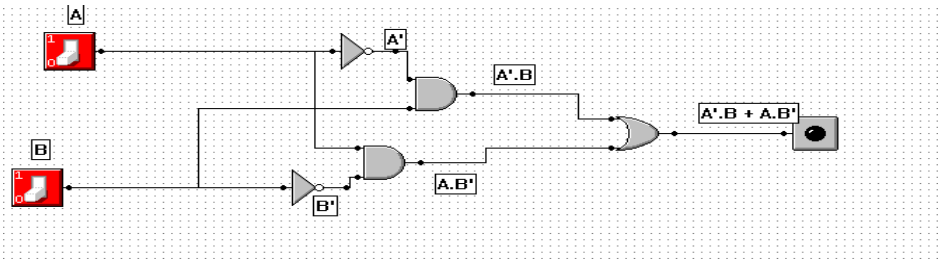
PRACTICAL ANSWER WORK SHEET 05

IT22124944, U.Kavinilavan

GROUP 10.1

06/12/2022

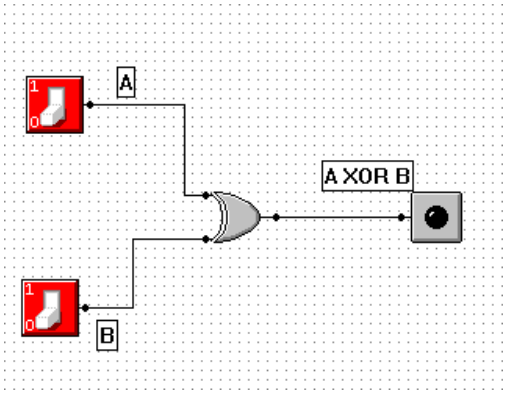
1)



i)

A	B	A’	B’	A’.B	A.B’	F
0	0	1	1	0	0	0
0	0	1	1	0	0	0
0	1	1	0	1	0	1
0	1	1	0	1	0	1
1	0	0	1	0	1	1
1	0	0	1	0	1	1
1	1	0	0	0	0	0
1	1	0	0	0	0	0

a)

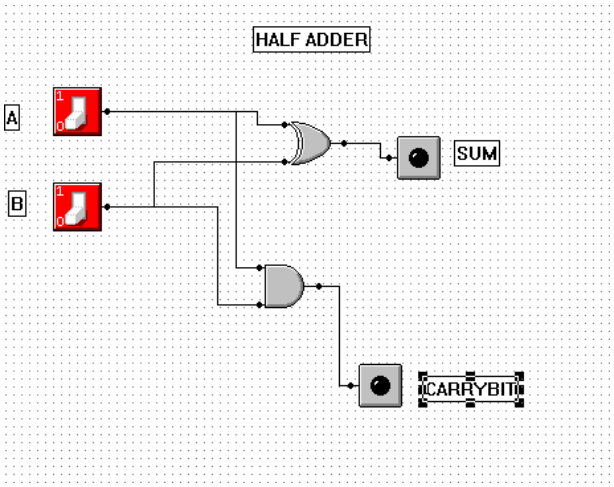


A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

i) Similarity between the above circuits

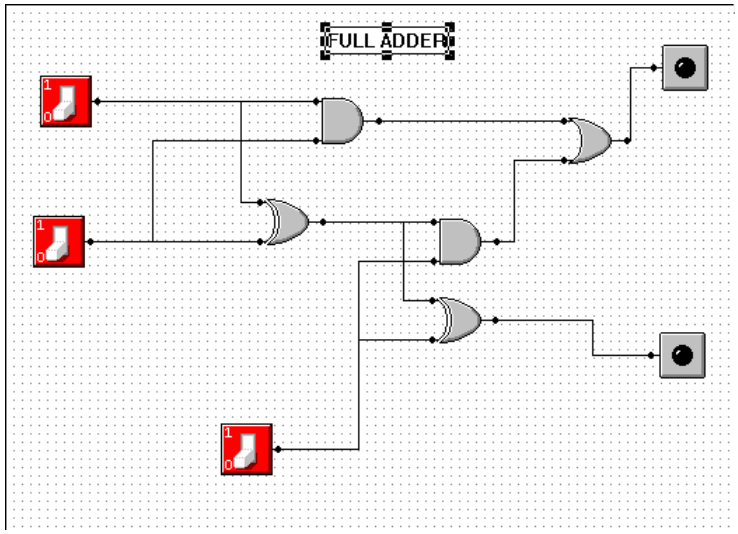
- When both switches are off the light is off
- When one switch is on the light is on
- When both switches are on the light is off

ii) Half adder



A	B	SUM	CARRYBIT
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

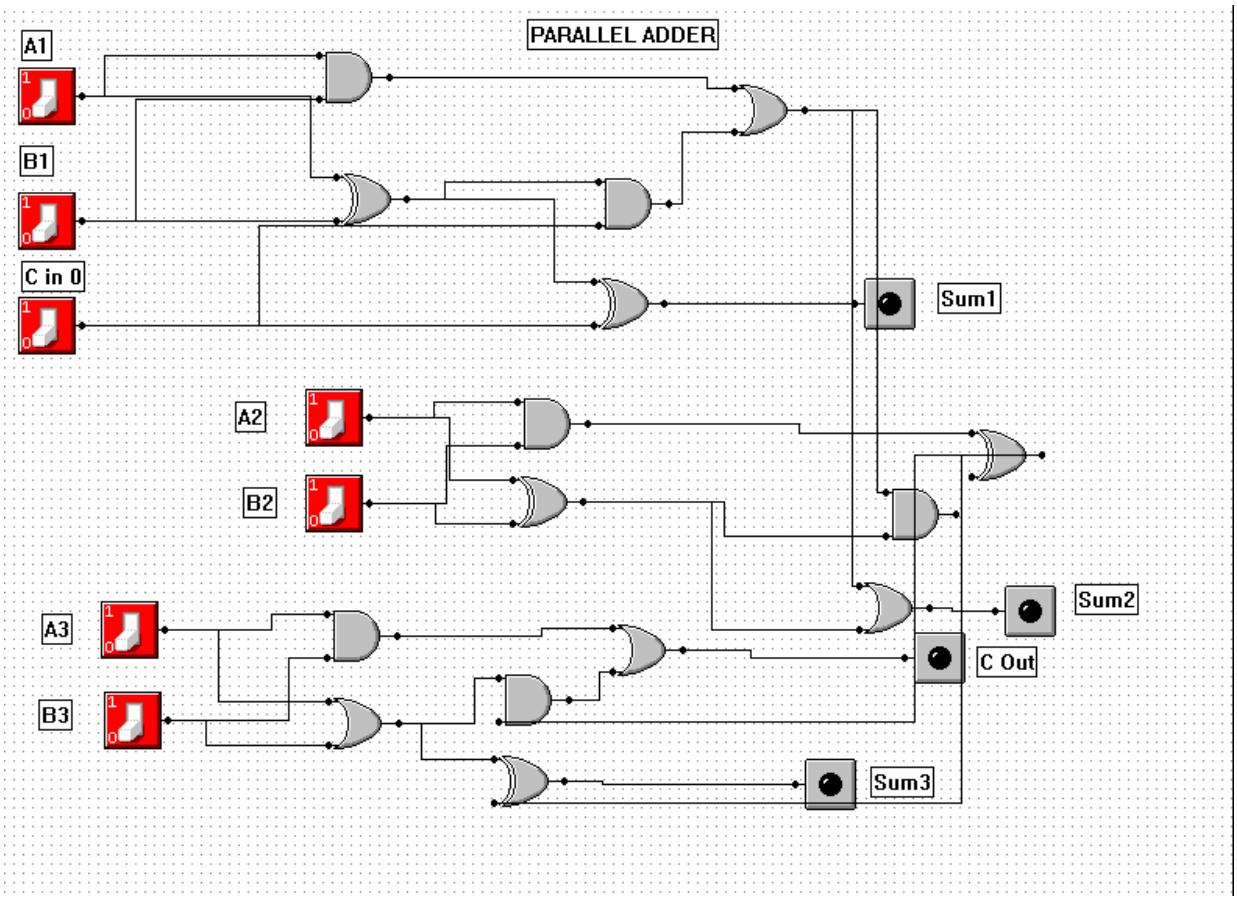
iii) Full adder



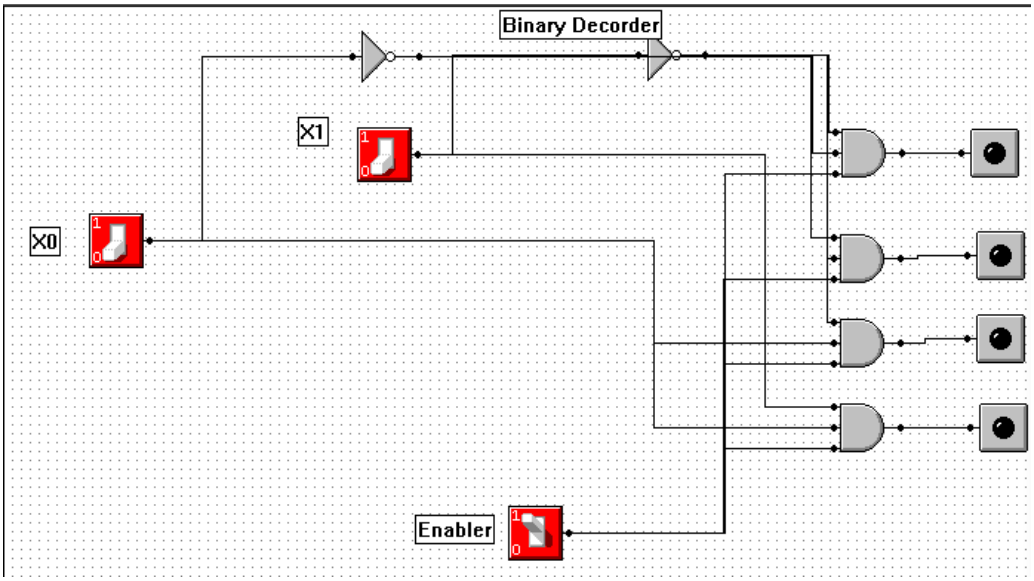
A	B	C	SUM	CARRYBIT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The purpose is

2) Parallel Adder

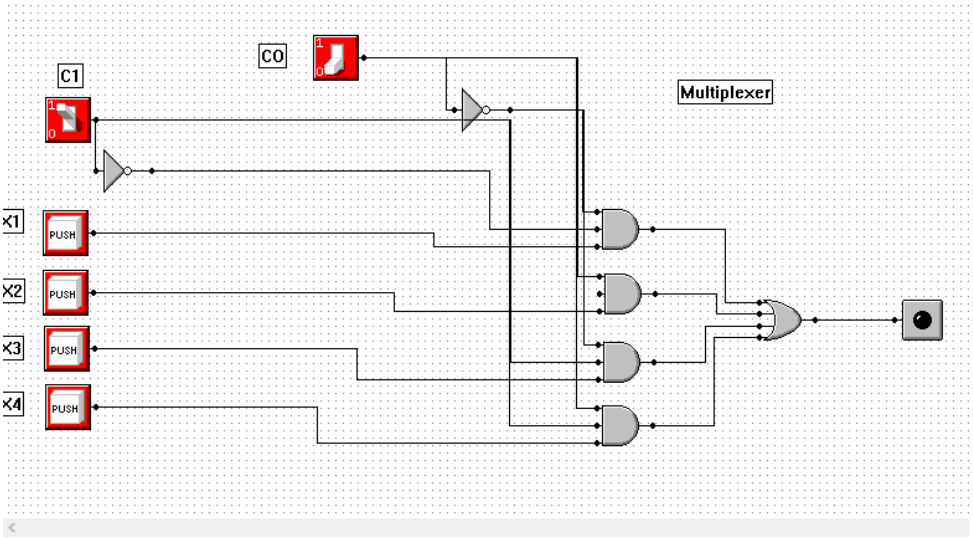


3) Binary Decoder



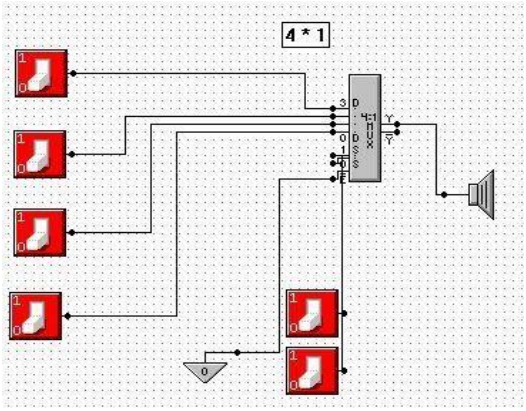
X0	X1	ENABLER	Y0	Y1	Y2	Y3
0	0	1	1	0	0	0
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	1

4) Multiplexer



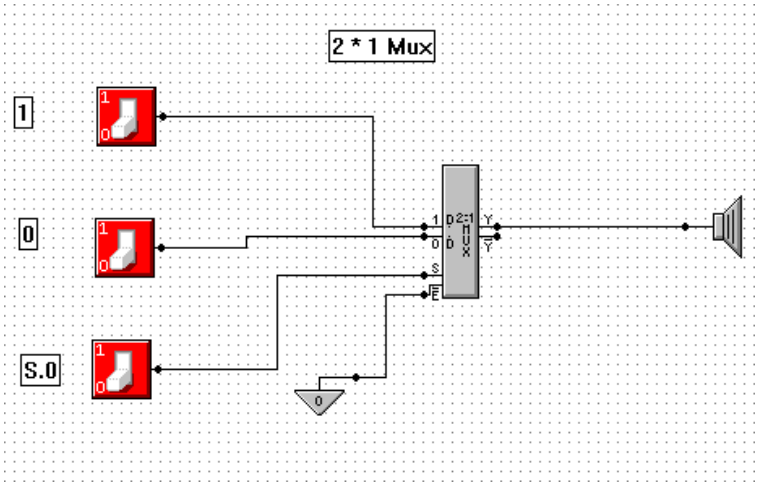
C1	C2	X	M
0	1	0 X1 1	0 1
0	0	0 X2 1	0 1
1	1	0 X3 1	0 1
1	0	0 X4 1	0 1

5) 4 to 1 mux



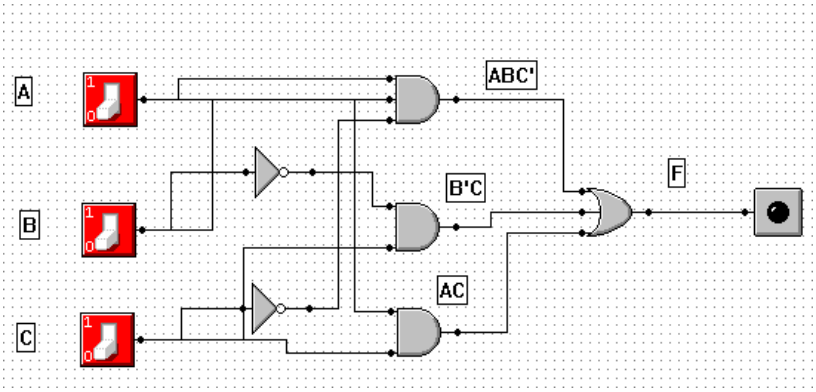
S0	S1	D0	D1	D2	D3	Y
0	0	0	X	X	X	0
0	0	1	X	X	X	1
0	1	X	0	X	X	0
0	1	X	1	X	X	1
1	0	X	X	0	X	0
1	0	X	X	1	X	1
1	1	X	X	X	0	0
1	1	X	X	X	1	1

6) 2 to 1 mux



1	0	S.0	**Y**
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

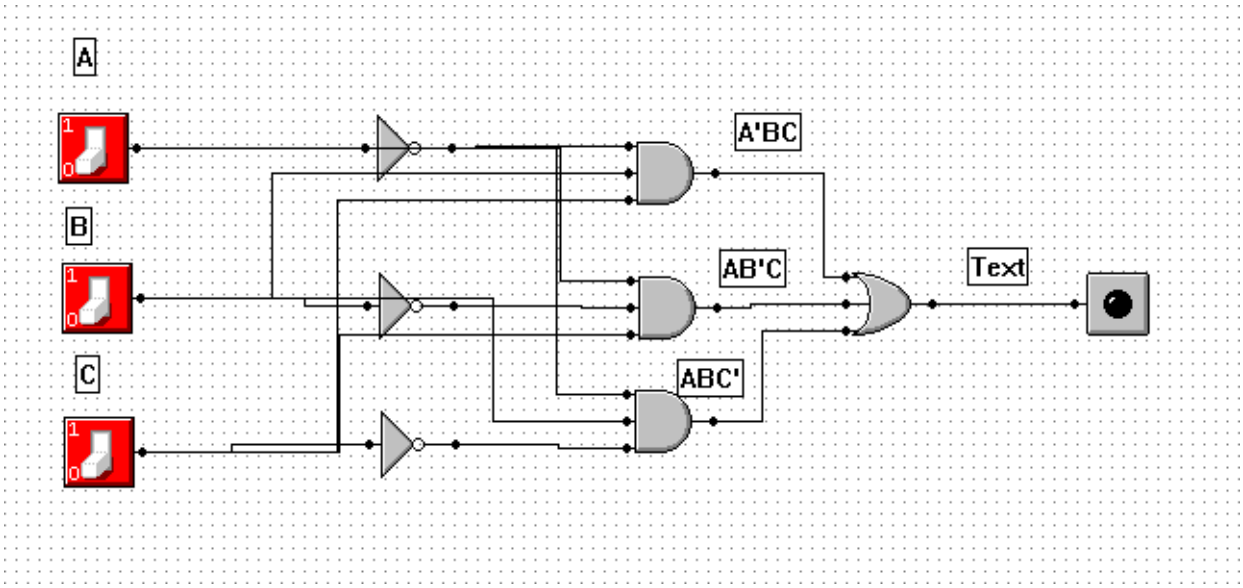
7) F = ABC’ + B’C + AC



8)

A	B	C	OUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

F = A’BC + AB’C + ABC’



9)

	A	B	C	0UT
0	0	0	0	0
1	0	0	1	0
2	0	1	0	1
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	0
7	1	1	1	1

F = A’BC’ + A’BC + AB’C + ABC

F = A’B(C’ + C) + AC(B’ + B)

F = A’B + AC