DANG NGUYEN

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Ambitious engineer with industry experience undergoing graduate program. Looking for opportunities doing Digital Circuit Design within an Embedded environment.

TECHNICAL SKILLS

- Digital Signal Processing
- Image Processing
- Switch Mode Power Supply Design
- Computer Architecture
- Linux Kernel Development
- Synopsys VCS
- PADS/Altium
- Verilog, SystemVerilog, UVM
- C/C++, Python
- MATLAB

EDUCATION

- **San Jose State University**
  M.S. Electrical Engineering, 2021 *GPA 4.0*

- **University of California, San Diego**
  B.S. Electrical & Computer Engineering, 2015

LinkedIn

www.linkedin.com/in/dang-nguyen-a4955366

Github

https://github.com/VimfulDang

PROFESSIONAL EXPERIENCE

San Jose State University, EE Dept San Jose, CA
Student Teacher Associate August 2020 – Present

- Instructed undergraduate embedded laboratory course using TI Robotic Learning Kit. Responsibilities in addition to lab instruction are offering advices, monitoring student performance, and grading lab reports.

Wavestream San Dimas, CA
Electrical Engineer Mar 2018 – Aug 2019

Power Supply Design for 40W Ku Airborne Transmitter

- **Designed Boost, Buck-Boost, and Buck Switch Mode Power Supply Converters -** Responsibilities consisted of simulation in LTSpice, drafting schematic in Altium, collaborating with PCB designer in PCB board design, component derating analysis, and verified design intents of PCB Assembly.

- **AC/DC converter Design Refresh** - consisting of EMI Filter, Diode Bridge Rectifier, and PFC boost converter - Responsibility consisted of updating existing schematic drawings, simulating circuit functions to meet DO-160 Airborne Environmental system specifications.

MaXentric Technologies, LLC La Jolla, CA
Design Engineer June 2015 – Feb 2018

- **LabView Test Automation for Evaluation and Integration of CoTS RFPA Devices -** Designed LabView program incorporating RF Signal generators, power supplies, Spectrum Analyzers to automate DC Test and Constant Wave Characterization of RF Power Amplifiers in terms of Psat, Gain, Power-Added-Efficiency, Drain Efficiency vs Drain Voltage.

- **Envelope Tracking RFPA System**
  Evaluated and integrated CoTS products along with prototype devices to achieve high efficiency and linearity of RFPAs operations under a wide range RF center frequencies, bandwidth, and Peak-Average Power Ratio (PAPR) with Envelope Tracking.

PROJECTS

- **Scientific Calculator implementation on FPGA DE10-Lite** – Simple calculator performing operations such as add, subtract, multiply, division, cosine, and sine. FSM design simulation conducted on VCS Synopsis and implementation using Intel Quartus Prime on FPGA DE10-Lite.

- **Pipeline MIPS CPU Design Performing Dot Product with Forwarding in Verilog –** Designed 5 stage pipeline CPU with Forwarding logic to compute dot product using limited instruction set. Simulated using Verilog and Synopsis VCS.

- **Stopwatch Linux Kernel Driver on DE1-SOC FPGA–** Implemented a stopwatch as a Linux Kernel Driver with C programming where the timer is tracked by a hardware clock, time is displayed on Seven-Segment display, and the timer is set with switches and buttons. A test script was developed to test kernel functionality through user space filesystem.

- **Canny Edge Detection Algorithm in C on Linux –** Project intakes a bitmap image and applies a series of image processing operations to output an edge pixel map. Some operations such as Gaussian blurring to remove image noises, Sobel operator to obtain the gradient, and non-maximum suppression & hysteresis to emphasize edges