Vinay Desai

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SUMMARY

Hardware Design Engineer with 4 years of dedicated experience, I have played an integral role in the end-to-end hardware product development process for networking equipment. My expertise spans across various critical aspects, including architectural design, specification development, schematic captures, power consumption estimation, signal integrity analysis, layout review, test plan development, board bring-up, and rigorous debugging. My proven track record in these areas reflects my commitment to delivering innovative, high-quality solutions in the realm of hardware design.

EDUCATION

Institute of Technology, Nirma University, Gujarat **May 2016 - May 2020**
Bachelor of Technology in Electronics and communication - Grade: A (8.4/10)

Institute of Technology, Nirma University, Gujarat **May 2017 - May 2020**
Minors in Computer Science - Grade: A (8/10)

TECHNICAL SKILLS

- **System Design:**
  - Strong EE fundamentals with expertise in designing complex FPGA/ASIC/Embedded processors for networking systems.
  - Proficient in High-Speed SerDes Board design (>10G).
  - Proficient in creating detailed schematics using Altium and Cadence tools.
  - In-depth understanding of PCB technologies and layout review.
  - Knowledgeable in power supply design, voltage regulation, efficiency, and power distribution on the PCB.
  - Expertise in board bring-up, testing, and debugging of analog and digital circuitry.
- **Automation & Programming:**
  - Proficient in scripting using Python, Perl, Linux, and Tera Term.
  - Proficient in C/C++ and Hardware Descriptive Languages Verilog and SystemVerilog.

PROFESSIONAL EXPERIENCE

Hardware Design Engineer 3 **Nov 2022 – Present**
Juniper Networks, India

- Currently working on Juniper's next-generation PTX series routers. These systems are based on QSFP112 & SFP112 optical modules.
- Worked with a PLM team to identify customer requirements and build hardware functional specs for the product.
- Worked with the component engineering team in choosing appropriate components based on performance, cost, and availability, and evaluating their suitability for the design.
- Worked on designing the schematics for the system's SFP112 board, which includes high speed SerDes lanes and SFP112 ports.

Hardware Design Engineer 2 **Dec 2021– Nov 2022**
Juniper Networks, India

- Worked with a PLM team to identify customer requirements and build hardware functional specs for the product.
- I designed the schematics for the system's main board, which includes high speed SerDes lanes and 400G ports.
- To release the product, I collaborated with a cross-functional team (SI, FPGA, Mech, PCB, Power, EMI, Manufacturing).

- Worked on developing testing prototypes, as well as developing comprehensive test plans and procedures for design verification.

Hardware Design Engineer 1 **July 2020 – Dec 2021**
Juniper Networks, India

- Contributed to the development of Juniper's next-generation ACX7100 series enterprise switching products.
- Worked on building a hardware test strategy for the test team to do resiliency testing.
- I contributed to the debugging of critical issues such as an uncorrectable fatal error on the PCIe link between the CPU and the switching fabric.
- I have developed several test scripts and tools for testing and data analysis using Python/shell scripting.

Hardware Design Intern **Jan 2020 – June 2020**
Juniper Networks, India

- Worked on Juniper's PTX1000-36MR series routers having data routing capabilities of 14.8 Tbps.
- Validated high-speed interfaces, clocks, and reset signals by capturing waveforms for various components on the forwarding plane board.

Internship Trainee **May 2019 – July 2019**
Oil and Natural Gas Corporation Ltd

- Received Training and Certification from Infocom Services, ONGC Ahmedabad Asset, where I have done in depth research about BWA (Broadband Wireless Access Control) and SCADA (Supervisory control and data acquisition).

ACHIEVEMENTS

- **Department Spotlight Award** for my contributions to resolving the 400G FEC Error issue in the PTX Routing Platform. **- Sep 2021**
- **Best Paper Award** at JTC 2021 for the paper titled 'Impact of Traffic Type and Ambient Temperature to Optimize Network Infrastructure Power Efficiency'. **- Dec 2021**
- **CEO Excellence Award** for my contributions to the development of ACX7100 Series routers. **- Feb 2022**
- Built python-based tool to automate power consumption measurements of networking systems. **- Mar 2023**
- Worked on creating a framework for characterizing router's power consumption to create power estimation calculator using ML. **- Sep 2023**

ADDITIONAL INFO

- **BTech Projects**
  - Link to all the projects : <Add Link>

- **Online Courses:**
  - Introduction to FPGA Design for Embedded Systems - Coursera - Dec 2021
  - Gold Badge in Python Programming - HackerRank - Oct 2021
  - Using Python for Automation - Linkedln - Jan 2021
  - Learn PCB Design - Udemy - March 2020

- **Management Skills**
  - Ability to manage NPI hardware projects, including planning, scheduling, resource allocation and working with cross-functional teams (SW, Power, SI, PCB, MFG, Test).

- **Technical Event Organizer & Graphics Head at ECO, Nirma University**
  - Coordinated a variety of technical events held by ECO throughout the academic year.
  - Designed newsletters and magazines for ECO - Link to Newsletter.