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**Lab 07 Report**

Ryan Beck

Jared Bronson

**Objectives**

For this lab, interface the FPGA development board to a standard computer monitor using the VGA protocol and hardware. Display the national flags of the 12 given countries. The design will use the two push buttons, the on-board clock, and the VGA. One push button will be used as “reset” to display the first flag. The other push button will be used as “advance”, to display the next flag.

**Procedures**

Create a Finite State Machine(FSM) with states for the A, B, C, D, Clear, and Debounce. States A, B, C, and D correspond to the horizontal front porch, sync, back porch, and data. The vertical timing is determined when the line count increases after going through the four horizontal states.

Using the system builder, create a Quartus Project File with the VGA, the on-board clock, and the two push buttons. Take the generated Verilog file and create a VHD file with matching port names. Take the Verilog file out of the project after creating the VHD file. In the generic, create values for the pixel count of each horizontal state, the line count of each vertical state, the flag count, and the delay for debouncing.

In the architecture, create variables for pixel count and line count to keep track of both vertical and horizontal values. Create a variable to keep track of which flag is displayed and variables to pass the flag color values into the VGA. Then, a type needs to be declared for the state type to create the FSM.

Define a process for the on-board clock. In this process, on the rising edge of the clock, the next state of the state machine becomes the current state unless either of the buttons are pushed. When the push buttons are pushed, the current state goes to the state of the corresponding button.

Define another process sensitive to the state, pixel count, line count, flag count, and push buttons. This process will have a case statement to define what moves states in the FSM. The Clear state will reset all variables to their default values, and sets the state to A. The Debounce state will have a delay to ensure the FSM does not go to the next state if the button is falsely triggered, and increments the flag count so the next flag is displayed. After the advance button is released, the state is then set to A.

State A is the “Front Porch” of the horizontal timing. This state will start the pixel count at 15, and count down each clock cycle. When the pixel count reaches zero, the state is set to B. State B is the Vertical Sync in the horizontal timing. This state will drive the Horizontal Sync signal low, count down from 95. The next state, C, is the “Back Porch” in the Horizontal timing. The pixel count will start at 47 and count down each clock cycle. On the transition from state C to state D, the first color values of the VGA will be set, to ensure the data is being driven at the correct time. In state D, pixel count will start at 639 and count down. Colors will only be displayed on the VGA if the vertical timing has reached the data portion. Create another case statement inside state D to display the colors on the VGA.

The vertical timing will increment when the FSM cycles back to state A. The vertical “Front Porch” lasts 10 cycles, the sync lasts 2 cycles, the “Back Porch” lasts 33 cycles, and the data lasts 480 cycles. Data can only be sent to the VGA when the vertical timing is in the data portion. To ensure the FSM runs at the refresh rate of the VGA, 25 MHz, the FSM will only execute instructions every other clock tick.

**Results**

The VGA file, shown in figures, successfully displays flags on a VGA monitor using the DE10-Lite board. The design creates an FSM to implement proper timing for the pixels and the lines of the display. Push buttons are used to go back to the starting flag and cycle through the 12 required flags.

**Conclusion**

In conclusion, we were able to implement an FSM on the development board to display different flags to a standard computer monitor. One push button resets all values and returns the display to the beginning flag. The other push button advances the display to the next flag. The FSM updates at a rate of 25 MHz. This is done using the on-board 50MHz clock, and only executing on every other clock tick.

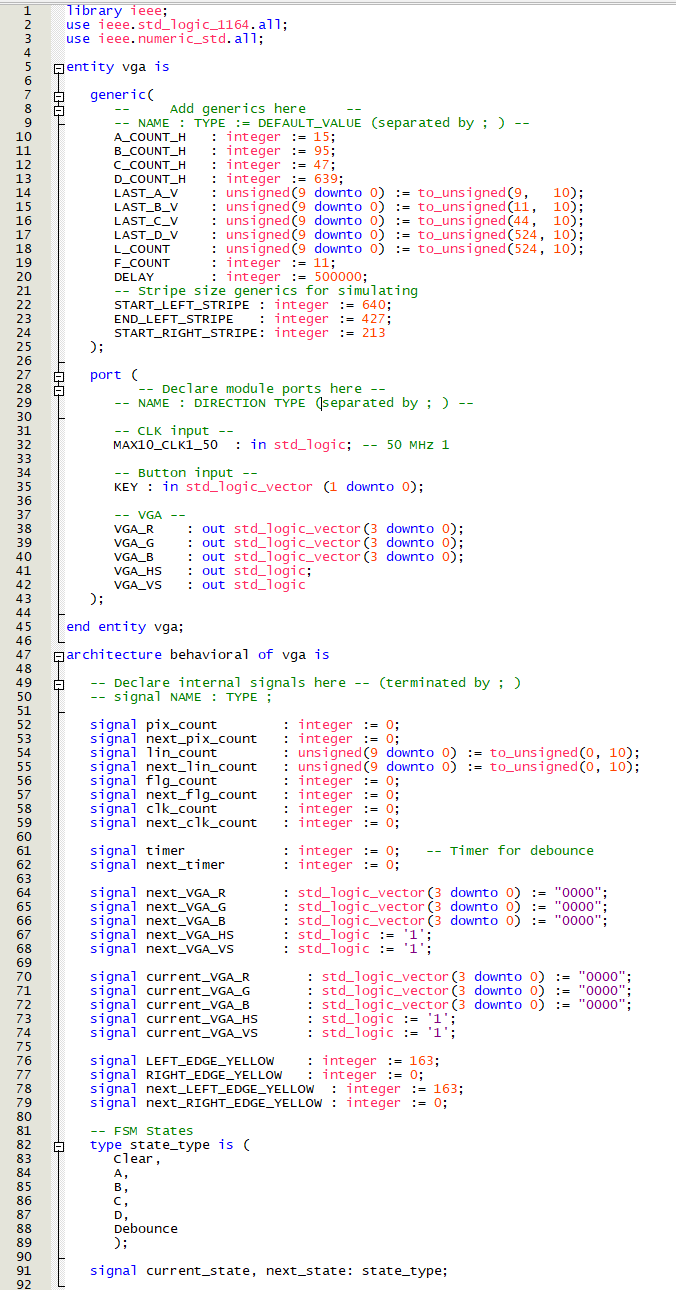
**Figures**

Figure 1: VGA.vhd Pt 1

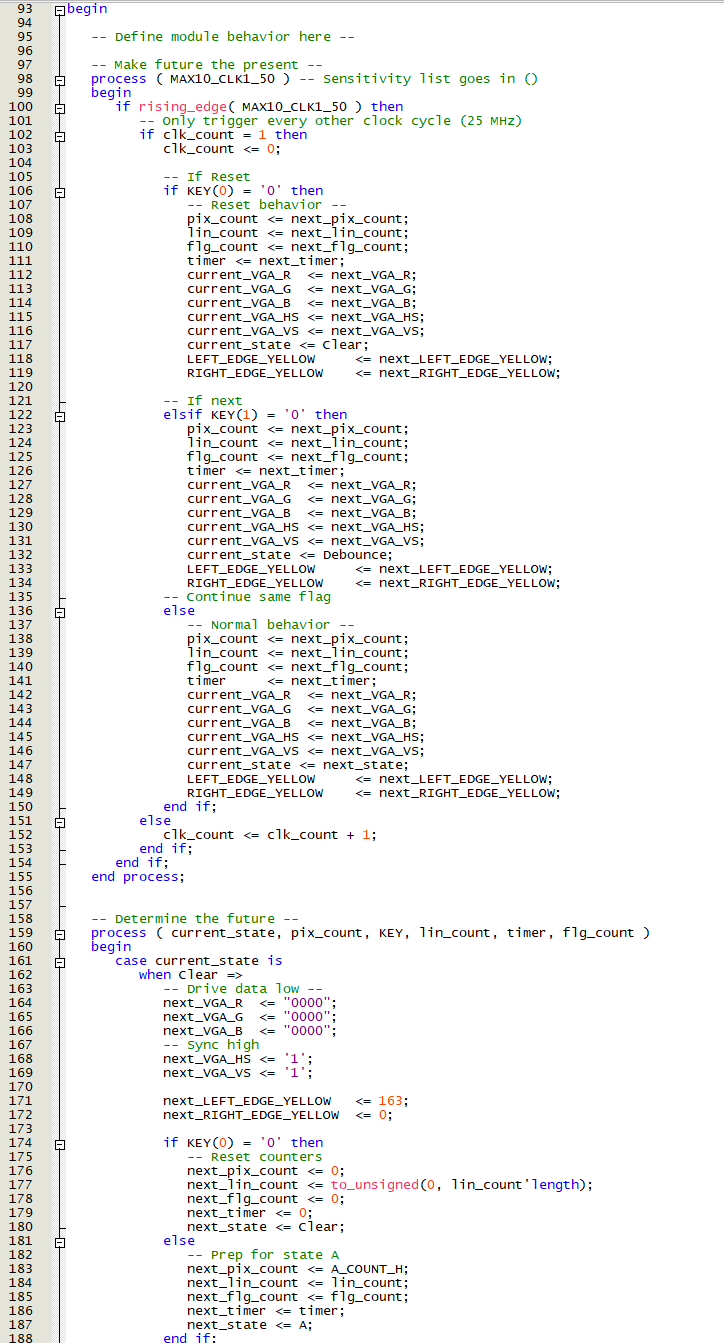


Figure 2: VGA.vhd Pt 2

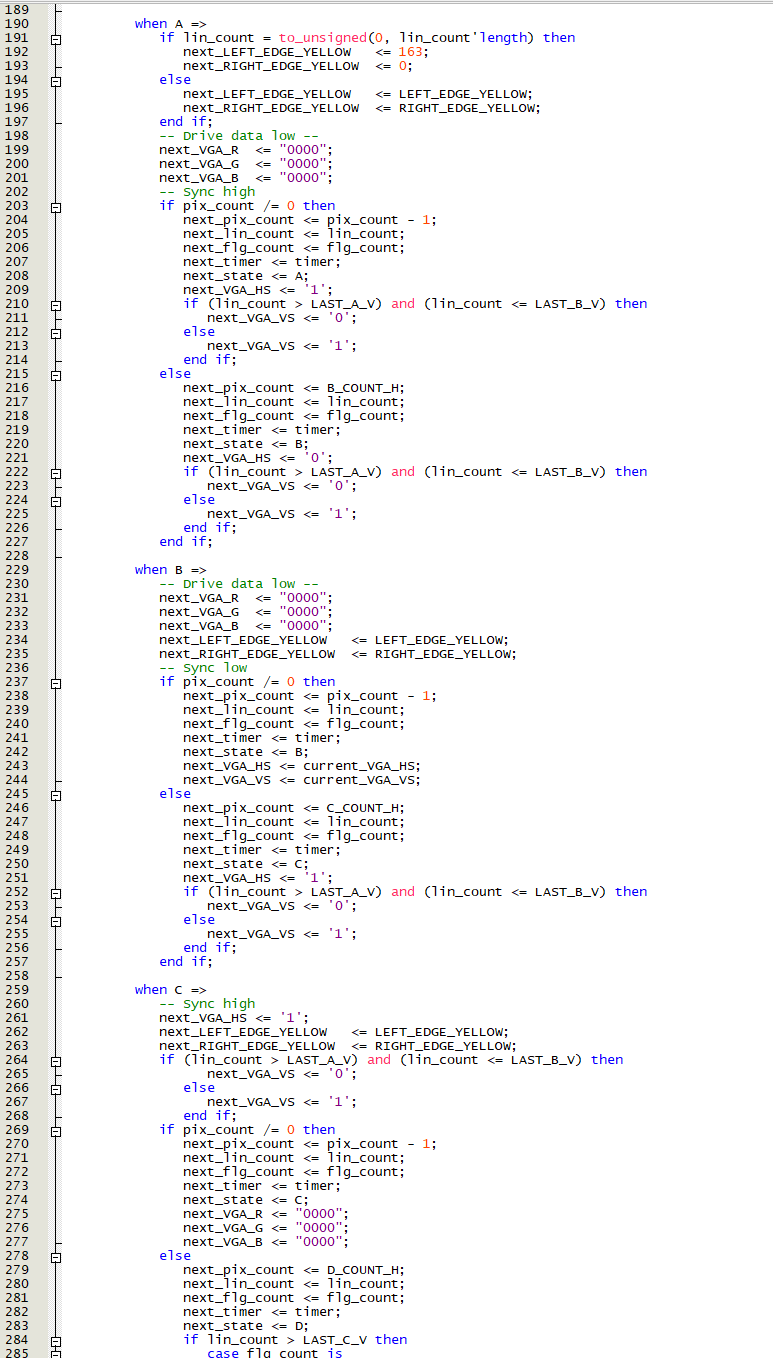


Figure 3: VGA.vhd Pt 3

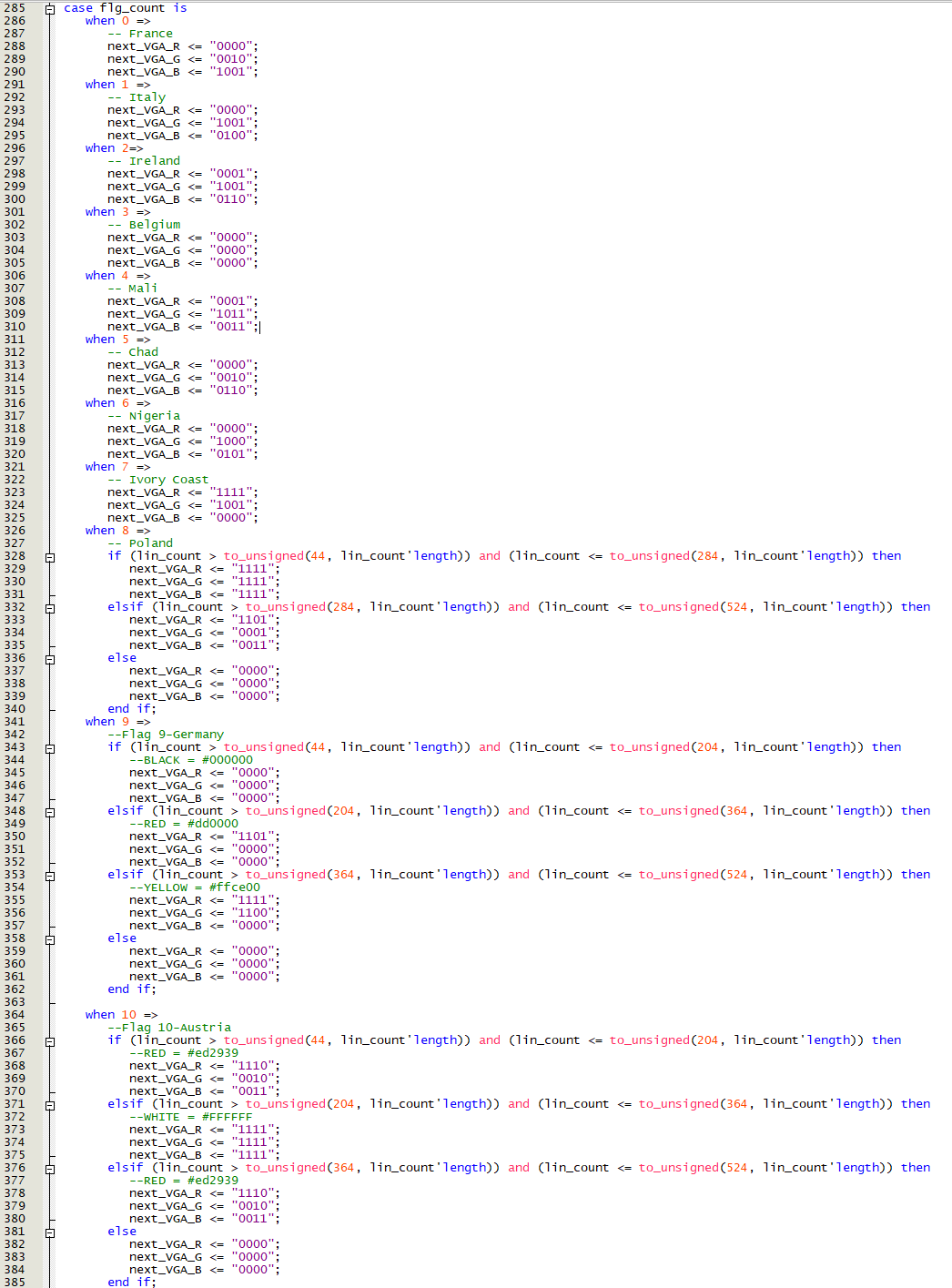


Figure 4: VGA.vhd Pt 4

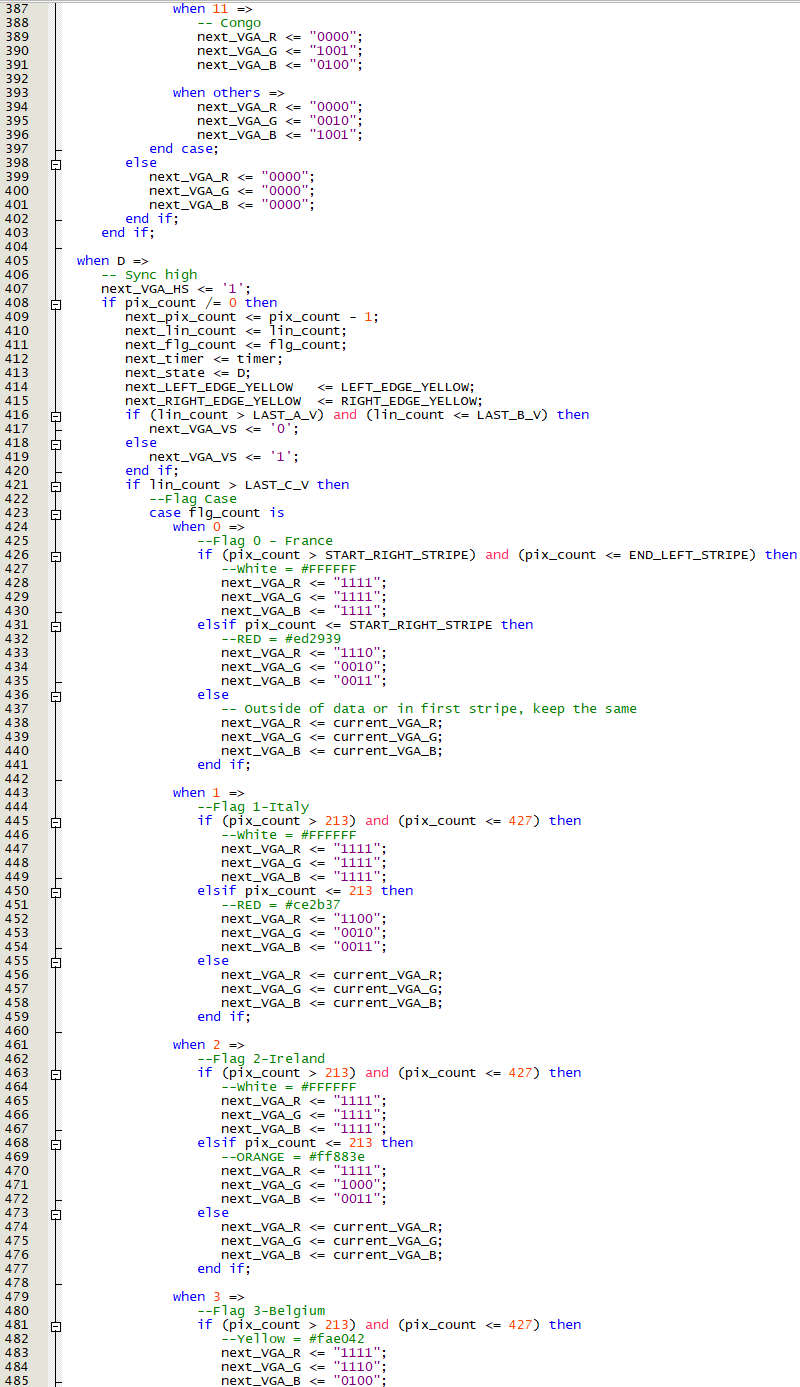


Figure 5: VGA.vhd Pt 5

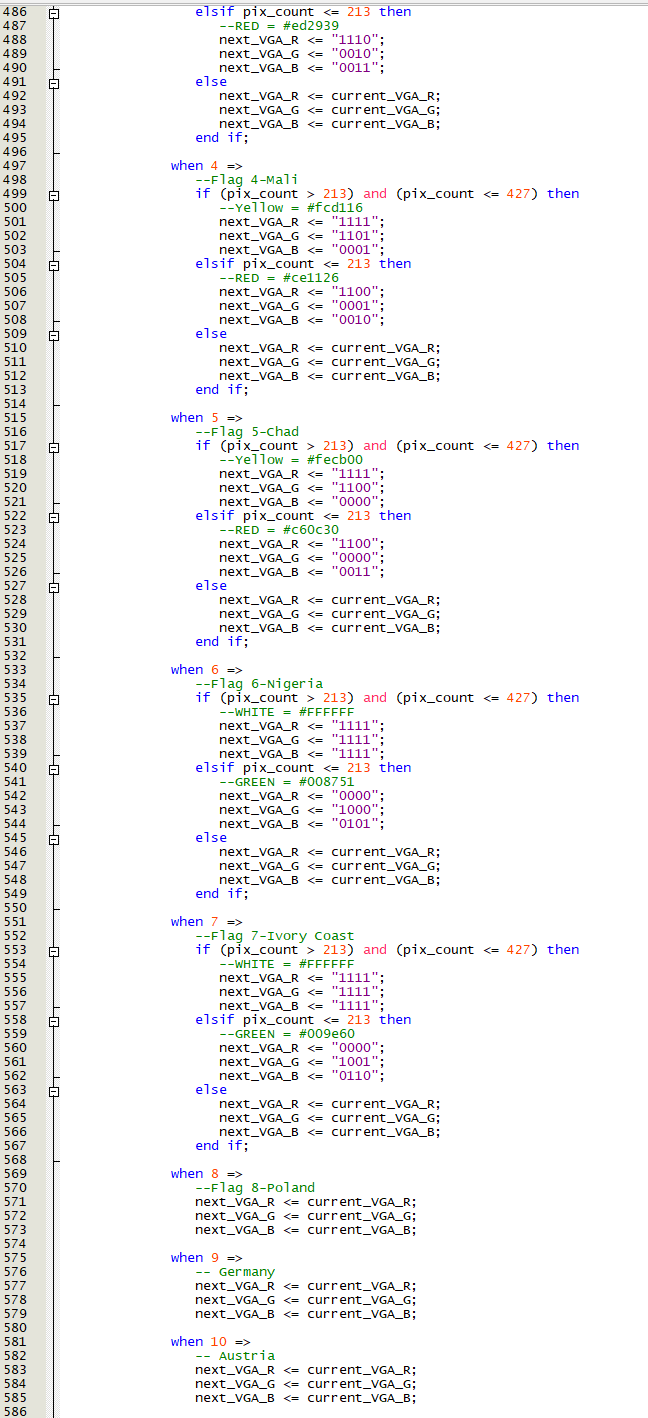


Figure 6: VGA.vhd Pt 6

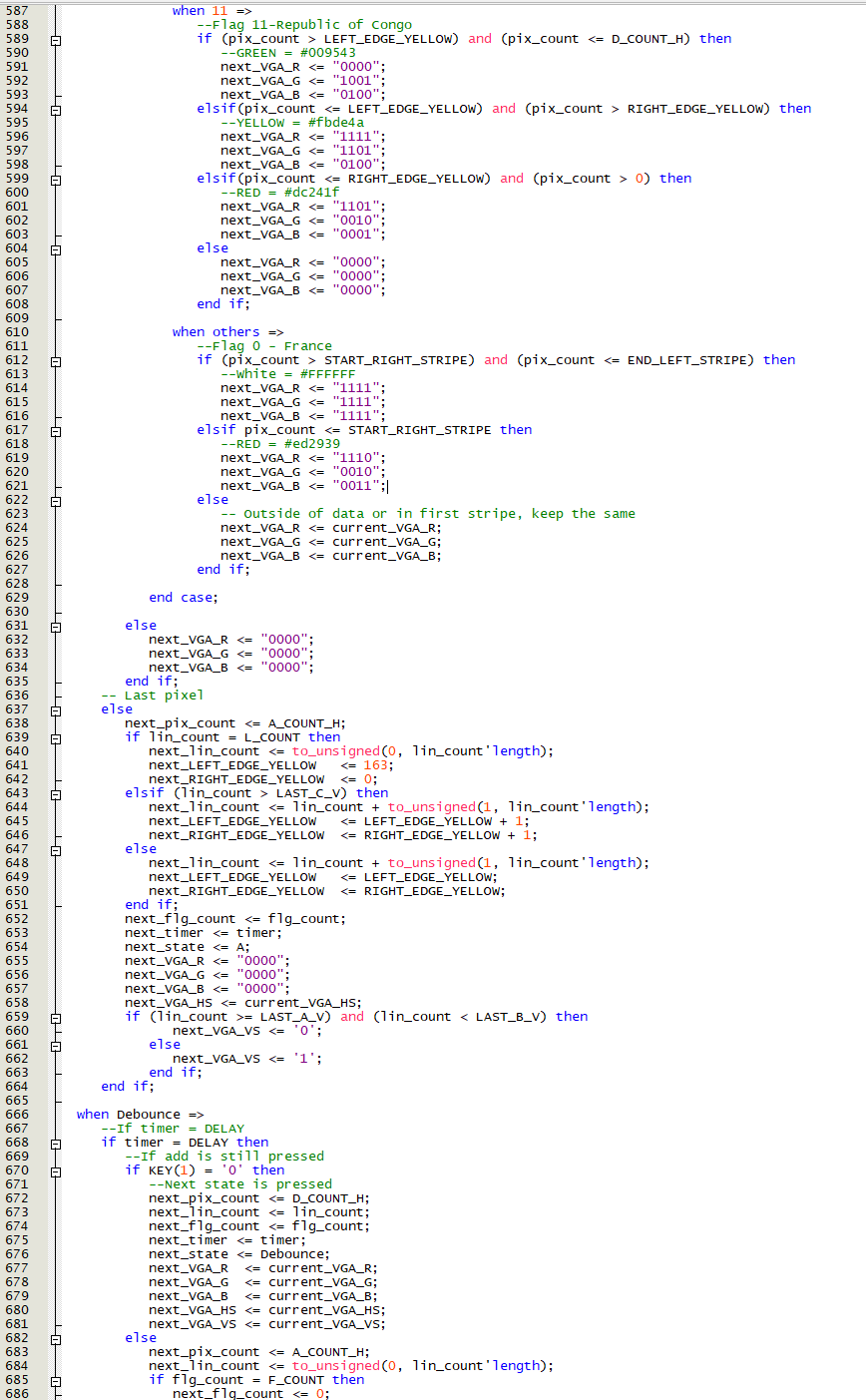


Figure 7: VGA.vhd Pt 7

A screenshot of a computer program

Description automatically generated Figure 8: VGA.vhd Pt 8

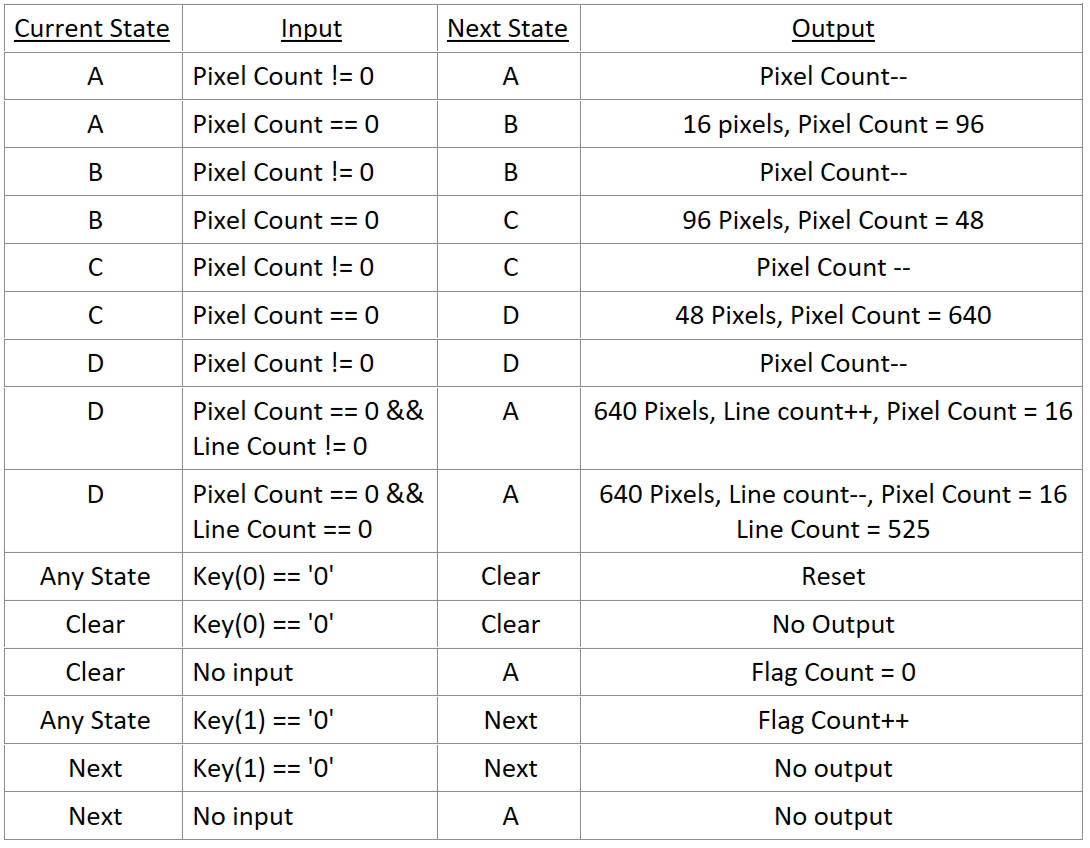


Figure 9: VGA Finite State Machine