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22ECP310: Project Lab-1

(V Semester)

Department of Electronics and Communication Engineering

Low-Dropout Regulator

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INTRODUCTION

Generally, advancement of power management within the electronic industry has been through the miniaturization of modern devices. In this regard, the development makes the devices smaller while complicating the management of the power. There has not been an improvement in the efficiency of the batteries that accompany the devices, leaving a gap between the energy storage available and the demands for power. Thus, good solutions of power management are necessary for proper operation and performance by the integrated systems.

Low Dropout (LDO) voltage regulators have emerged as a very impressive solution of power regulation, which ensures that power management is done with the minimum possible difference in voltage. LDOs are linear regulators, meaning they require a minimum difference between the input and the output in terms of voltage to ensure that proper regulation of voltage takes place.

LDO voltage regulators have become a core part of many portable power systems. They are highly sought since they provide stable output voltage even against variations in load impedance and temperature, as well as changes in the input voltage. In fact, this will be very important to achieve safe operations of sensitive electronic components, especially the ones contained in battery-driven devices where a very stable power supply is required.

One of the useful properties of LDOs is that they work with an extremely low dropout voltage and therefore prove quite useful to power sub-circuits in a system which possesses very low supply voltages. LDOs automatically evolve in modern design schemes because the trend towards utilizing the lower voltage supplies would have enhanced energy efficiency for extended periods of life for the cells in question. Because of this low dropout nature, thus they are suitable for stable operation; in other words, even in systems with lower voltage headroom, the low dropout reduces overall power consumption and improves efficiency in energy throughout the device.

Another important feature of LDOs is that they can minimize the current consumption, especially in those systems that consume less power when in idle or sleeping modes. LDOs extend the life of a portable's battery even further by minimizing power drain when the device is idle, since it does not have to draw as much from the battery. Multiple levels of LDOs can provide multiple levels of voltage and come in handy when one design of SoC will include multiple components operating on a different voltage level. The ability to provide a stable multiple voltage output through a single LDO regulator helps keep the design simpler as it reduces dedicated multiple voltage regulators needed in attaining overall system efficiency.

Another important advantage of LDOs is rejection or supply voltage noise suppression, most importantly in the cases where noise immunity is critical. LDOs can protect the internal sensitive

circuits from the noise of the power supply very efficiently; hence, high-performance components such as microprocessors or RF circuits are not interfered. It is a very significant function in portable devices where space is a constraint and thus cannot add filtering components; hence, the LDO becomes the solution that can ensure clean power delivery.

LITERATURE REVIEW

Low-Dropout Regulators (LDOs) have been a key focus in power management research due to their simplicity and effectiveness in providing stable output voltages with minimal input-to-output differentials. Early designs established the fundamental architecture using a pass transistor and an error amplifier, but challenges such as noise performance, transient response, and stability pushed the boundaries of innovation. Recent advancements, such as those highlighted in Darshil Patel's work, emphasize achieving low noise and fast set-up times through advanced compensation techniques and robust op-amp designs. With the growing demand for portable and battery-operated devices, researchers have also focused on low-voltage LDOs, introducing methods like adaptive biasing and dynamic current boosting to enhance efficiency and response. These developments have enabled modern LDOs to deliver high precision and reliability while maintaining a compact design. Our project builds on this body of work, aiming to design and evaluate LDOs that address these challenges. By focusing on key performance metrics like noise suppression, load regulation, and transient response, and by incorporating individual op-amp design methodologies, we aim to contribute to the ongoing pursuit of efficient and high-performance power management solutions.

LOW DROPOUT REGULATORS

Basics Theory of LDOs

A low-dropout regulator (LDO regulator) is a type of a DC linear voltage regulator circuit that can operate even when the supply voltage is very close to the output voltage.

A “linear” series voltage regulator typically consists of a reference voltage, a means of scaling the output voltage and comparing it to the reference, a feedback amplifier and a series pass transistor (bipolar or FET), whose voltage drop is controlled by the amplifier to maintain the output at the required value.

There are a few types of linear voltage regulators which can be divided into series, shunt, and LDO. LDO is the most widely-used voltage regulator in CMOS technology due to its superior functionality performance. The dropout voltage is the minimum voltage required across the regulator to maintain regulation. The advantages of an LDO regulator over other DC-to-DC voltage regulators include: the absence of switching noise ; smaller device size; and greater design simplicity. It consists of a reference, an amplifier, and a pass element.

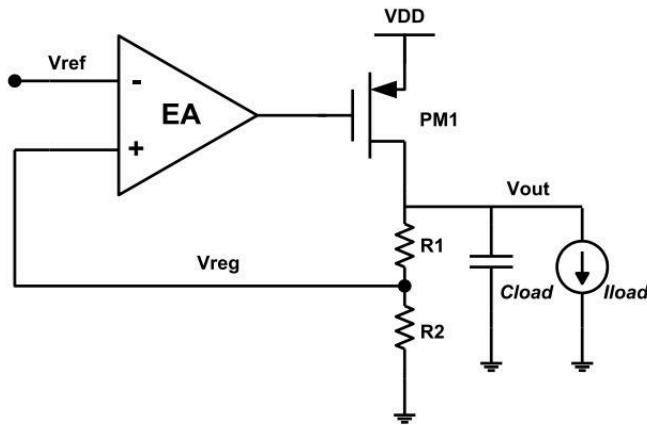


Fig. The basic architecture of the classic LDO

LDO Topology

There are mainly three types of LDO topologies:

1. Analog LDO
2. Digital LDO
3. Hybrid LDO

1. Analog LDO

Analog LDO provides a superior transient response and achieves a high PSRR due to the large external capacitor . The external capacitor consumes a large circuit area and indirectly increases the production cost.

To mitigate the stability issue without the use of a large output capacitor load in the zero-pole feedback system, the ALDO needs to drive the logic circuits near-threshold or subthreshold voltage (NTV).

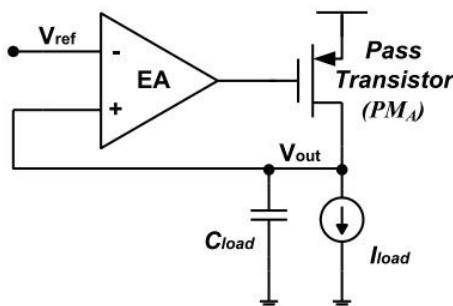


Fig. ALDO

2. Digital LDO

A Digital LDO in a synchronous circuit that consists of a sampling clock, FCLK at the comparator, and feedback to the quantizer which also acts as a clock controller and DLDO switching nature causes output ripple which affects LDO PSRR.

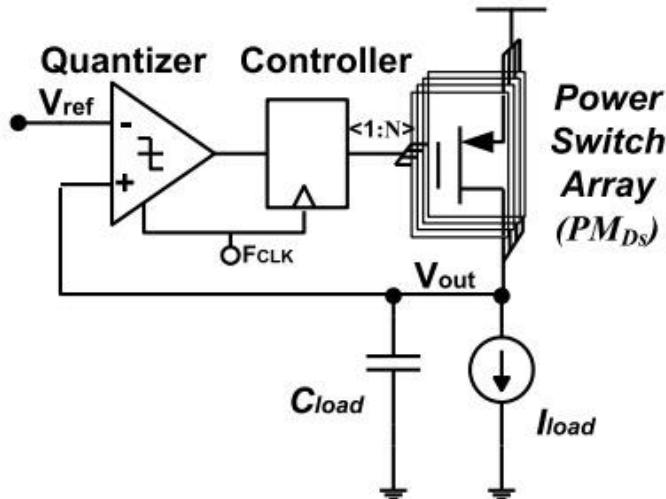


Fig. DLDO

The ALDO offers superior PSRR performance with low output ripples, while a DLDO exhibits excellent large signal transient response with a small regulator size and greater reliability.

3. Hybrid LDO

A Hybrid DLDO is an advanced power regulation and combines the precision and stability of an Analog LDO (ALDO) with the scalability and fast transient response of a Digital LDO (DLDO). This hybrid approach leverages digital control mechanisms for rapid response to load changes while maintaining analog feedback for enhanced stability and low output ripple. As CMOS technology scales into submicron ranges, traditional ALDOs face challenges such as insufficient voltage headroom, reduced loop gain, and degraded performance, making them less suitable for low-power applications. The hybrid DLDO addresses these trade-offs, making it an attractive choice for achieving high efficiency, better process scalability, and reliability in compact, low-voltage designs.

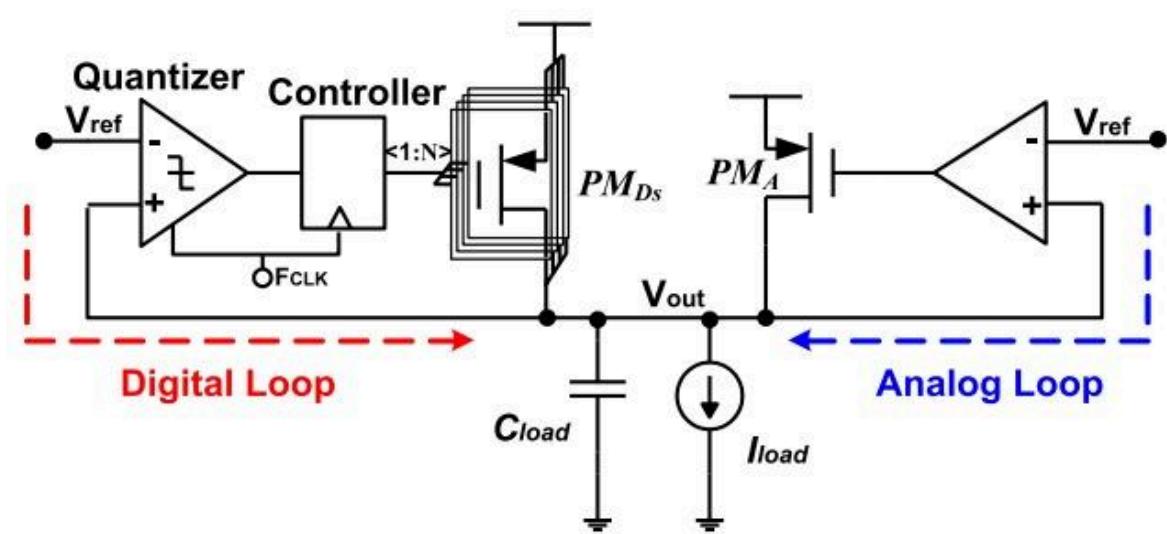


Fig. hybrid LDO

DESIGN PARAMETERS OF COMMON LDO

The dropout voltage is the most important parameter in designing the LDO, as it impacts the overall performance of the LDO. It is defined as the output voltage deviation from the input. An efficient and stable LDO has a small dropout voltage. In an analog LDO, the dropout voltage does not depend on the drain-source resistance (R_{DS}) of the power device when the power device is operating in saturation, but instead is determined by other factors such as the reference voltage, error amplifier, and pass transistor characteristics, it remains independent of R_{DS} . When the analog LDO operates with a heavy load, the power device may enter a triode region where the dropout voltage will be affected by the R_{DS} that changes across the loading effect. On the other hand, DLDOs typically employ power devices operating in the linear region. In this region, the power device acts as a variable resistance, with R_{DS} directly affecting the dropout voltage. Higher R_{DS} leads to an increased voltage drop across the device, resulting in a higher dropout voltage in DLDOs. Hence, the mathematical expression of the dropout voltage

$$V_{\text{DROPOUT}} = I_{\text{LOAD}} \times R_{\text{DS}} \quad (1)$$

where the I_{LOAD} is the load current and R_{DS} is the drain-source resistance at the PMOS switch at the output

The quiescent current, I_Q

$$I_Q = I_{\text{in}} - I_{\text{out}} \quad (2)$$

where the I_{IN} is the total input current used in the DLDO while the I_{OUT} is the output current delivered to the load.

Operational Amplifier

An operational amplifier is an integrated circuit that acts as a voltage amplifier. It has a differential input which consists of a non-inverting input with positive voltage and an inverting input with negative voltage, ideally the op-amp amplifies only the difference in voltage between the two which is called as the differential input voltage and output voltage of the op-amp is typically greater than the potential difference between the input voltages.

Block Diagram

Block diagram of Two stage Op-Amp which consist of two blocks i.e., Differential amplifier in the first stage and common source amplifier in the second stage. Differential amplifier will provide the needed high gain and the Common Source Amplifier provides high output voltage and also further increases the gain.

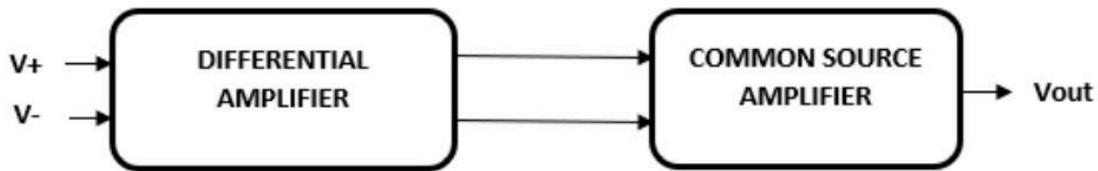


Fig. Block Diagram of Two Stage OpAmp

The first stage of the block diagram is a differential amplifier, which is a type of electronic amplifier that amplifies the difference between two input voltages but suppresses any voltage common to the two inputs. It has two inputs non-inverting voltage (V^+) and inverting voltage (V^-). The output can be either a differential voltage or single ended voltage depending on the input voltages. The output of this is given as the input to common source amplifier. Since the gain provided by the differential amplifier is not sufficient. The second stage of the block diagram which is Common Source Amplifier provides the additional amplification that's necessary.

Design Procedure of Two Stage Op-amp

The 2-stage CMOS operational amplifier shown in figure below consists of two stages one is Differential-input single ended output stage with PMOS current mirror as active load, the differential amplifier have two inputs that is V_{in+} and V_{in-} as first stage and second one is a common-source amplifier output stage to provide more voltage gain because gain provided by first stage is not sufficient and to provide low output resistance common-source amplifier is used. The schematic of two-stage operational amplifier design as shown in figure below contains of a NMOS differential amplifier (MOSFET M1 and M2) with active load PMOS current mirror (MOSFET M3 and M4) as the first stage next comes the second stage, which is made up of PMOS (MOSFET M6) and is common-source amplifier where mosfet M6 works as an amplifier and mosfet M7 works as the current source for biasing. Mosfet M5 and M8 form a NMOS current mirror and are used to bias the circuit to provide proper current and voltages to the circuit.

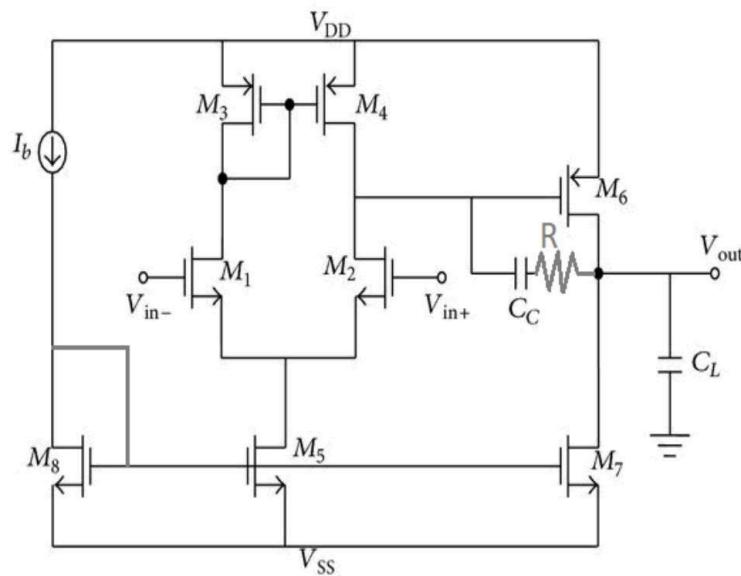


Fig. Two stage CMOS operational amplifier circuit diagram

A feedback capacitor C_c that is connected between the second stage amplifier's input (or called as the first stage amplifier's output) and the second stage amplifier's output is used as a miller capacitance to obtain pole splitting (increasing the distance between the first and second pole) and that will provide better stability, along with capacitor C_c a resistor R that is called as nulling resistor and is connected to provide greater phase margin to achieve greater stability. With the nulling resistor, we can move the RHP (right half plane) zero to infinity and a second option to achieve greater stability is to select R in a way that shifts RHP zero into the LHP (left half plane) such that it can be cancelled with one of the poles. However in this simulation we have chosen

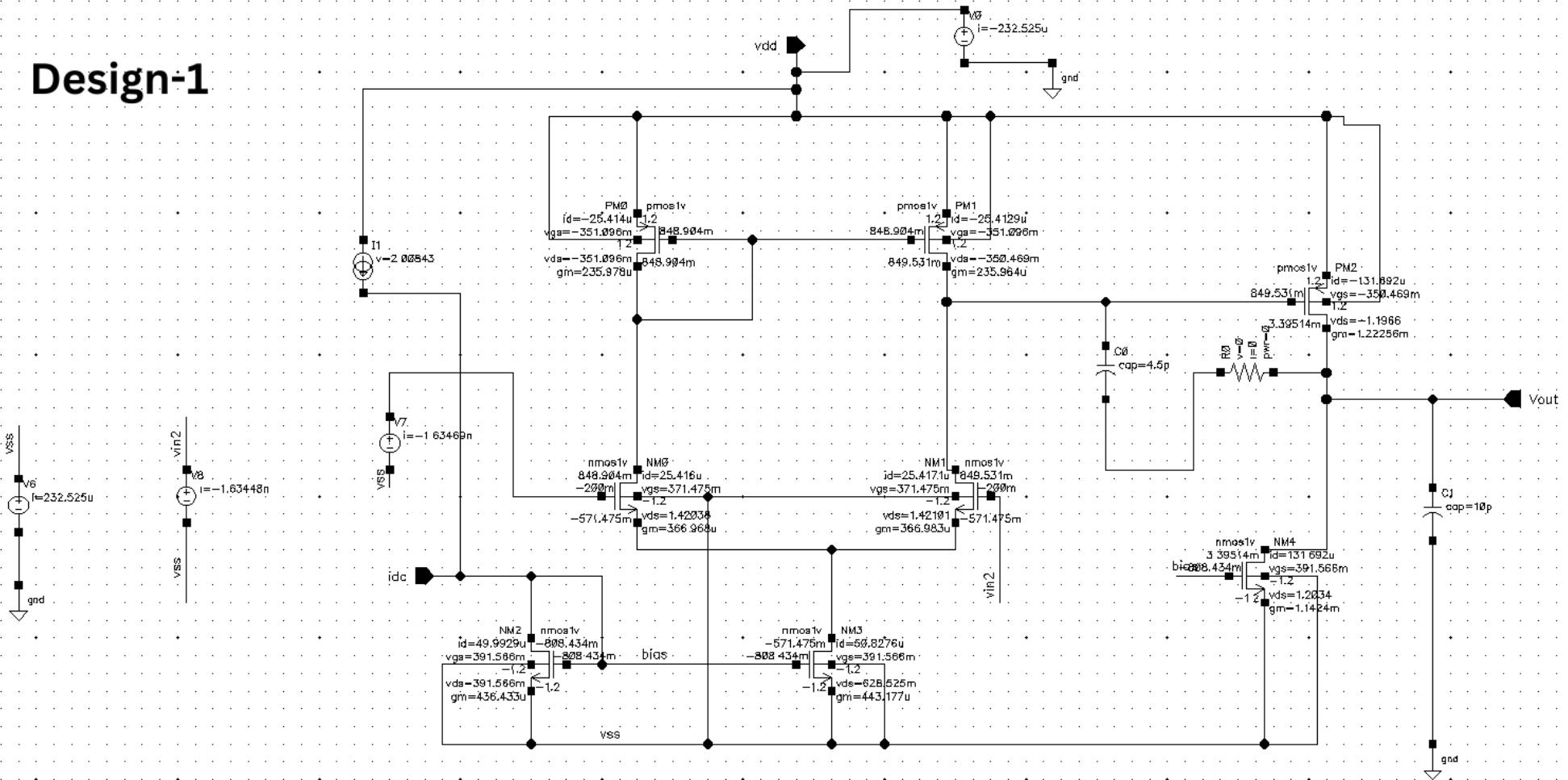
resistor R such that the RHP zero moves towards infinity or practically we can say towards a very higher frequency.

OUR DESIGNS FOR OP-AMPS

Each member of the group has designed one op-amp using various references and obtained the AC response, DC response, transient response, etc. for each design.

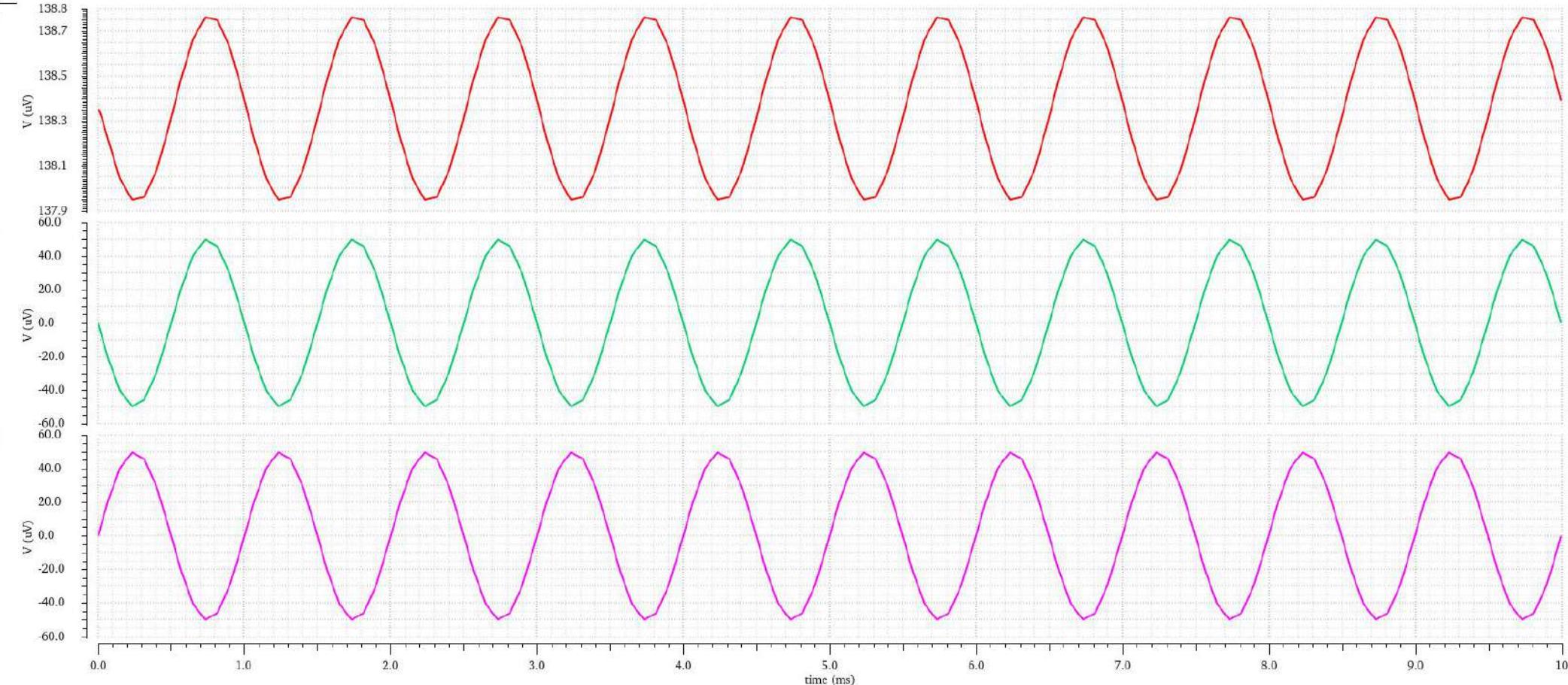
The results are as follows:

Design-1



Transient Response

Name Vis
/Vout

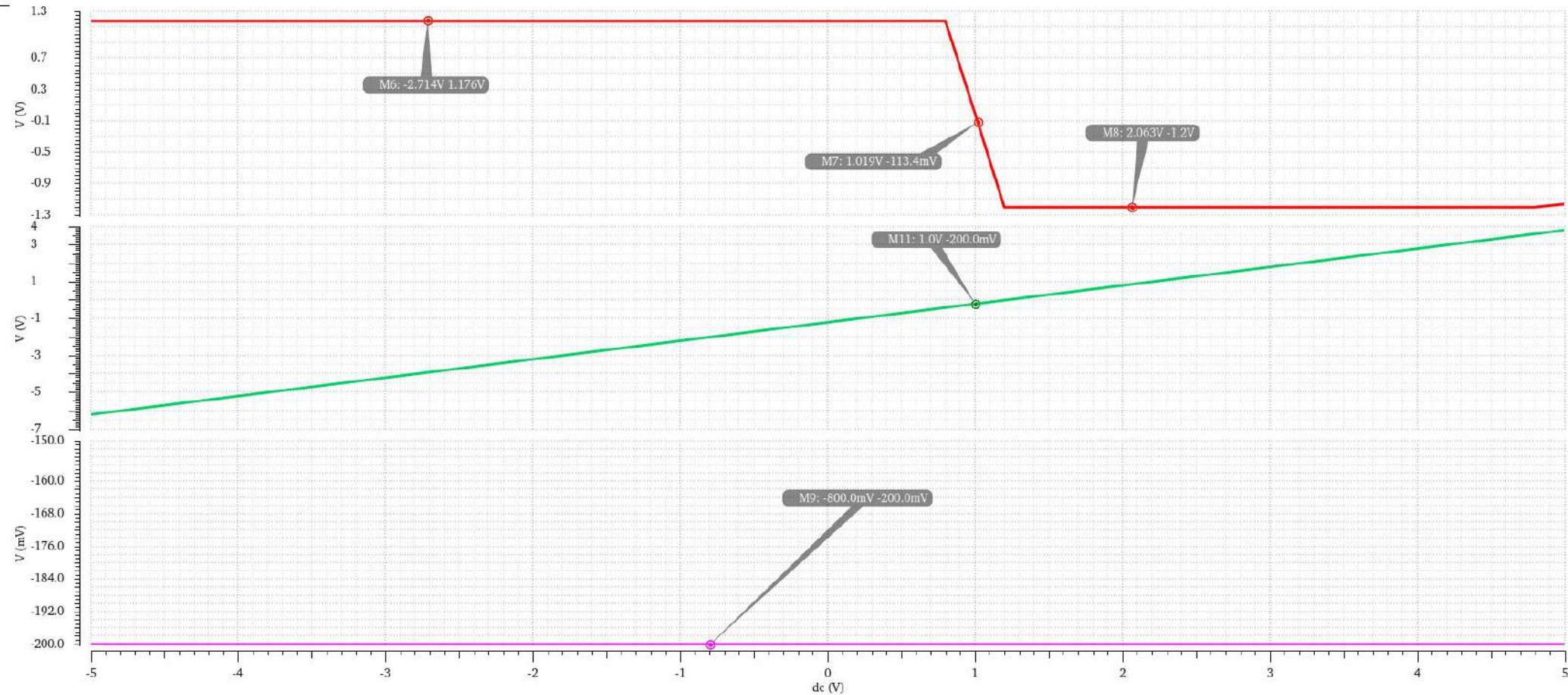


DC Response

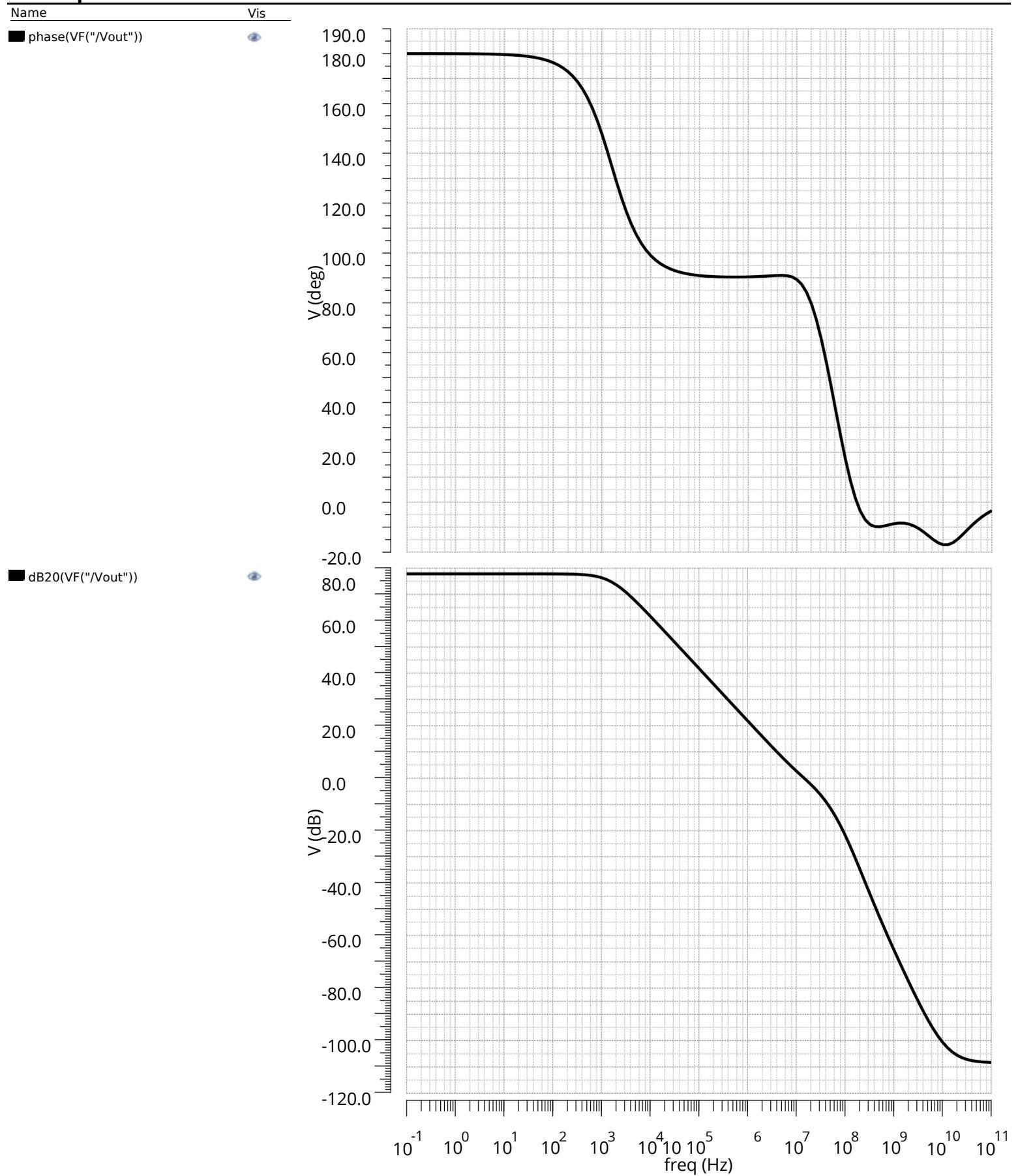
Wed Dec 11 16:09:06
2021Name: V_{in}V_{out}

/net020

/vin2



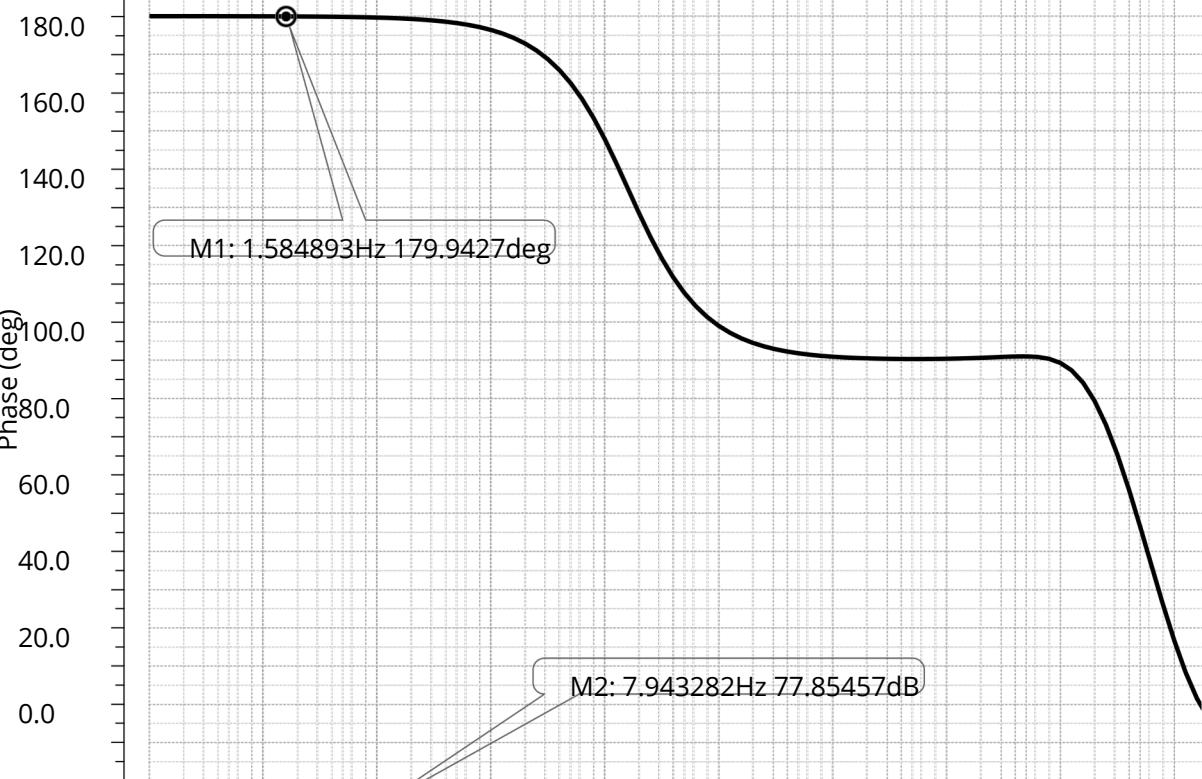
AC Response



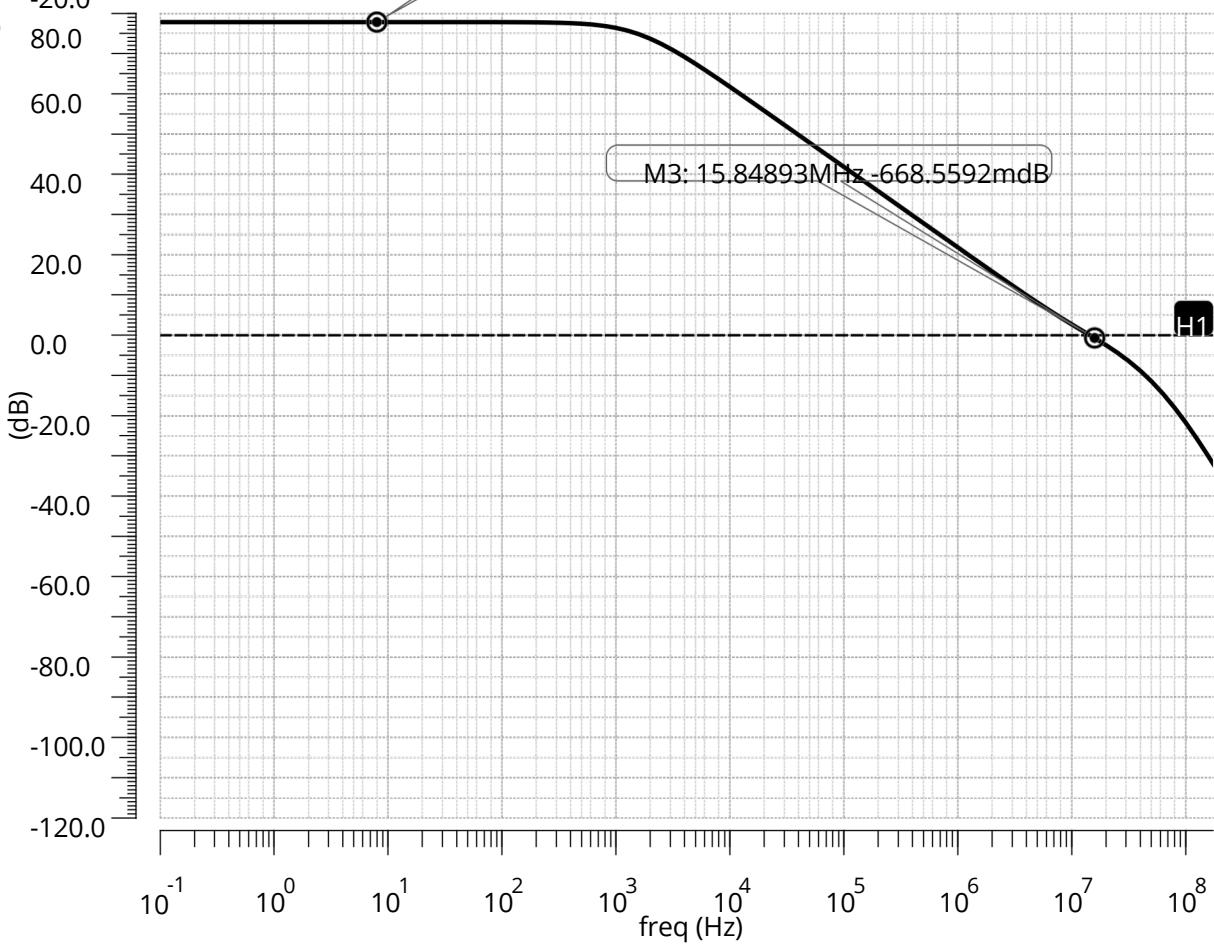
AC Gain vs Phase

Name

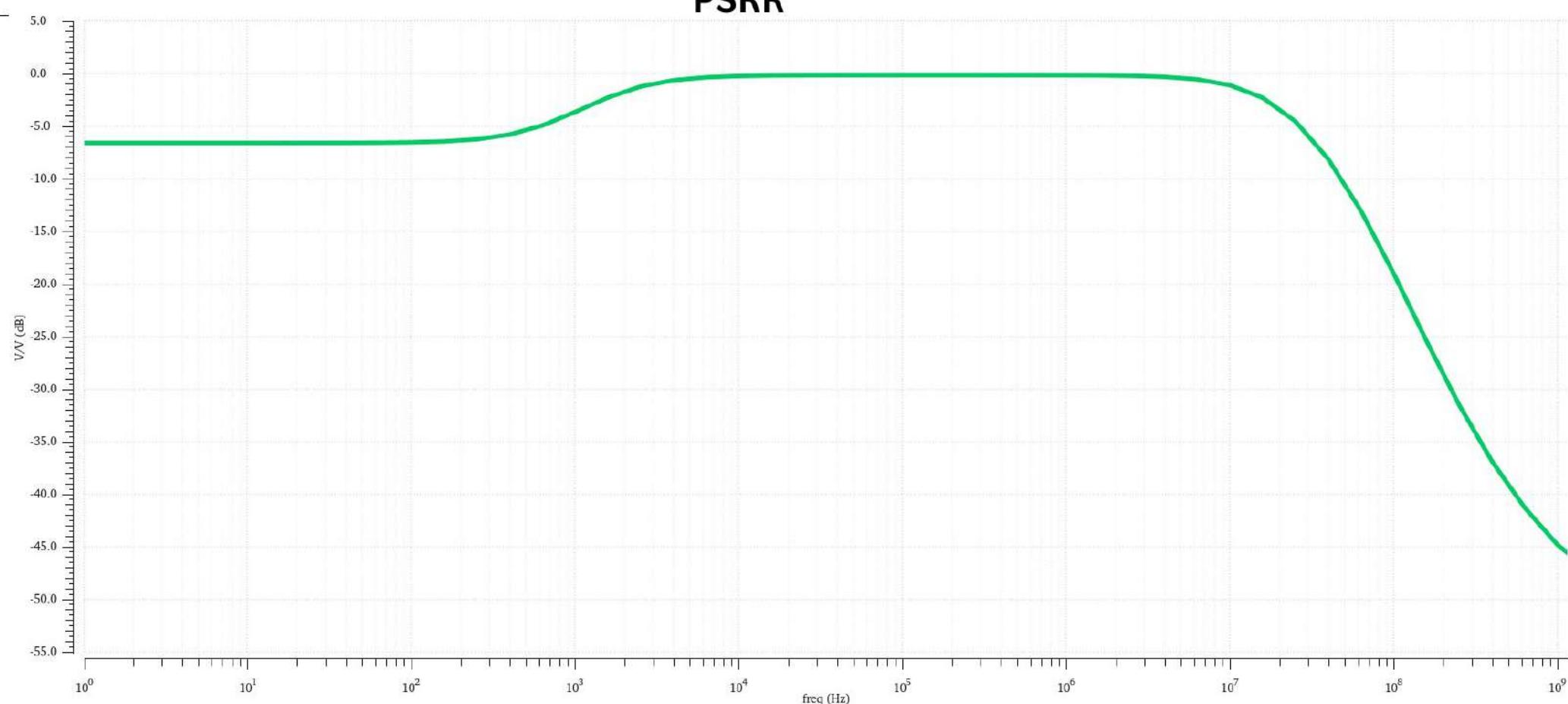
■ ...VF("/Vout")/VF("/net020")) 190.0



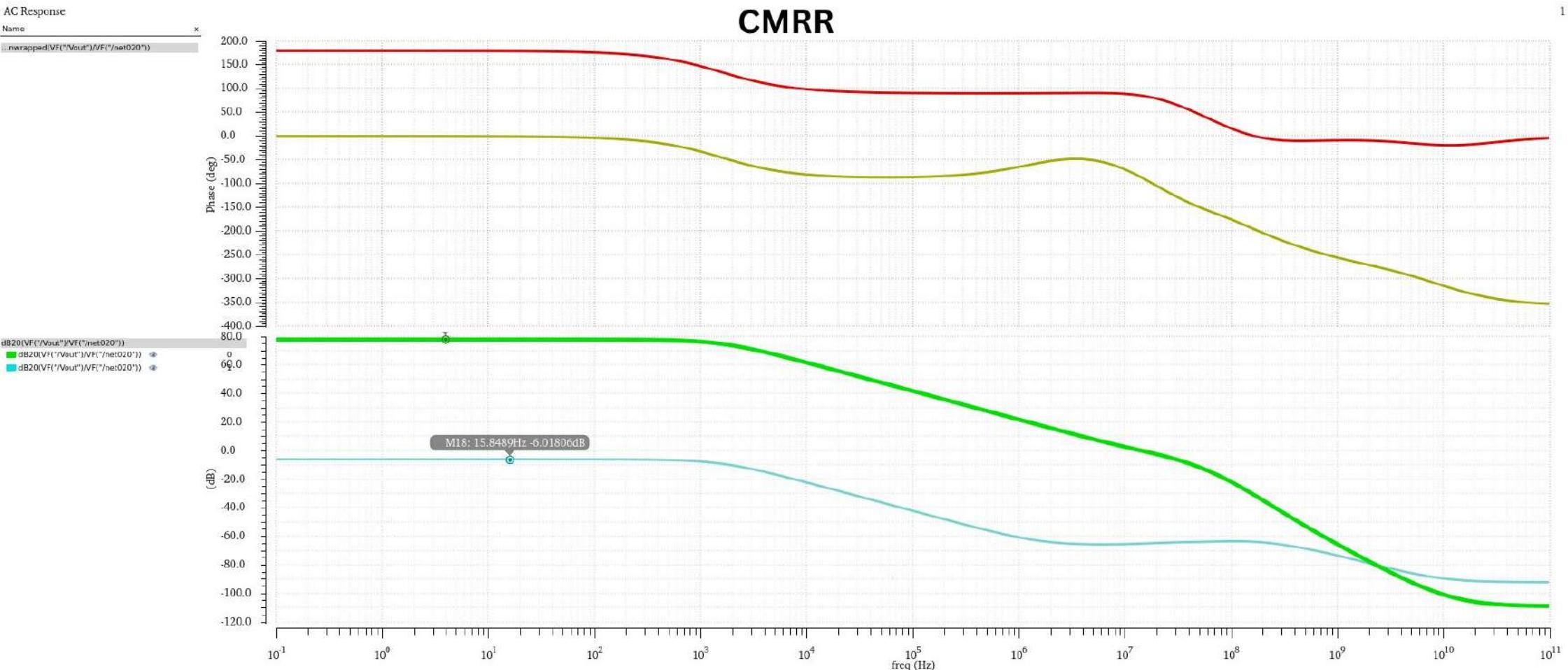
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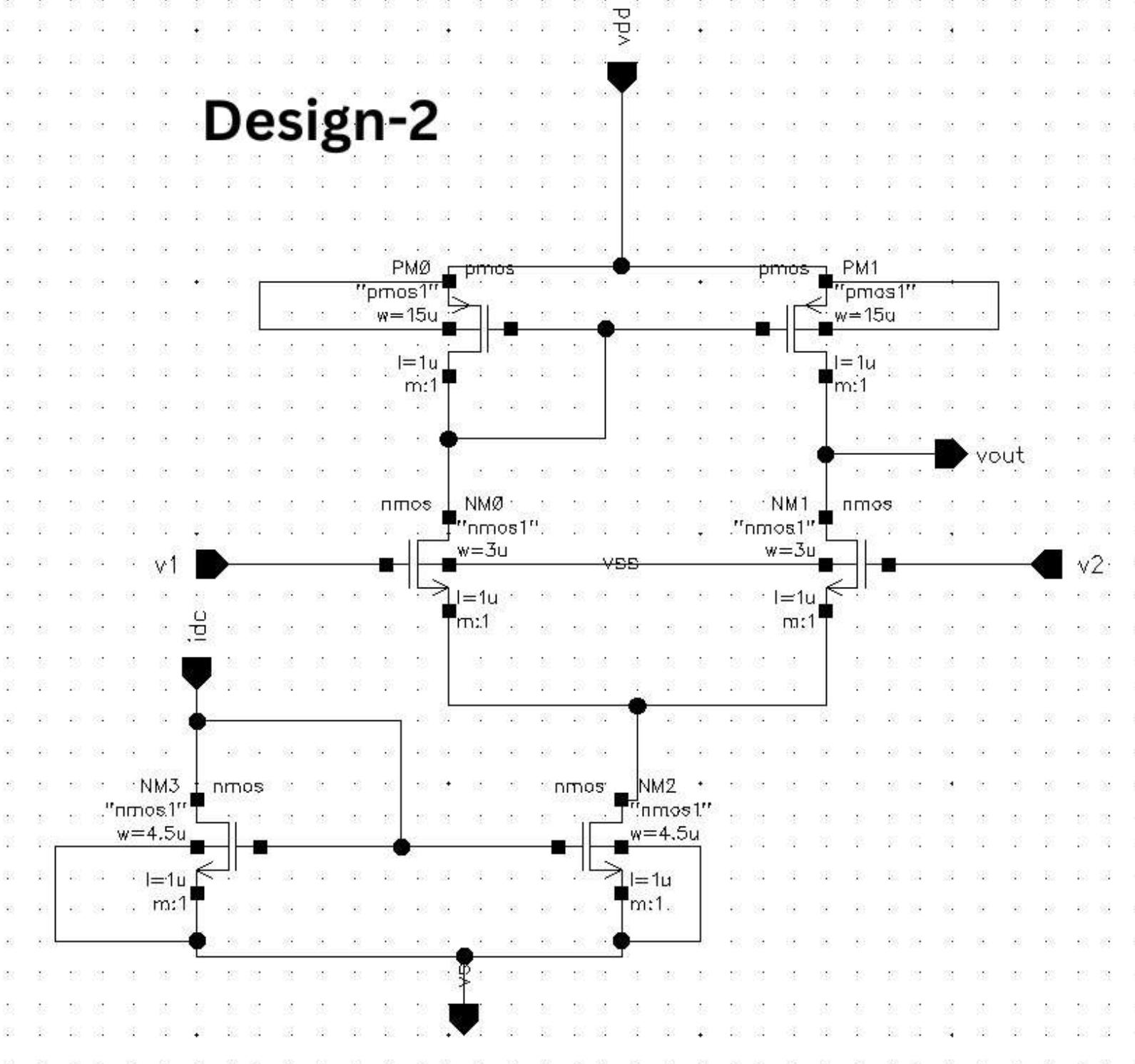
PSRR



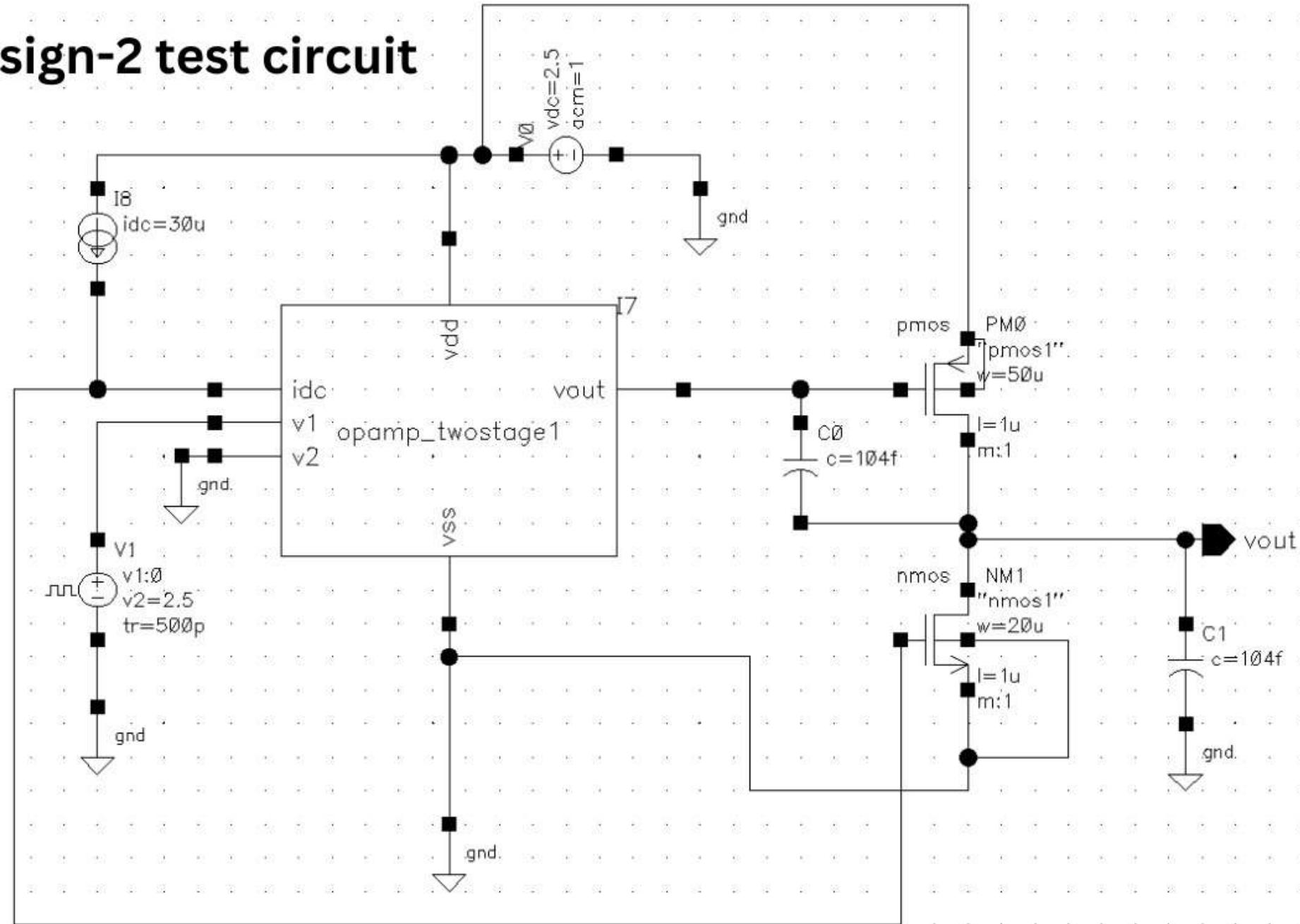
CMRR



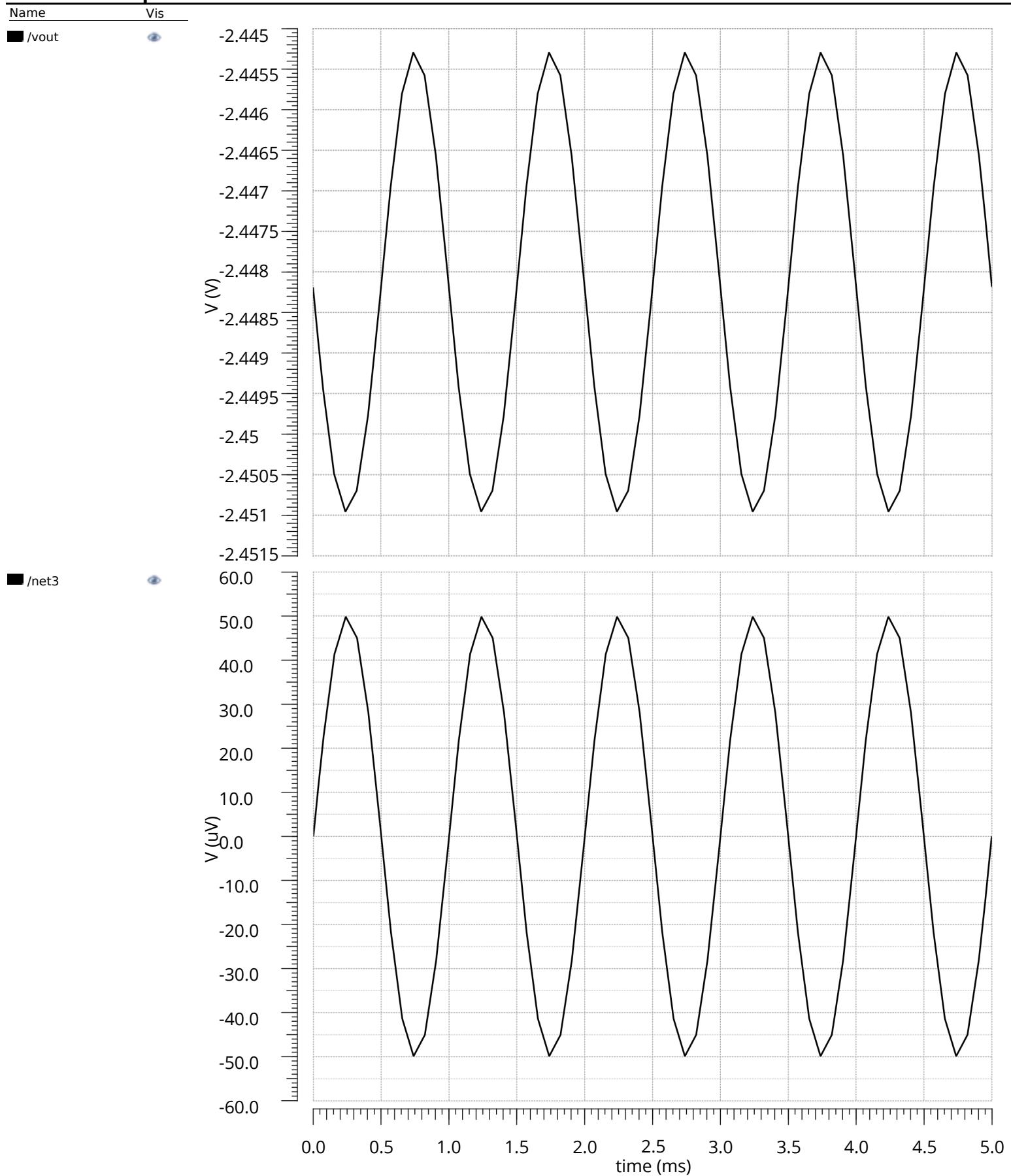
Design-2



Design-2 test circuit



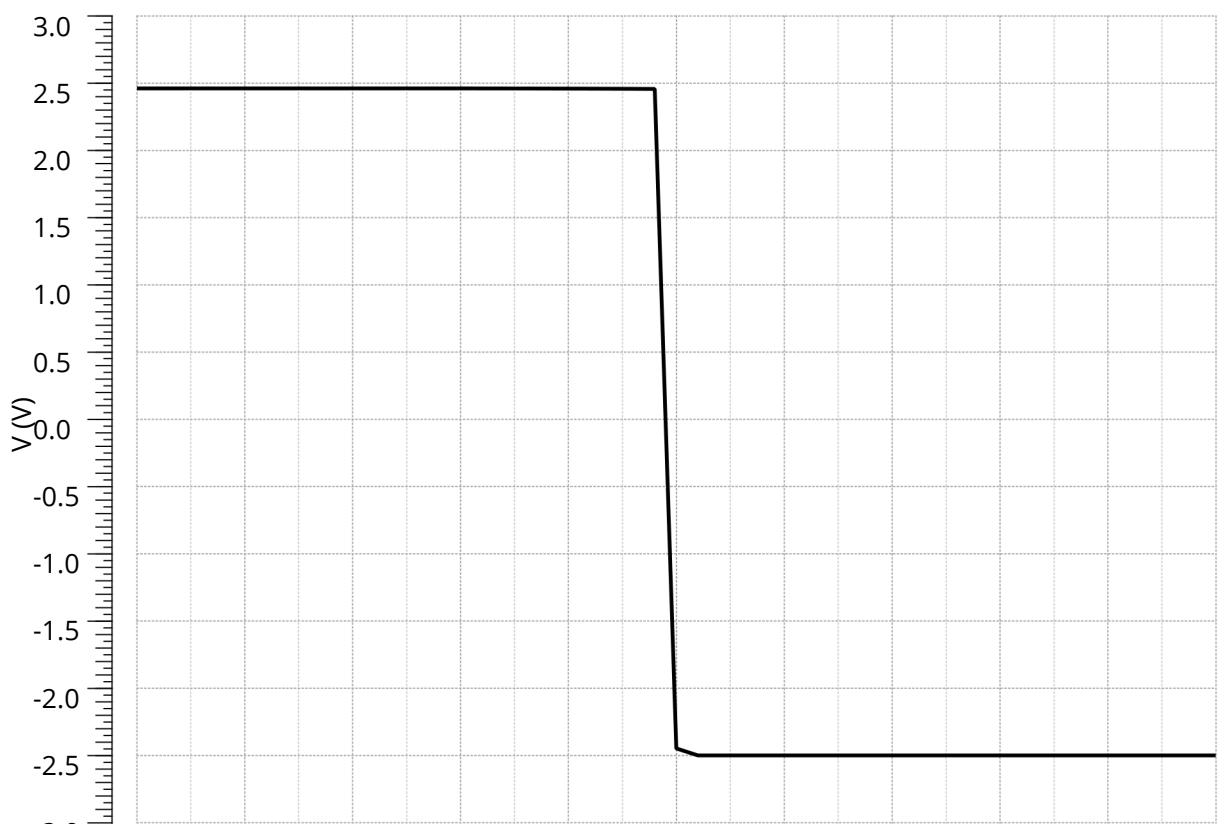
Transient Response



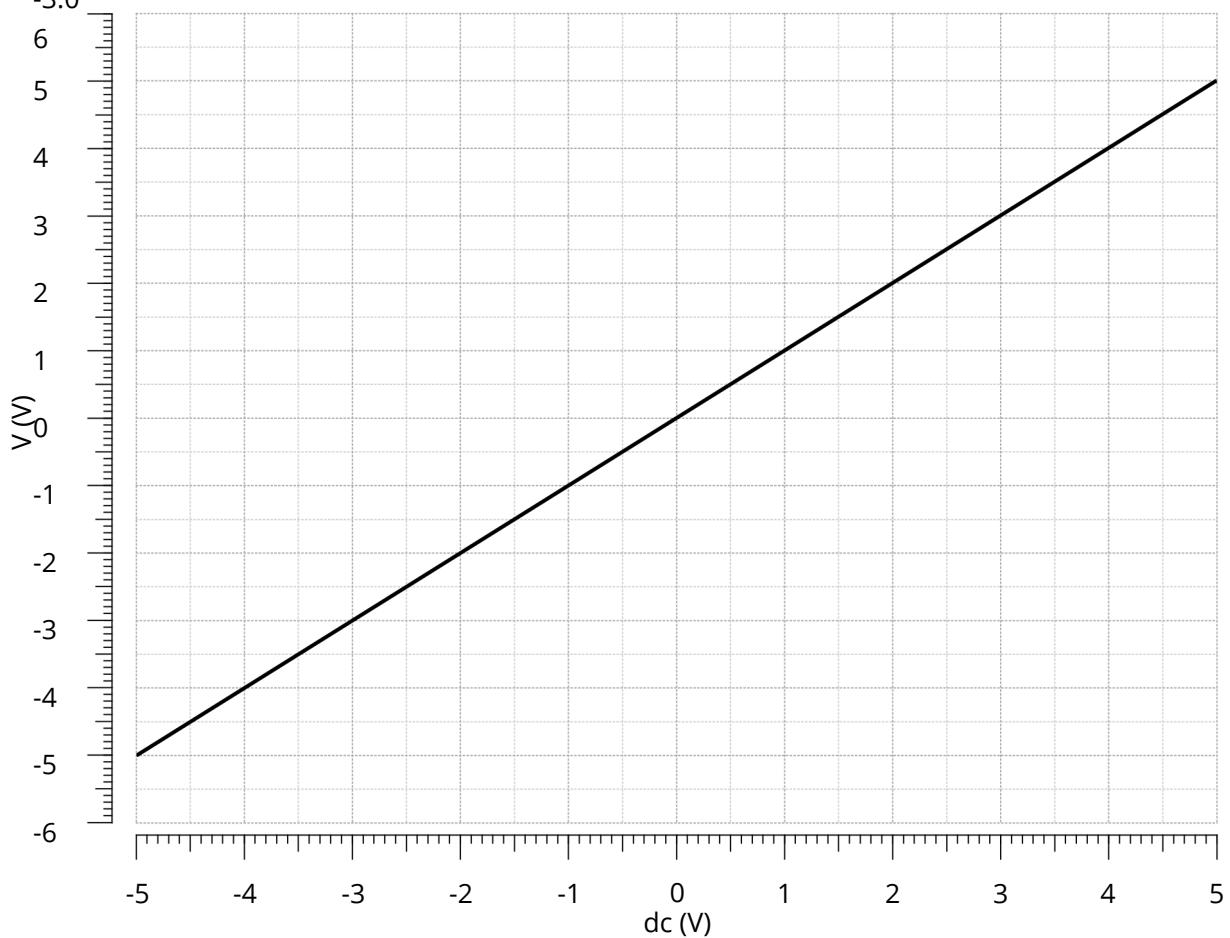
DC Response

Name Vis

■ /vout



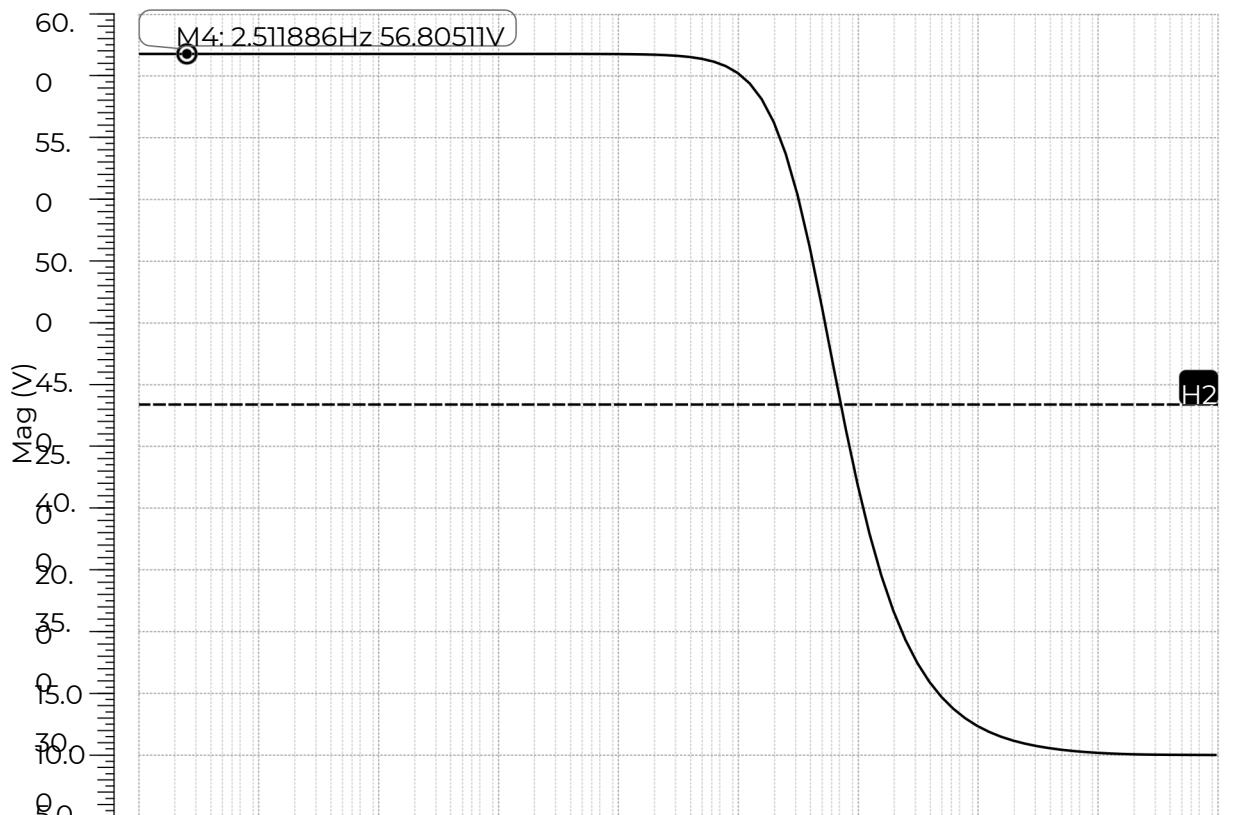
■ /net3



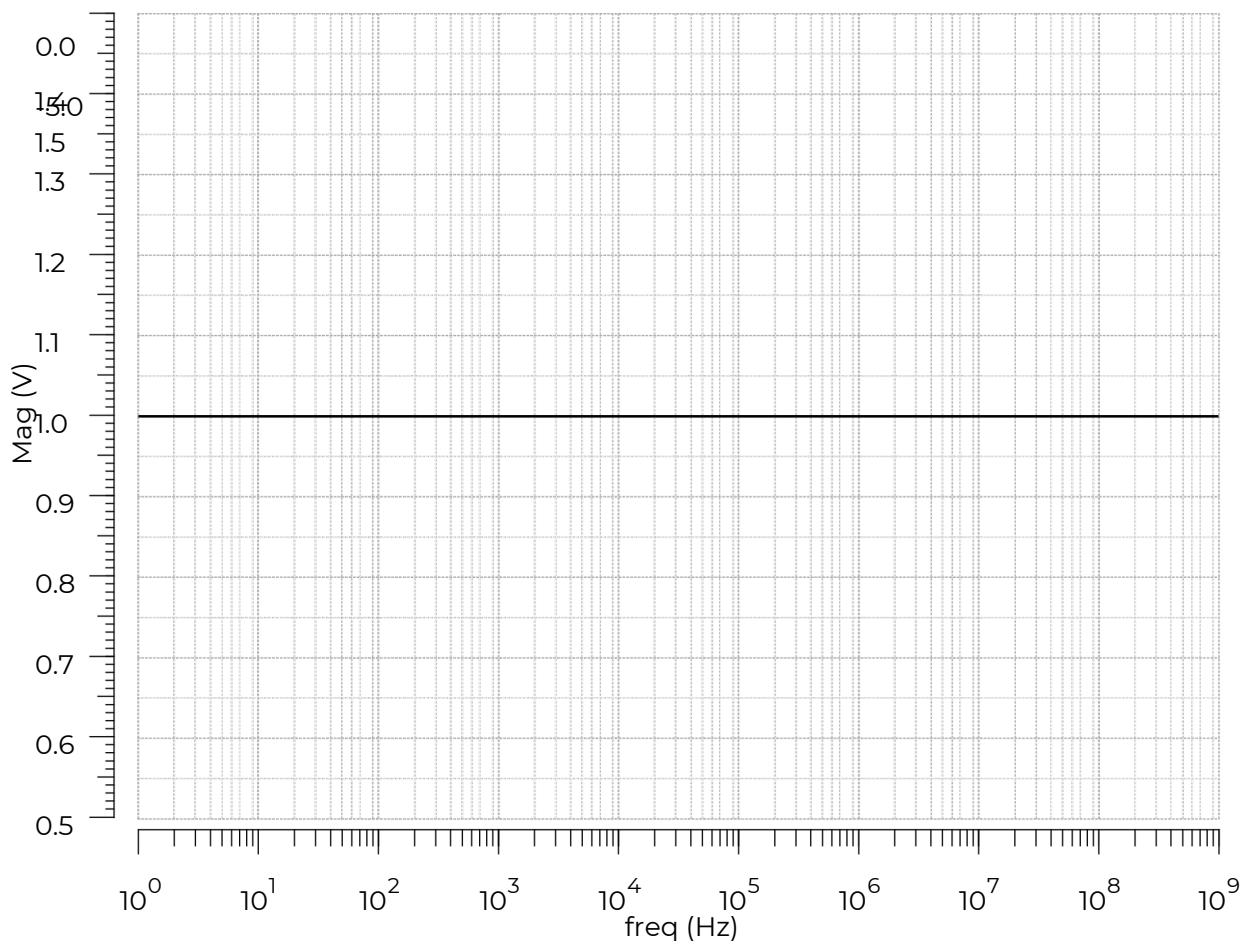
AC Response

Name Vis

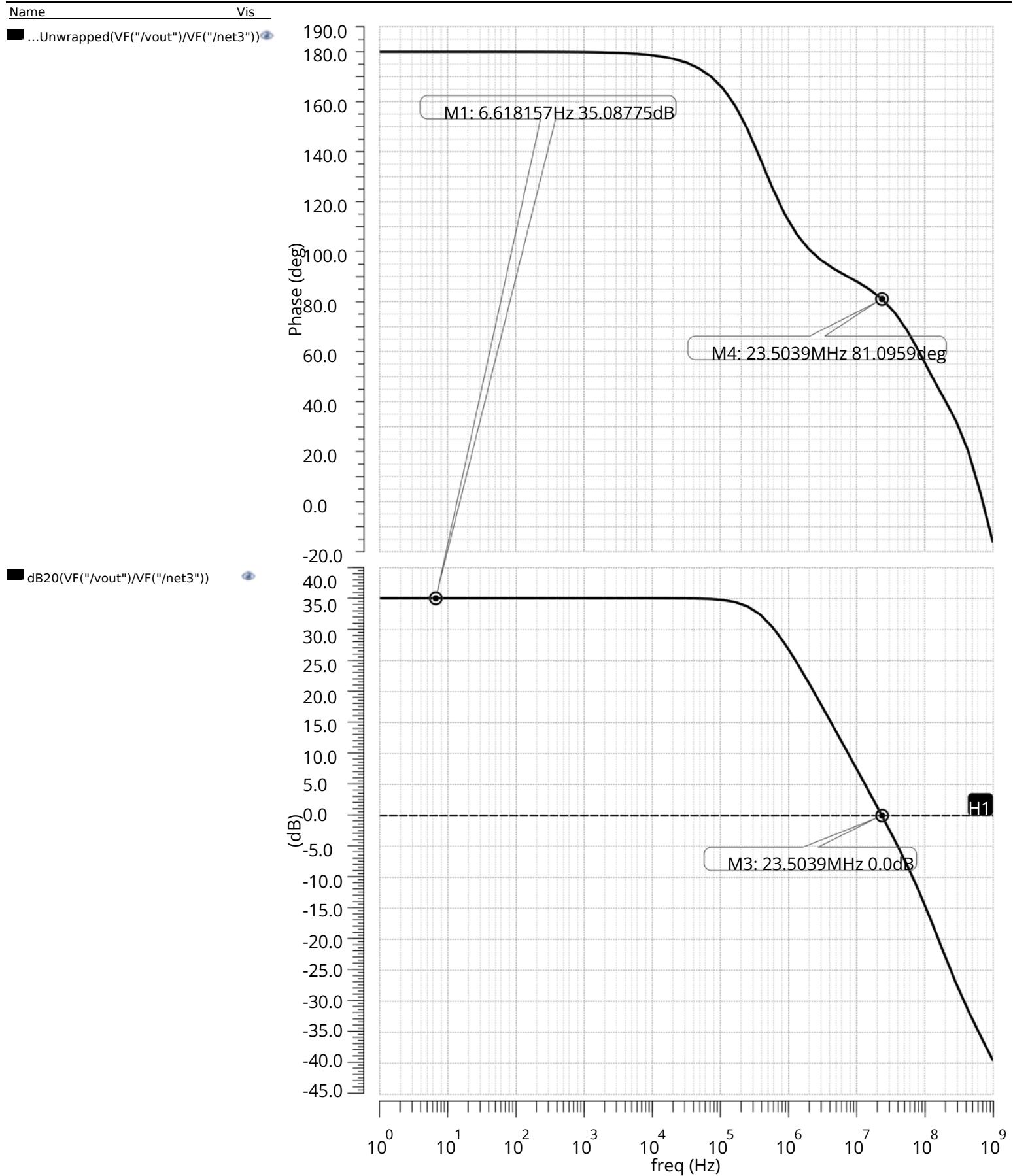
■ /vout



■ /net3



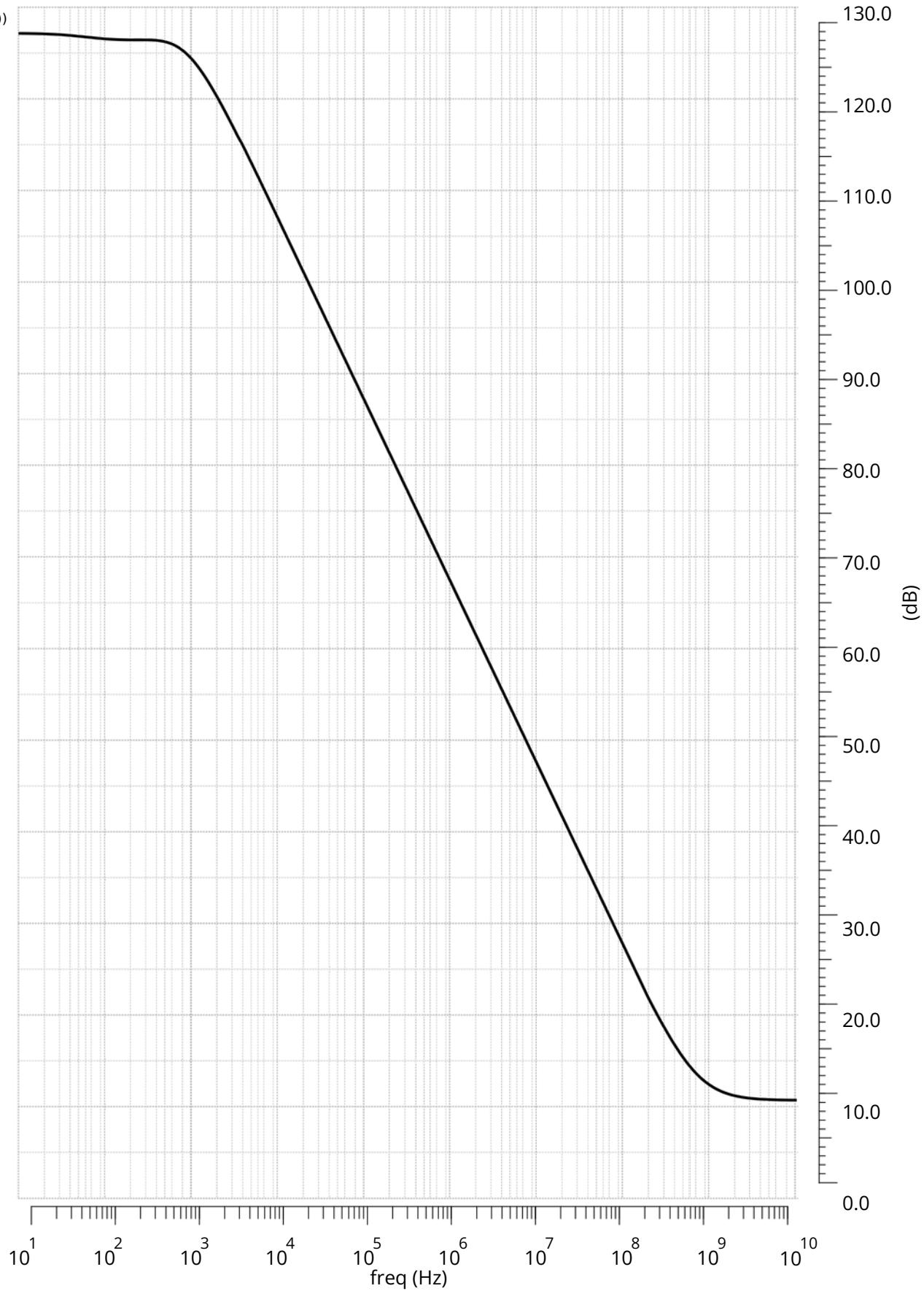
AC Phase vs Gain



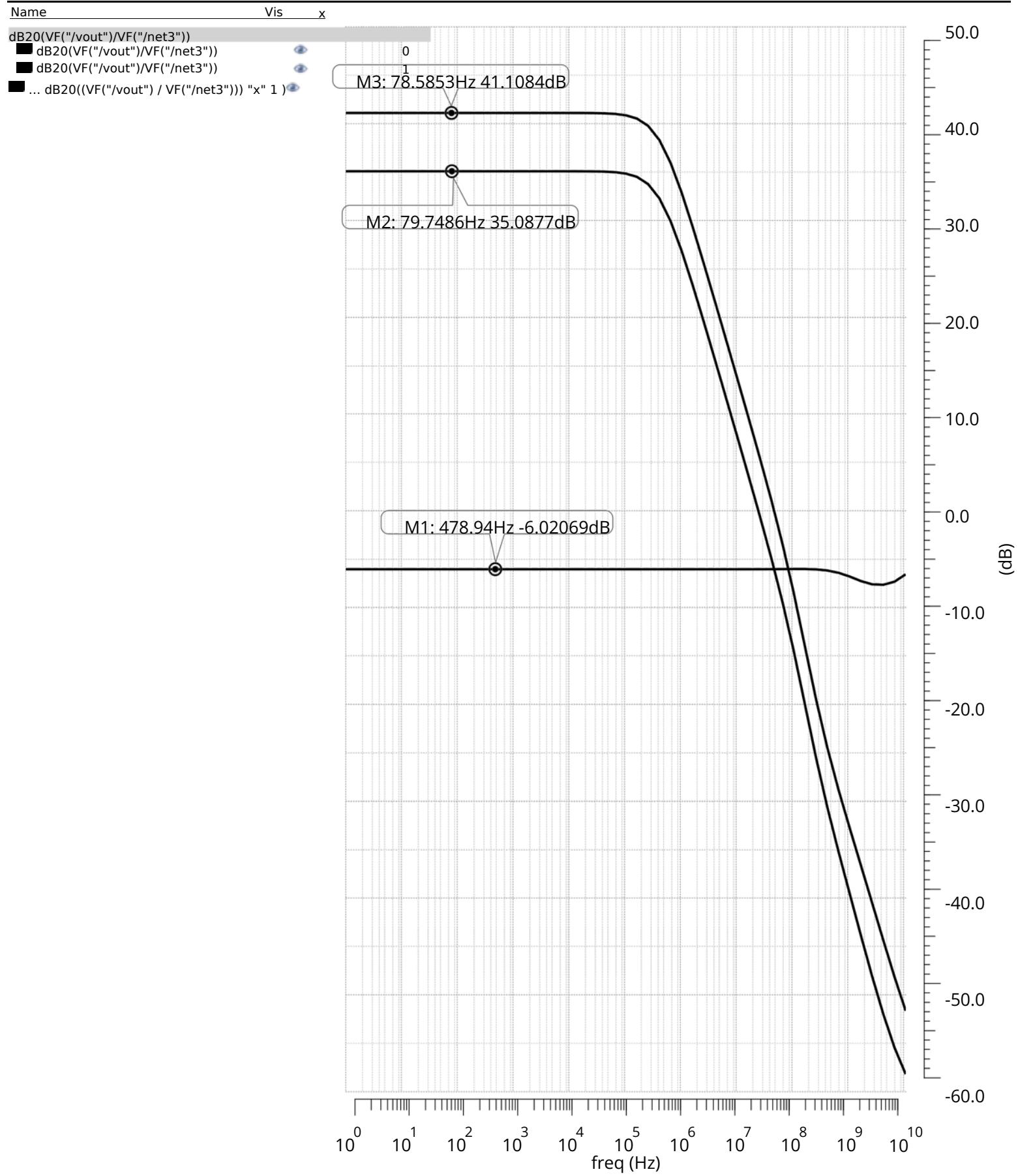
PSRR

Name _____

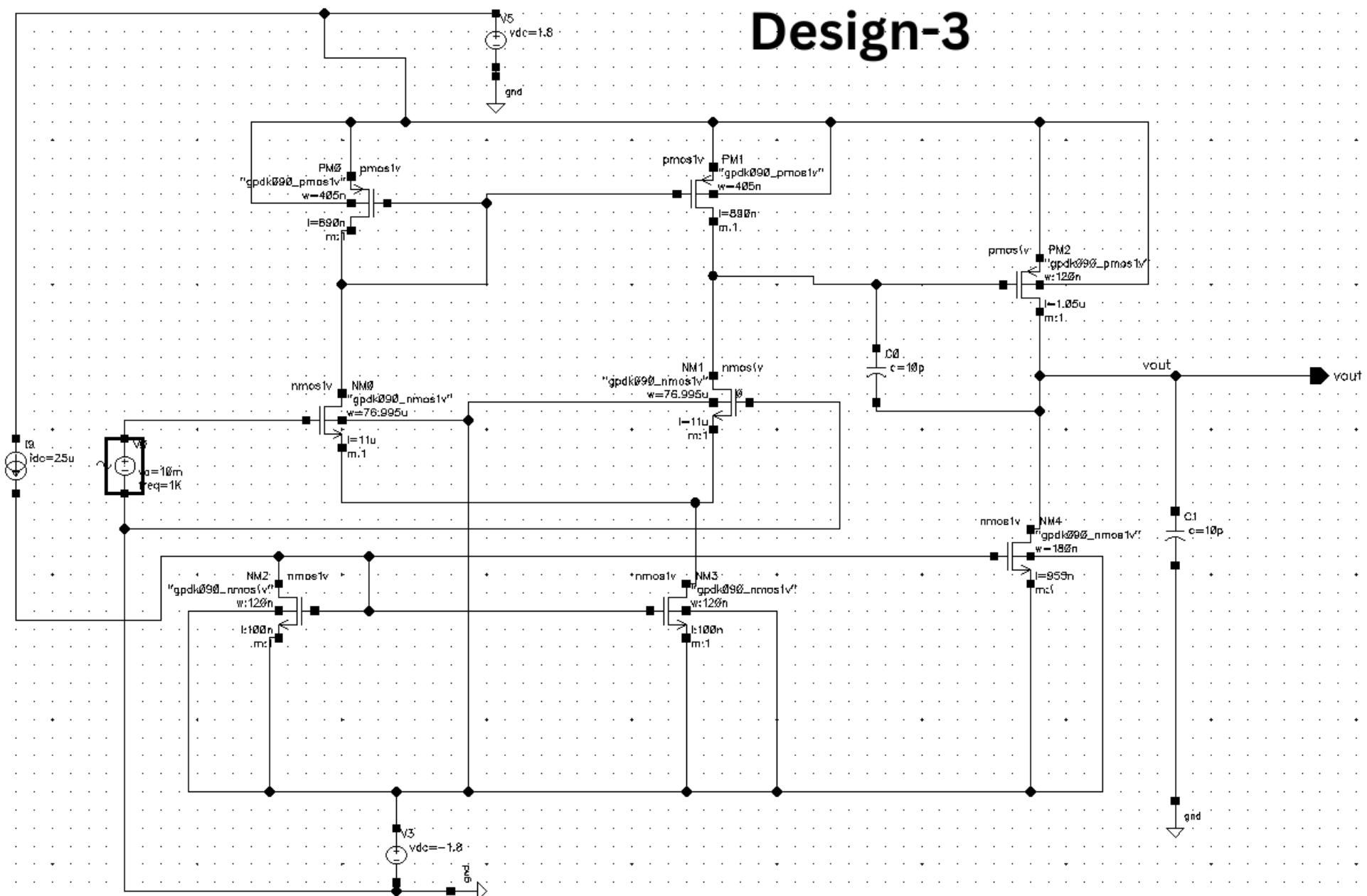
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CMRR



Design-3

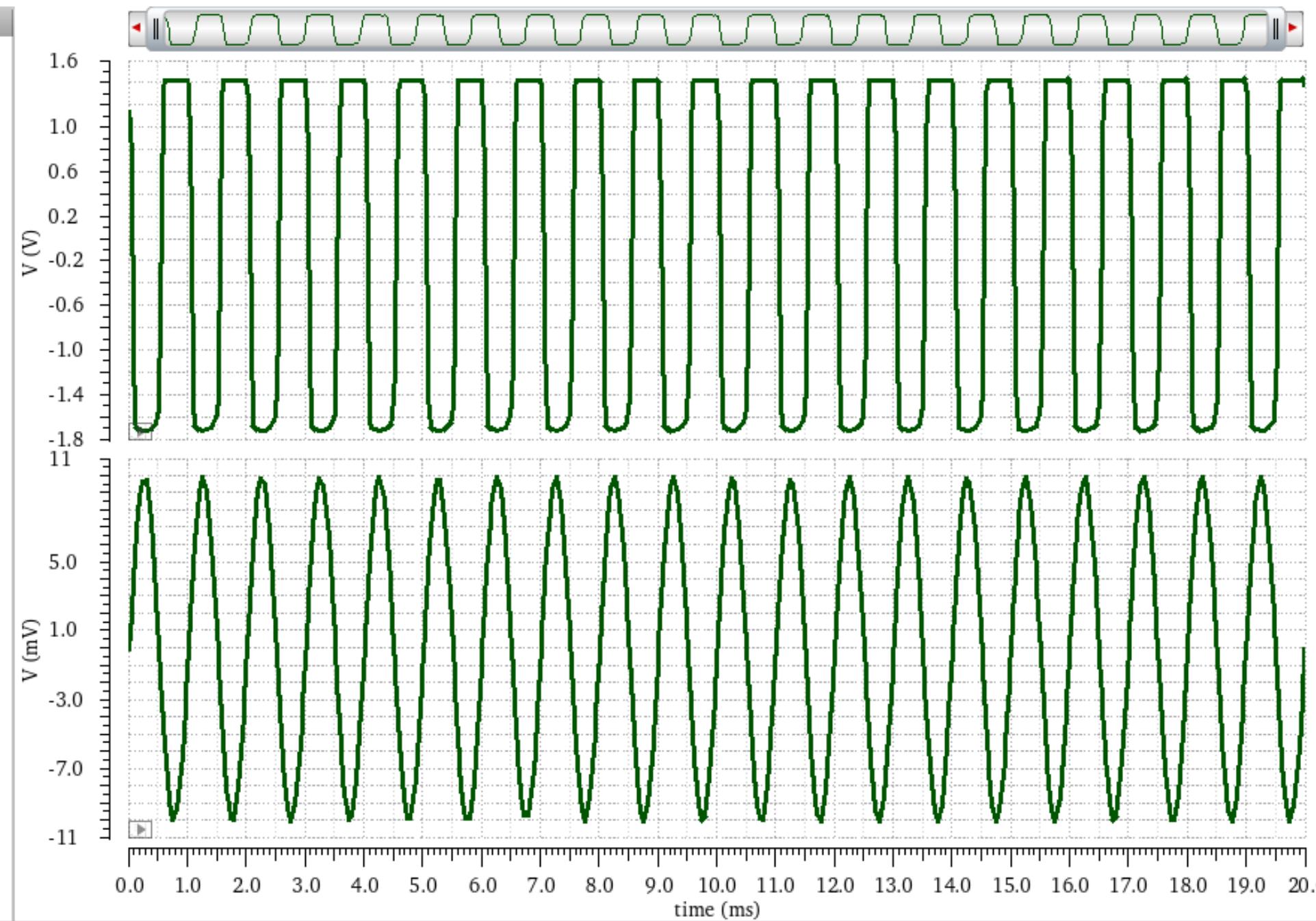


Transient Response

Thu Dec 12 14:40:58 2024 1

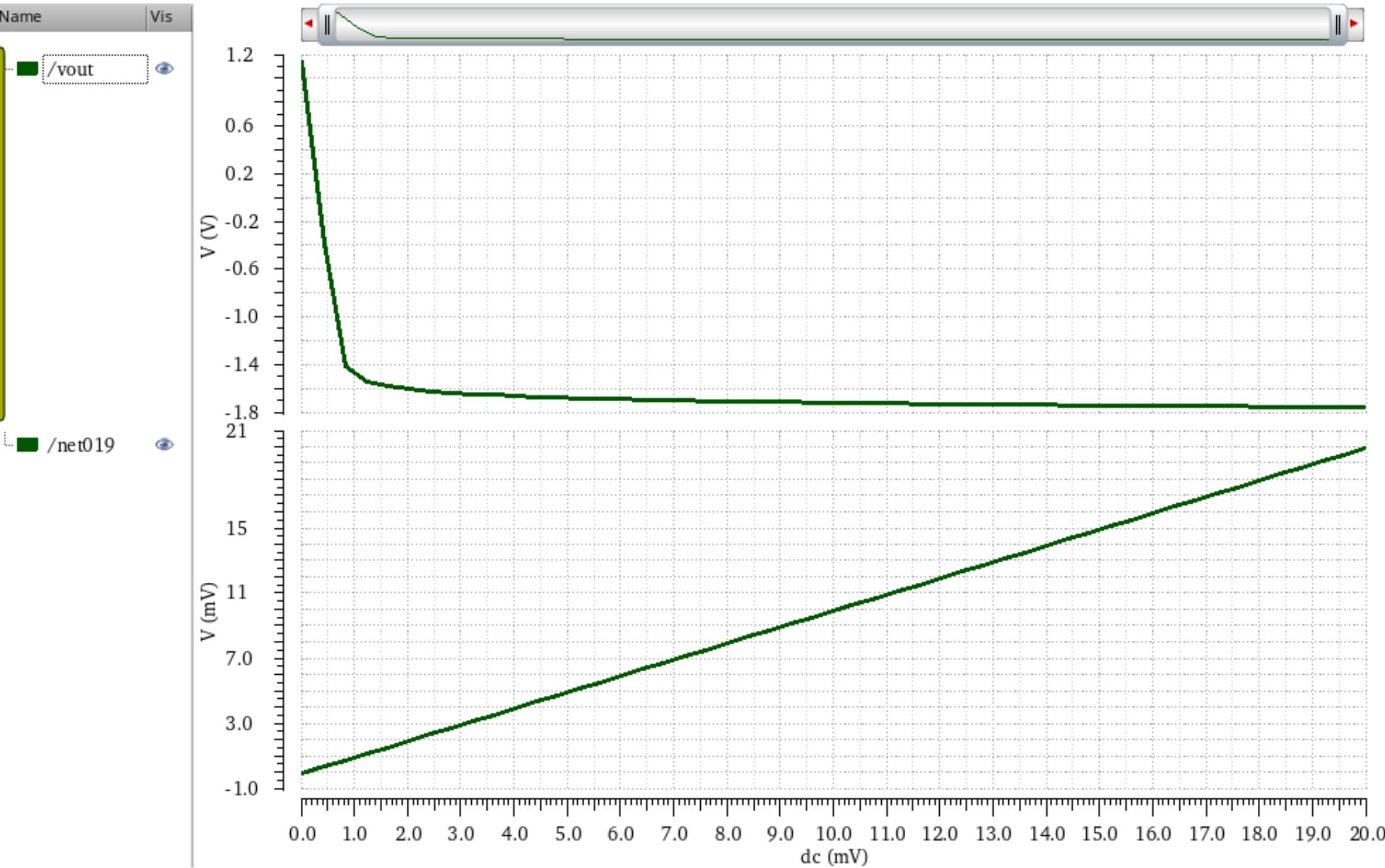
Name Vis

/vout



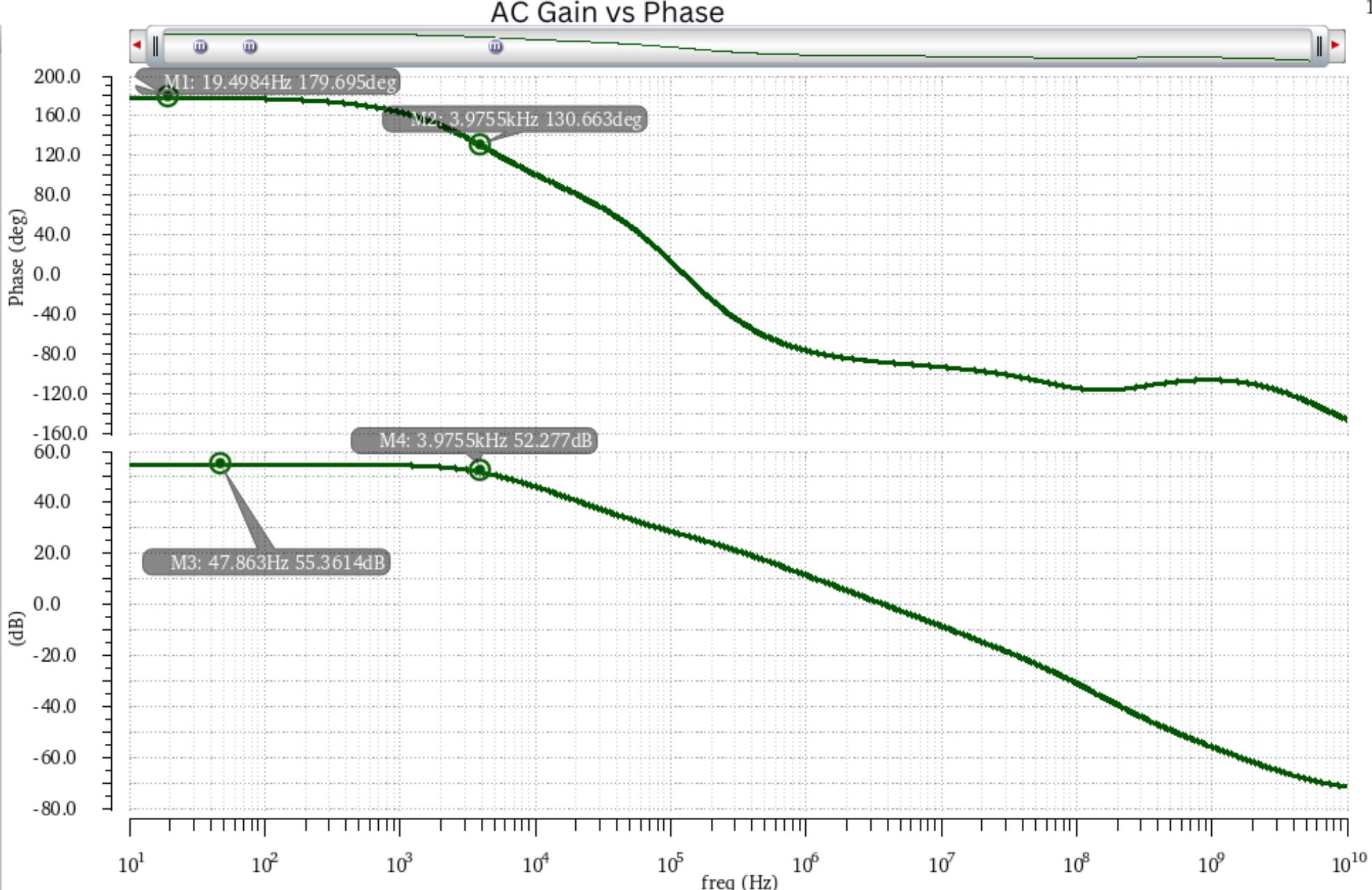
DC Response

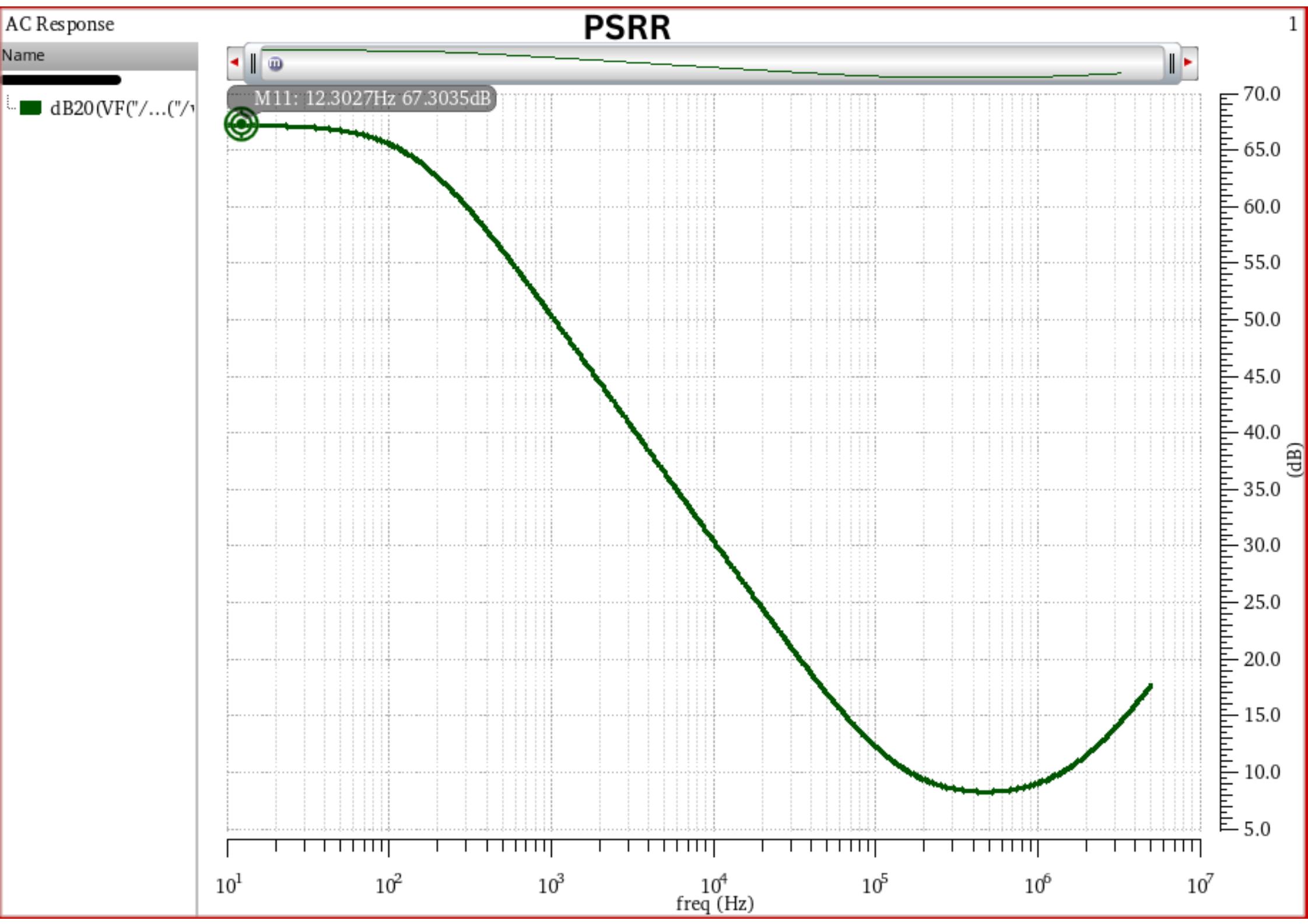
Thu Dec 12 12:17:53 2024



AC Response

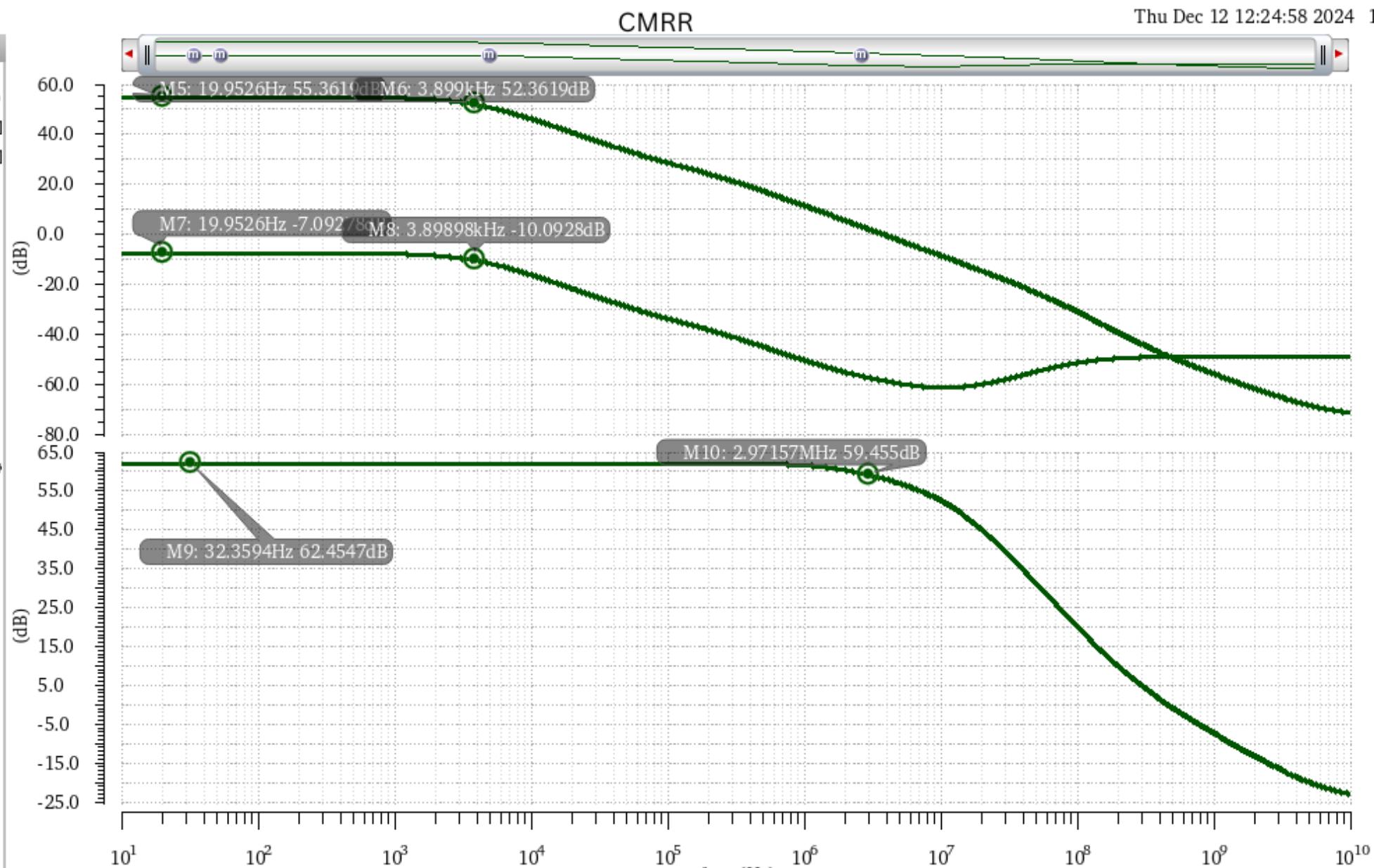
AC Gain vs Phase



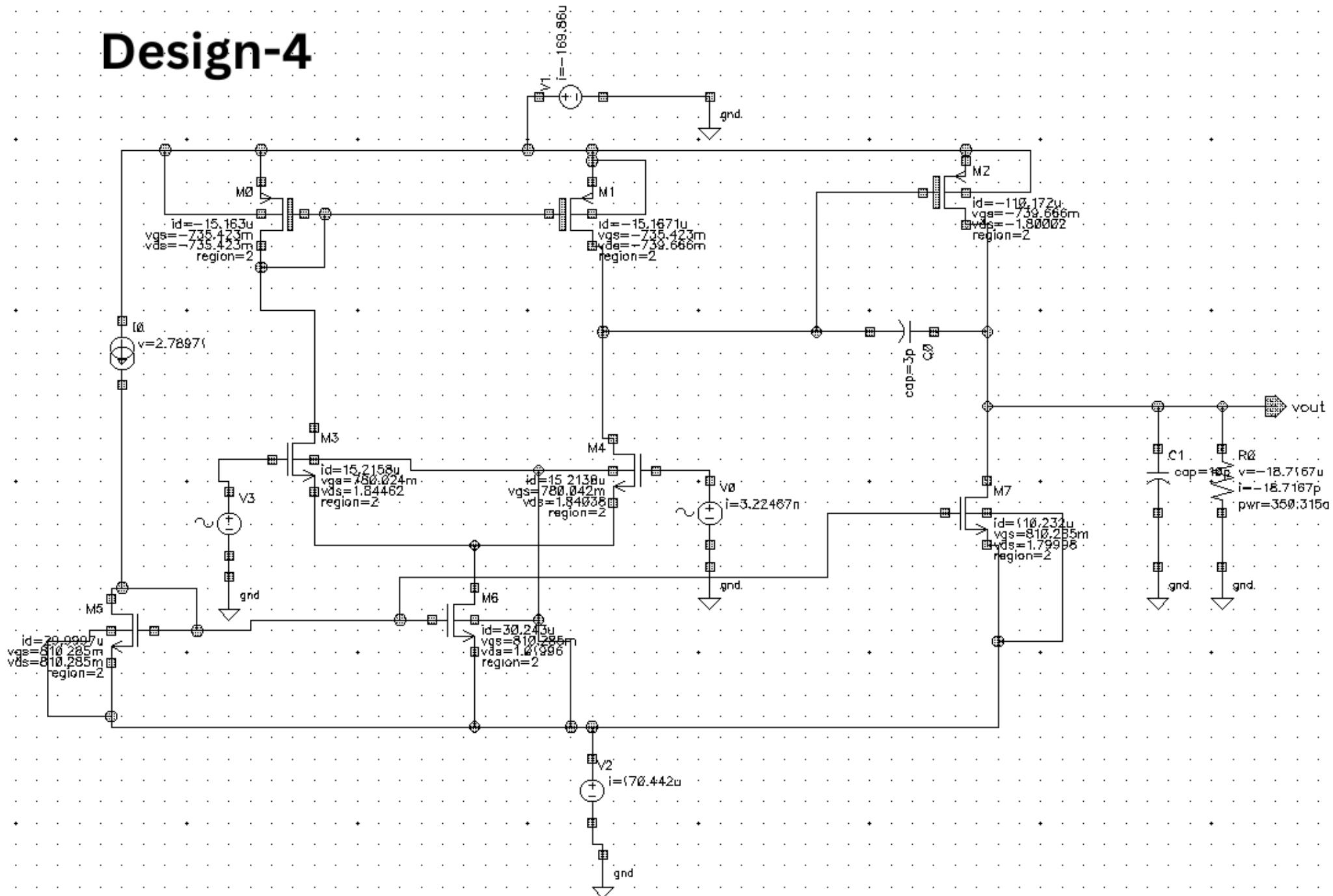


AC Response

Thu Dec 12 12:24:58 2024 1



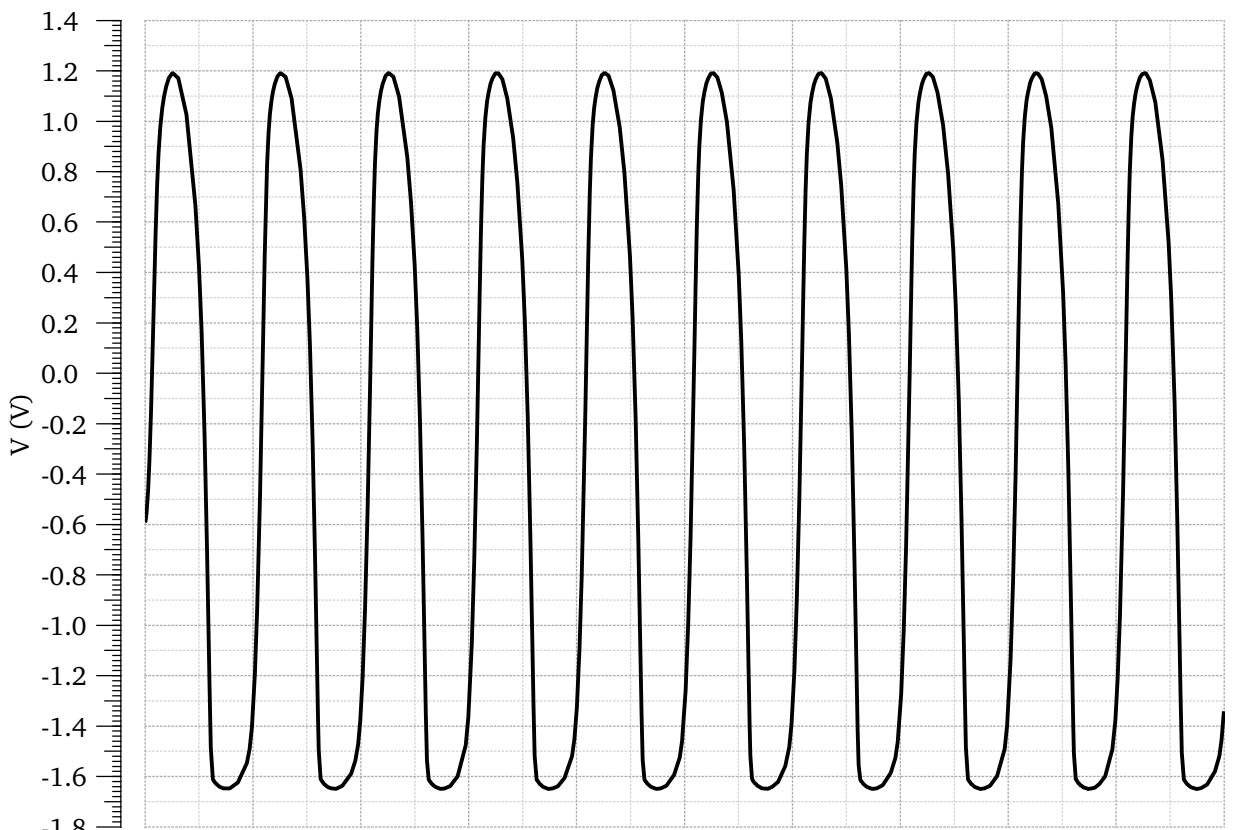
Design-4



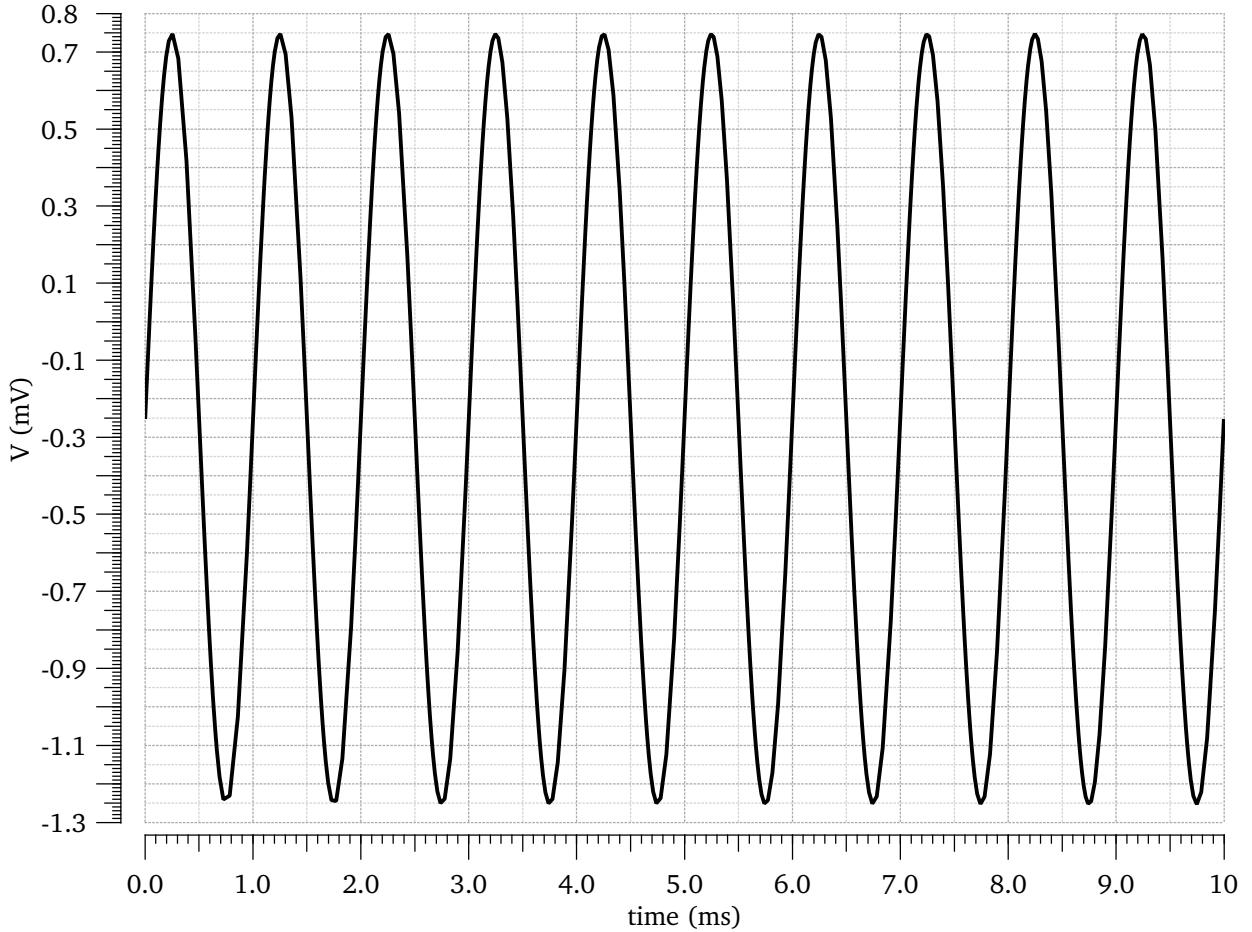
Transient Response

Name Vis

■ /vout



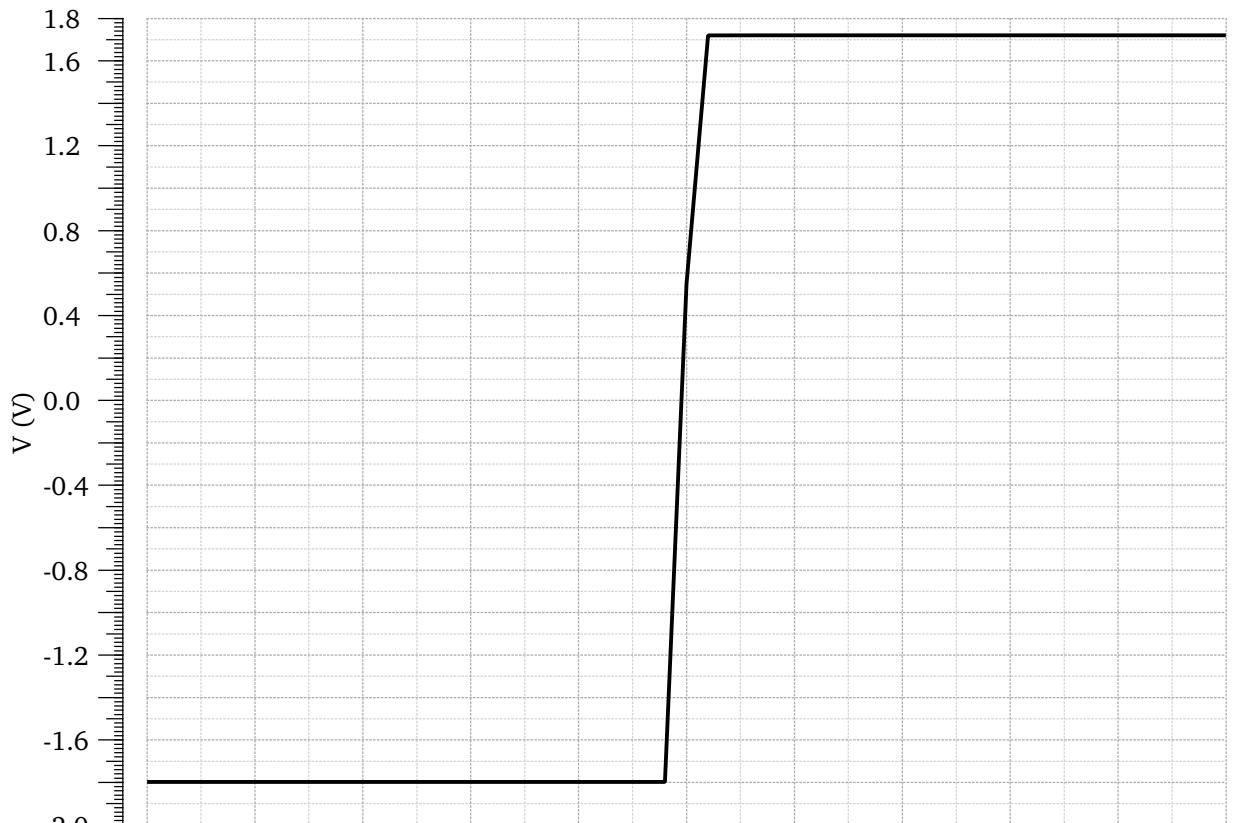
■ /net24



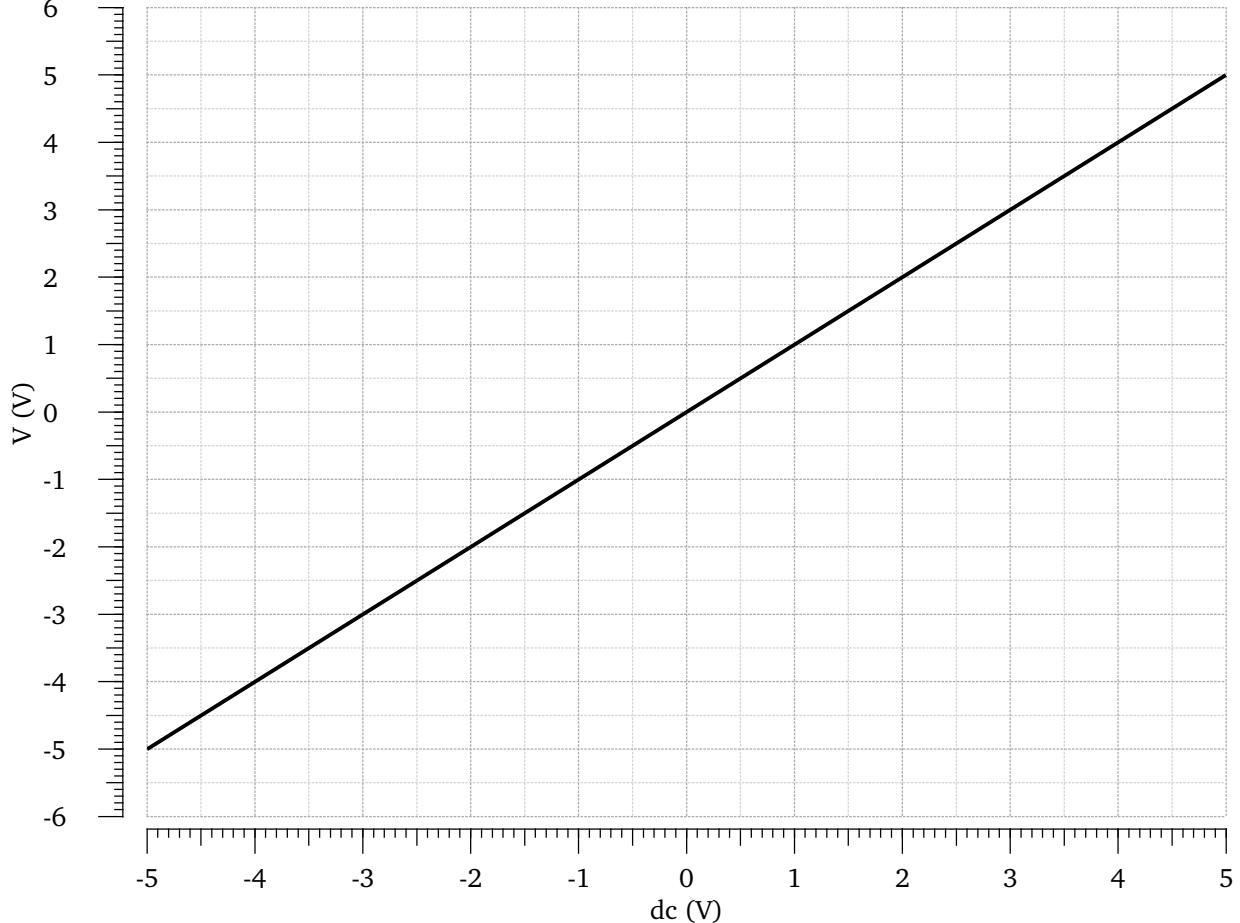
DC Response

Name Vis

■ /vout



■ /net24



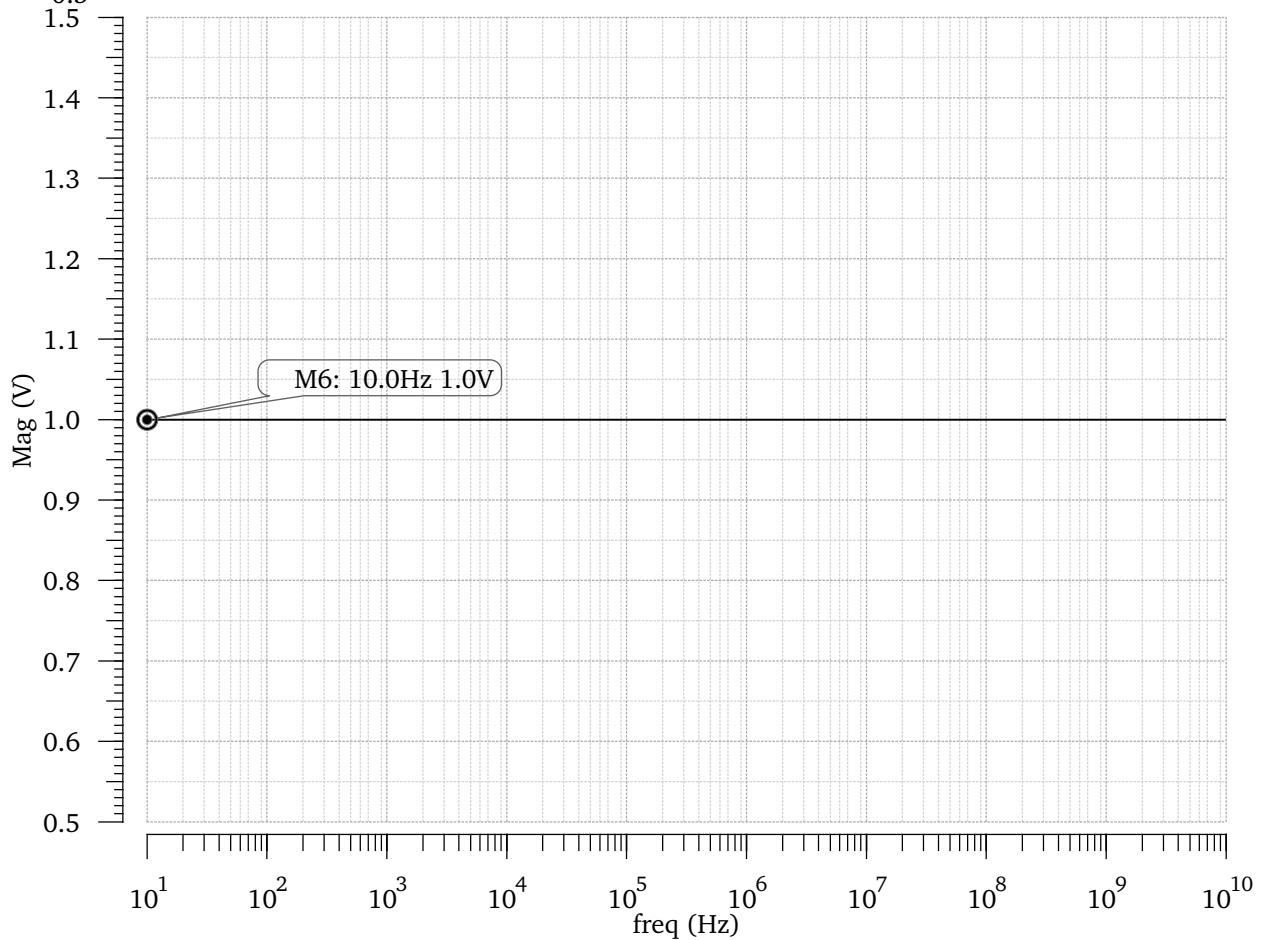
AC Response

Name Vis

■ /vout



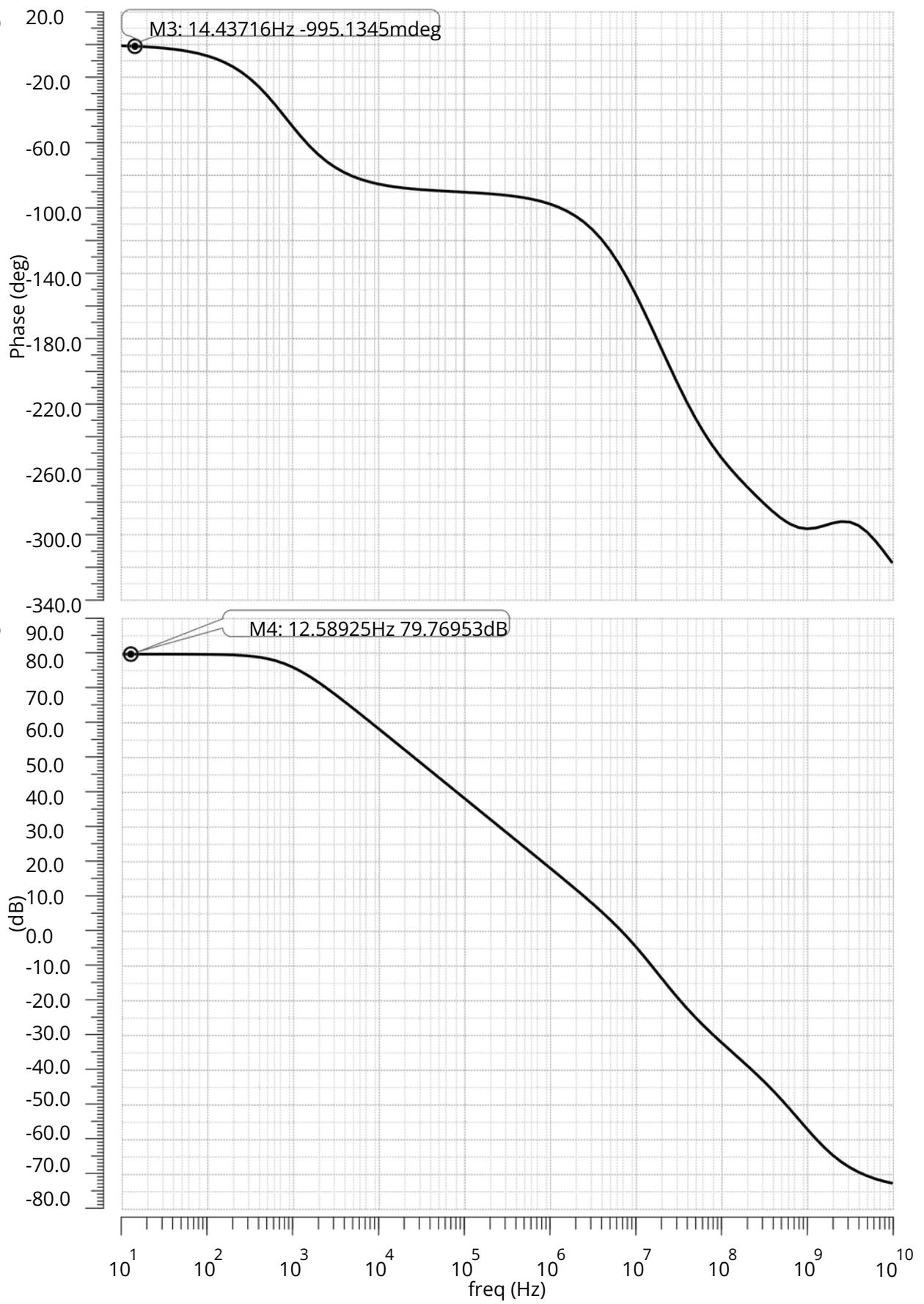
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AC Gain and Phase

Name _____

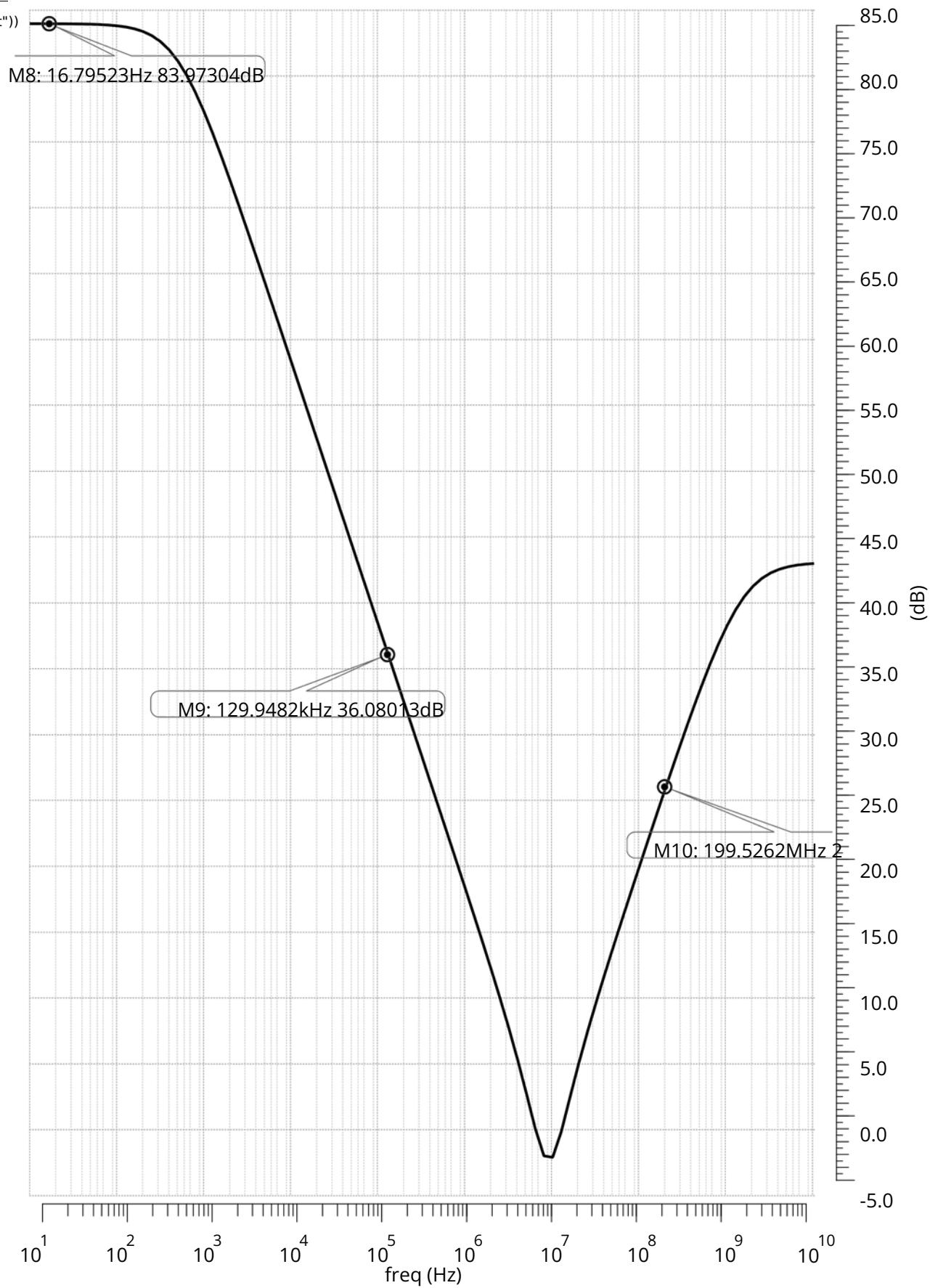
■ ...($\text{VF}("vout")/\text{VF}("net24")$)



PSRR

Name _____

■ ...0(VF("/net5")/VF("/vout"))



CMRR

Name Vis V2x

dB20(VF("/vout")/VF("/net24"))

■ dB20(VF("/vout")/VF("/net24"))

■ dB20(VF("/vout")/VF("/net24"))

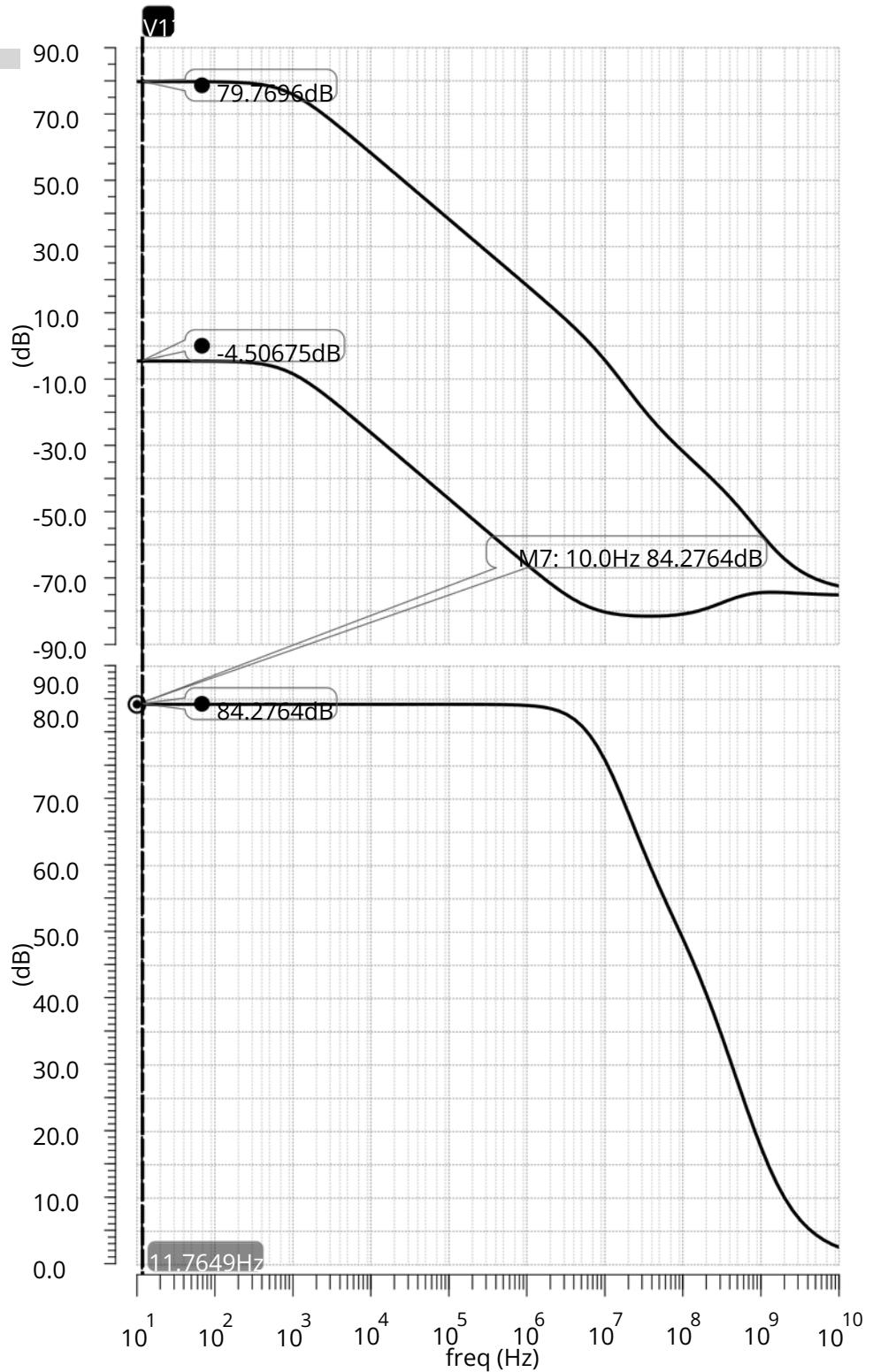
...dB0

...dB0

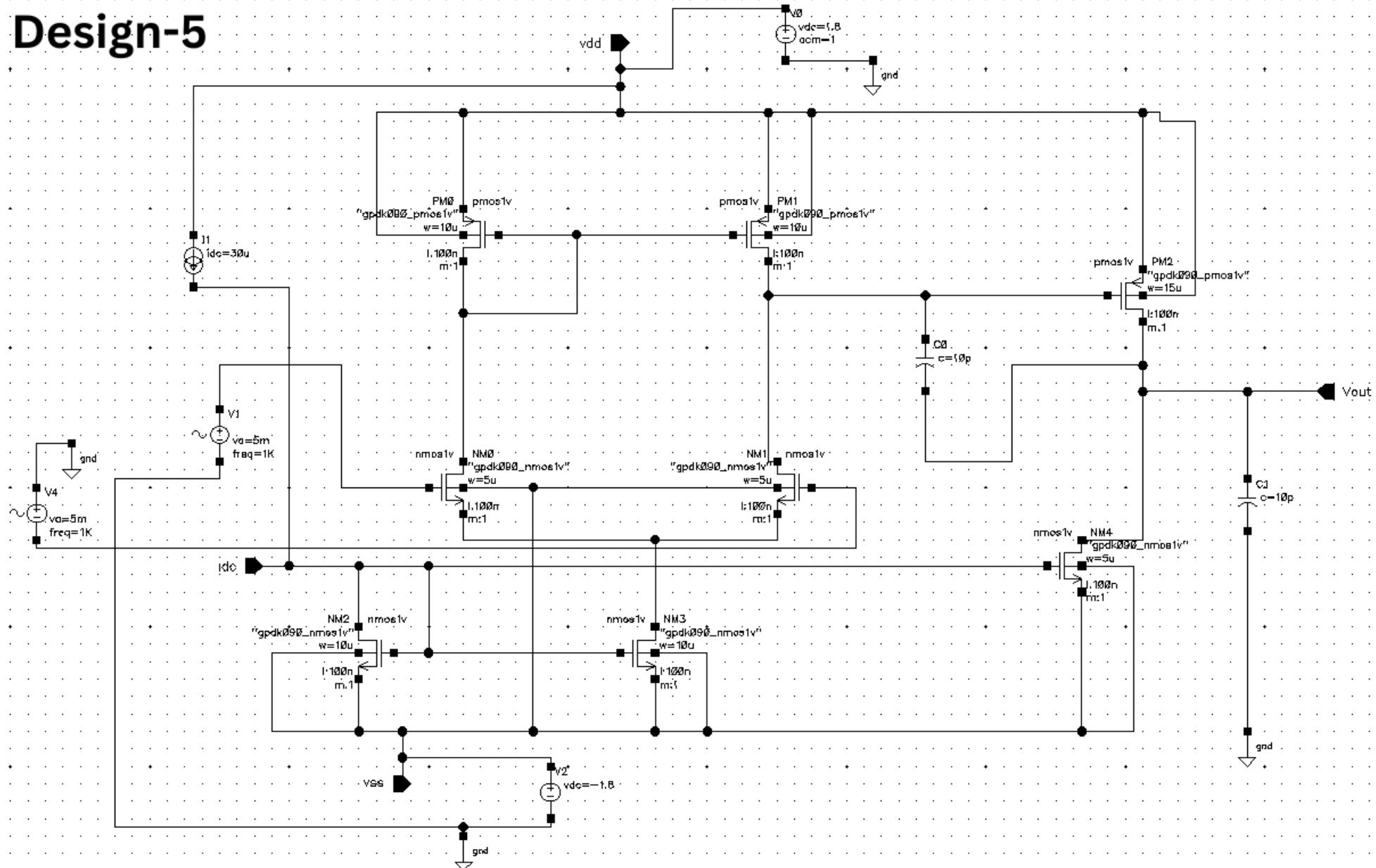
...dB1

■ ...dB20((VF("/vout") / VF("/net24"))) "x" 1)

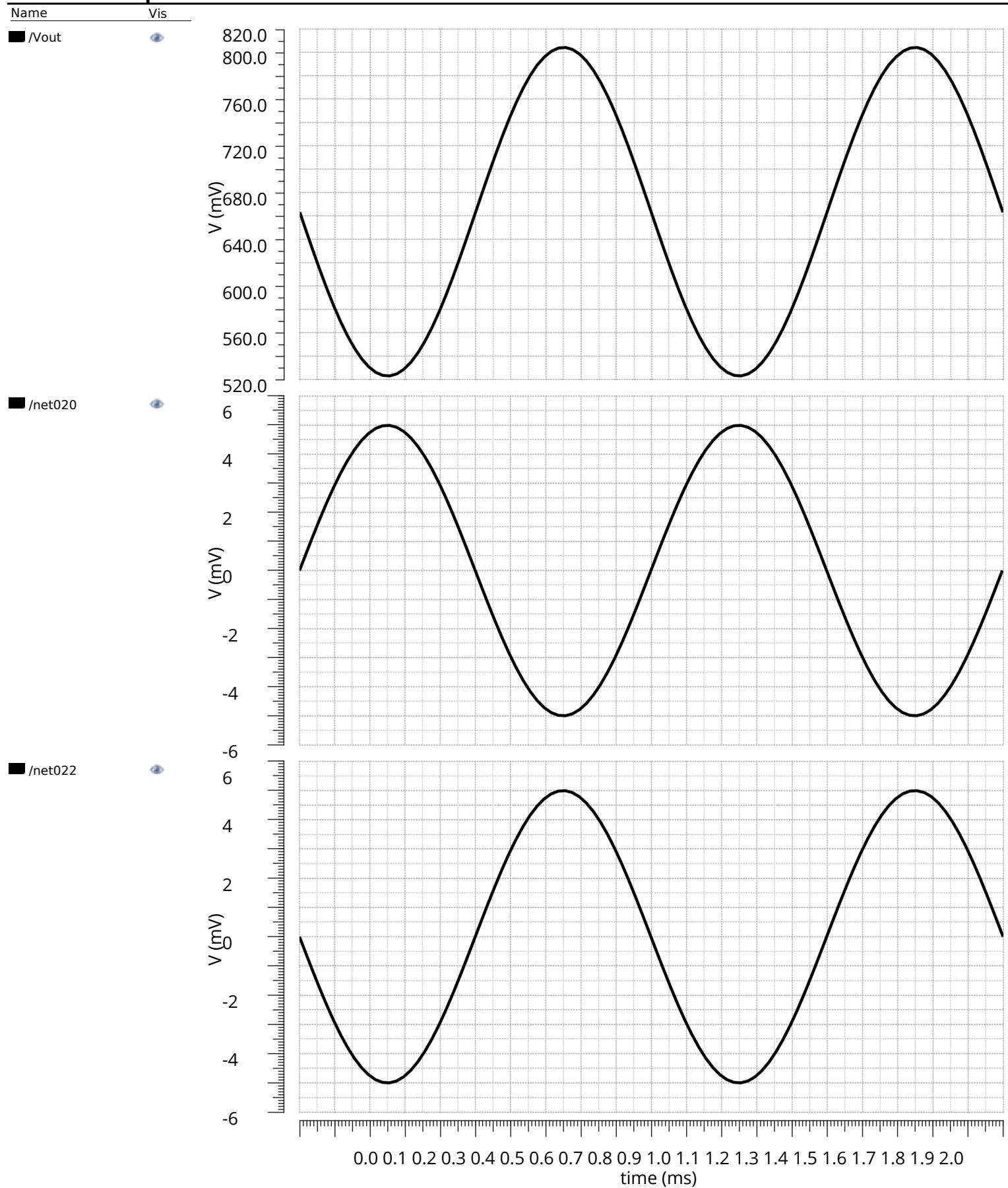
...dB



Design-5



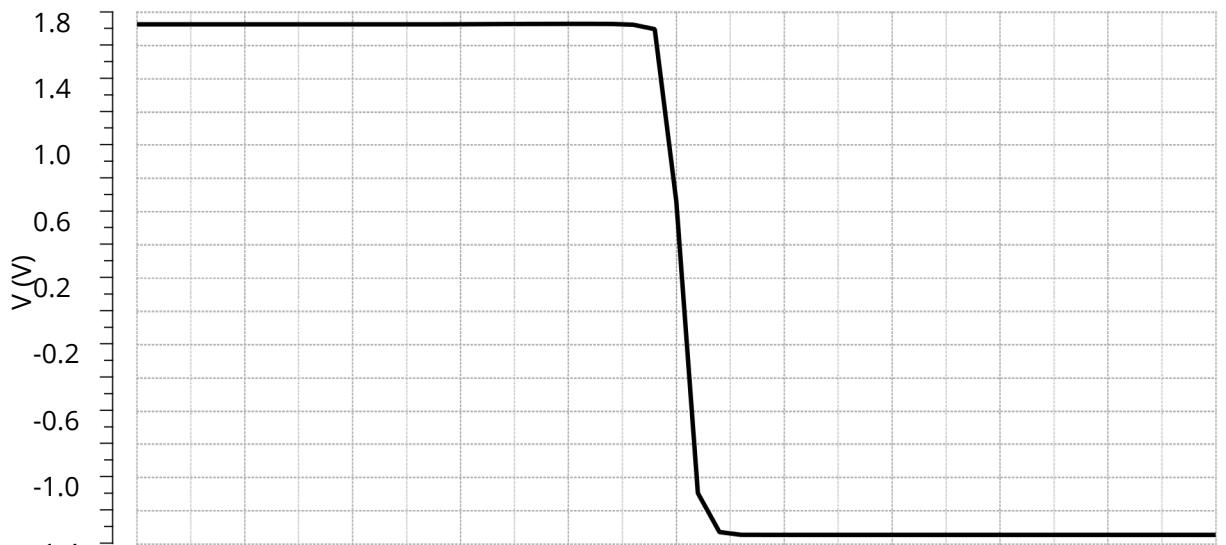
Transient Response



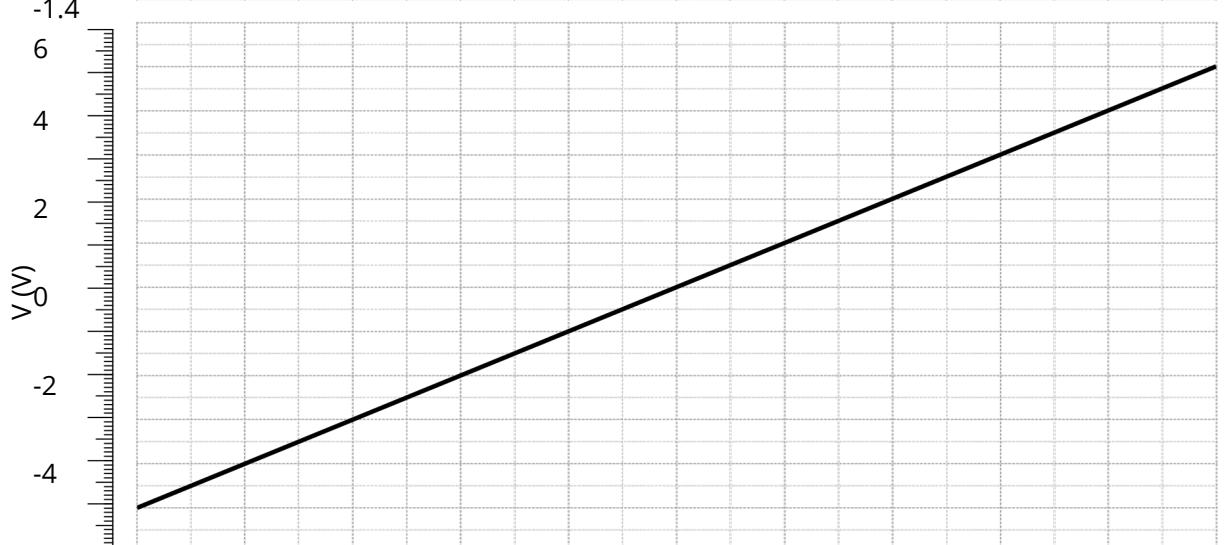
DC Response

Name Vis

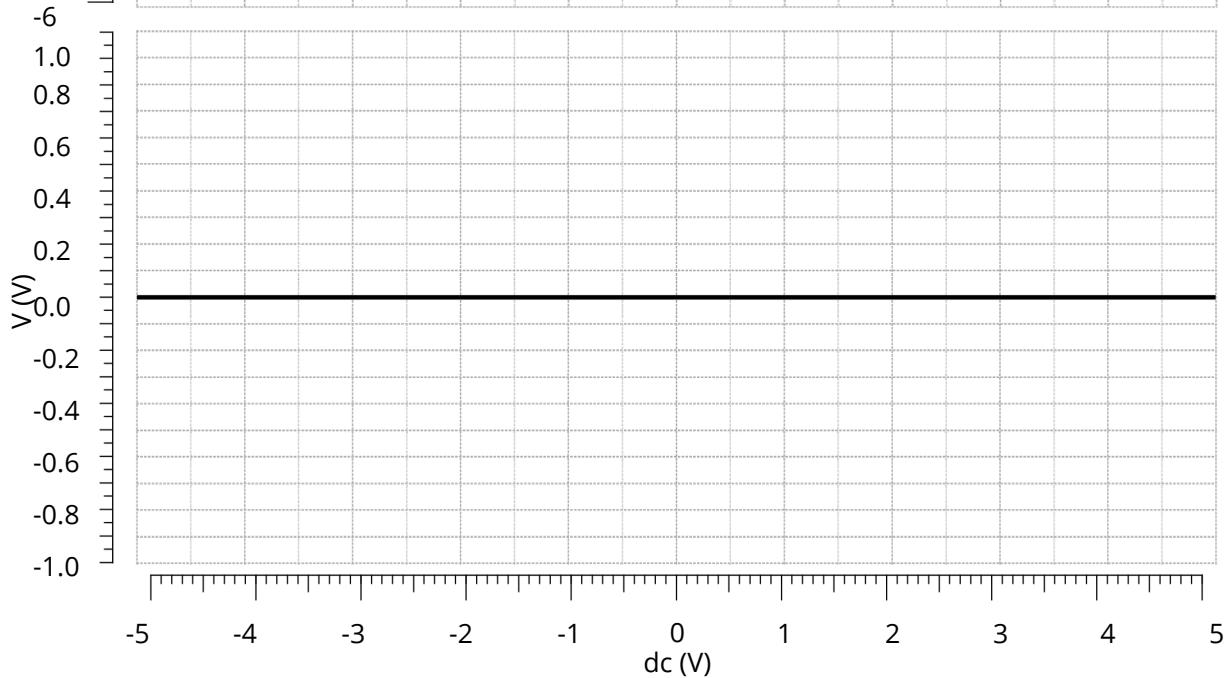
■ /Vout



■ /net020



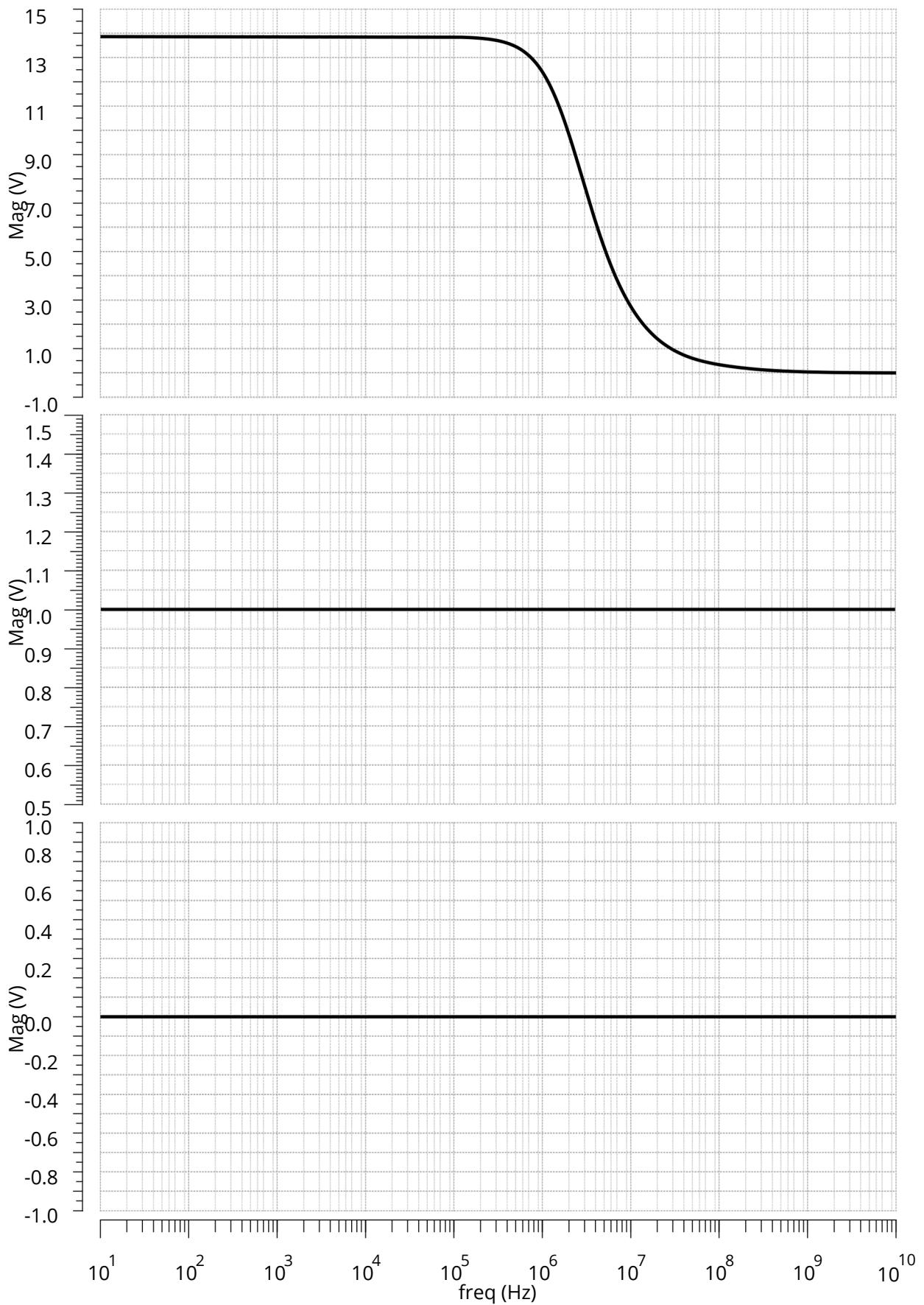
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AC Response

Name _____

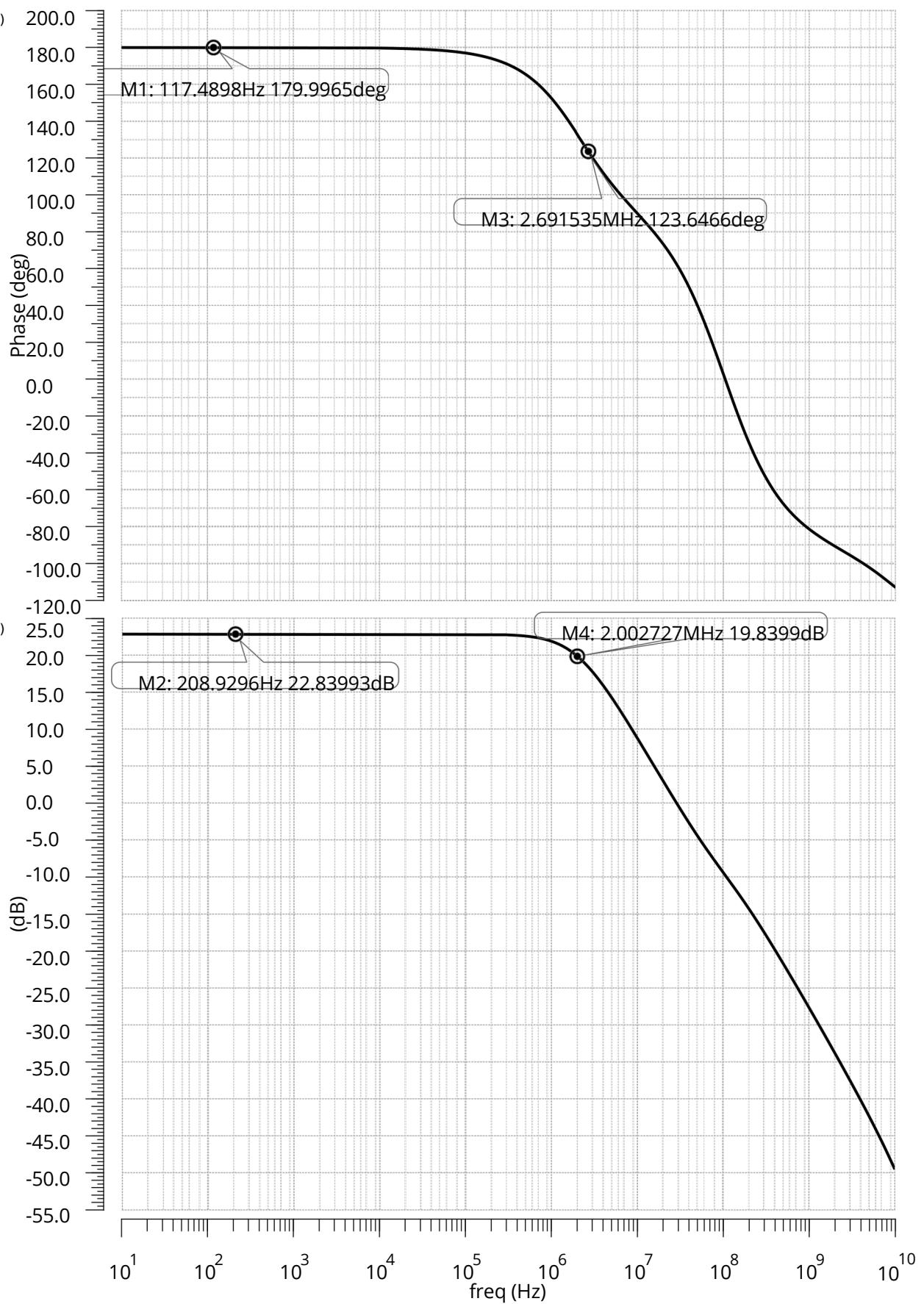
■ /Vout



AC Gain vs Phase

Name

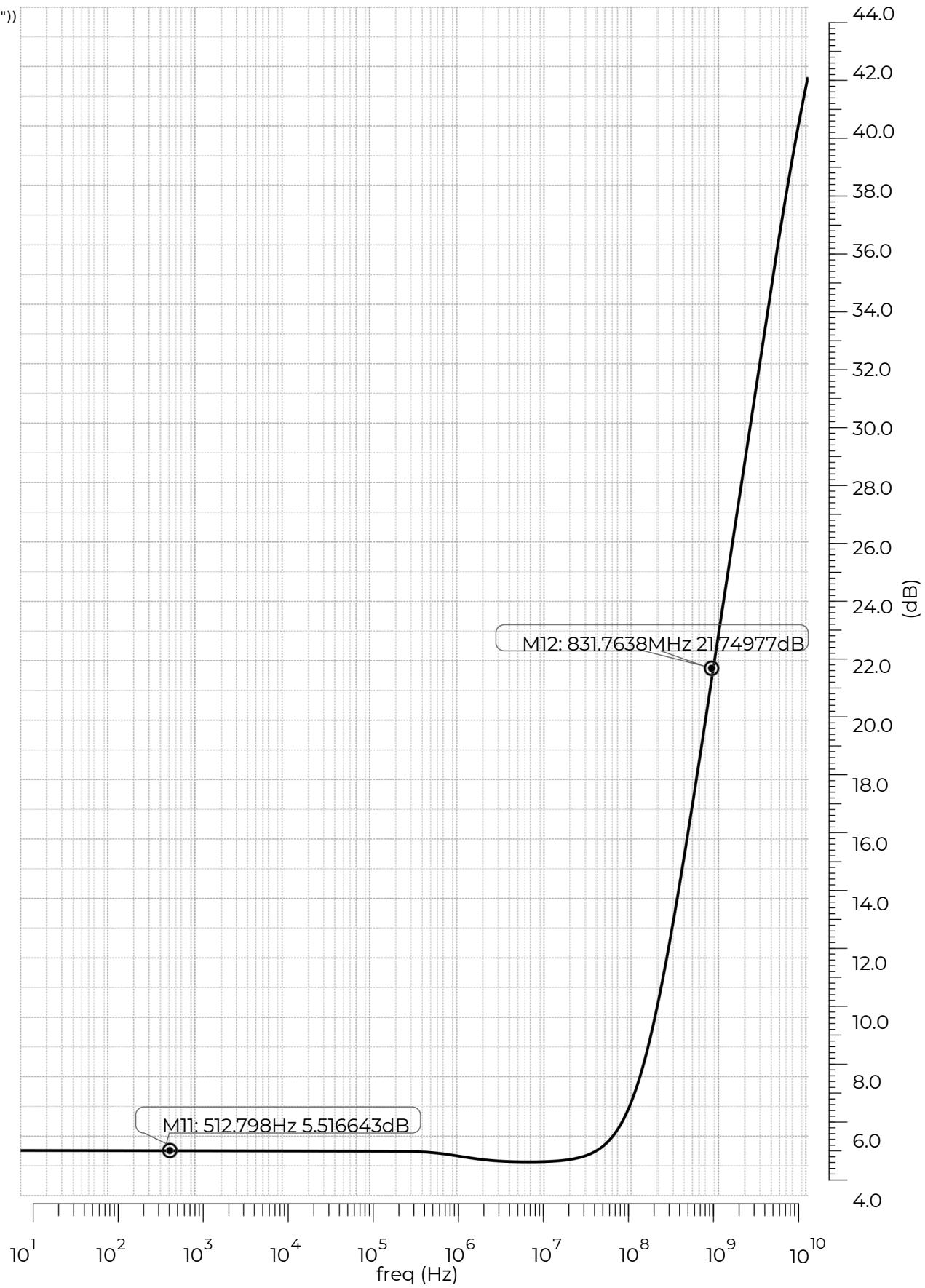
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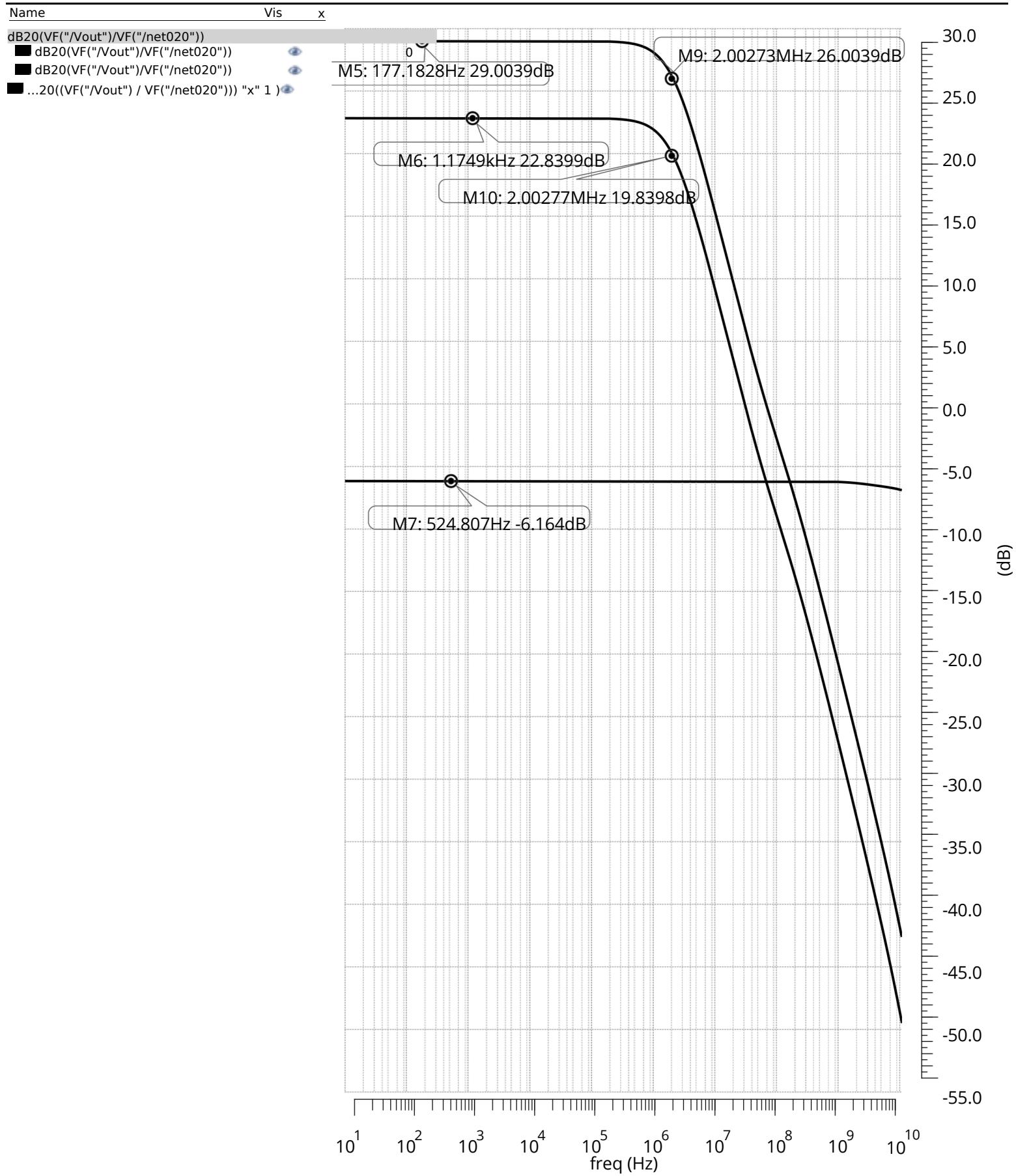
PSRR

Name _____

dB20(VF("/vdd")/VF("/Vout"))



CMRR



Results

	DESIGN 1	DESIGN 2	DESIGN 3	DESIGN 4	DESIGN 5
GAIN	77.8 dB	35 dB	53.36 dB	79.76 dB	22.83 dB
SLEW RATE (V/μS)	0.2	14.52	4.9	9.75	1.71
UNITY GAIN BANDWIDTH	15.84 MHz	23.50 MHz	3 MHz	8 MHz	13 MHz
PSRR	-	127 dB	67.3 dB	83.97 dB	5.51 dB
CMRR	80 dB	6.02 dB	62.45 dB	84.27 dB	6.16 dB

CONCLUSION

The two stage op-amp using Differential amplifier and common source amplifier is designed, simulated and analysed using 90 nm and 180nm technology. It provides high performance with gain of 22.83 db (min) and 79.76db (max) , bandwidth of 3 MHz (min) and 23.50 MHz (max), CMRR of 6.02 db (min) and 84.27 db(max), PSSR of 5.51dB (min) and 127 dB (max). The main purpose of designing a two stage Op-Amp is to obtain high gain, low power consumption, high output swing, greater bandwidth and low noise. However the implementation of Low Dropout Regulators has not been implemented in this.

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