INDIAN INSTITUTE OF INFORMATION TECHNOLOGY,NAGPUR

CMOS FINAL PROJECT

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TOPIC :- SERIAL-IN-PARALLEL-OUT SHIFT REGISTER

CONTENTS

OBJECTIVE

I have design the serial in parallel out shift register by using pass transistor and Verify it using the ngspice and microwind.

INTRODUCTION :

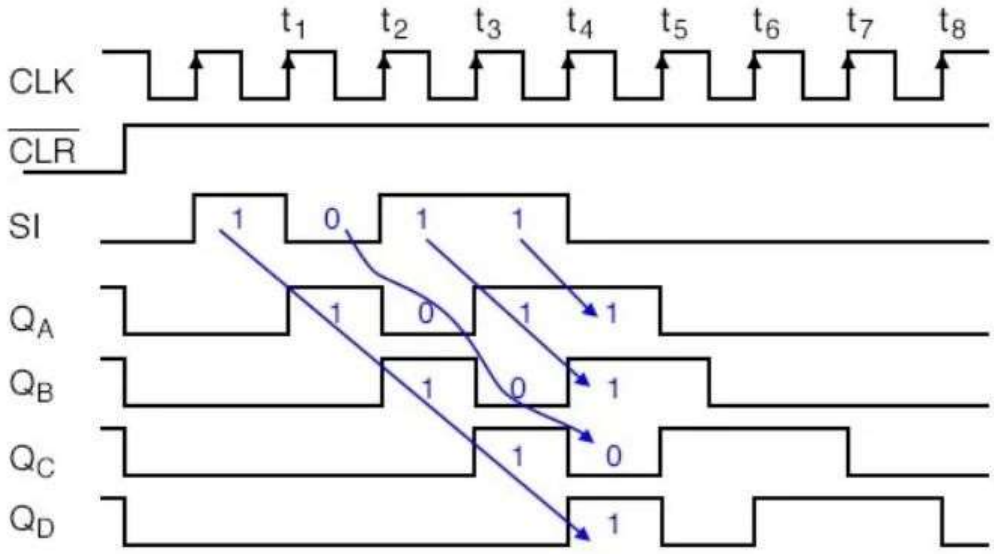
A serial-in, parallel-out shift register is similar to the serial-in, serial-out shift register in that it shifts data into internal storage elements and shifts data out at the serial-out, data-out, pin.

It is different in that it makes all the internal stages available as outputs. Therefore, a serial-in, parallel-out shift register converts data from serial format to parallel format..

that they actually only offer the serial-in, parallel-out shift register, as long as it has no more than 8-bits.

Note that serial-in, serial-out shift registers come in bigger than 8-bit lengths of 18 to 64-bits.

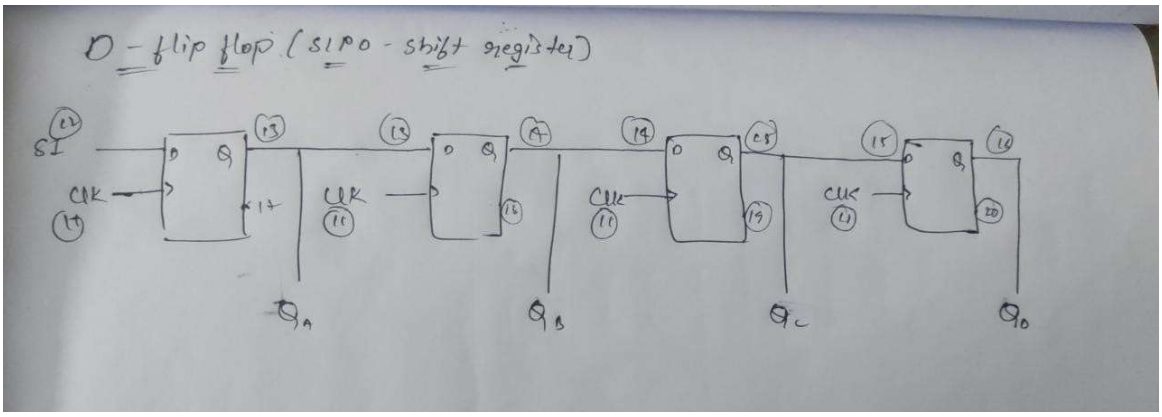
It is not practical to offer a 64-bit serial-in, parallel-out shift register requiring that many output pins. See waveforms below for above shift register.



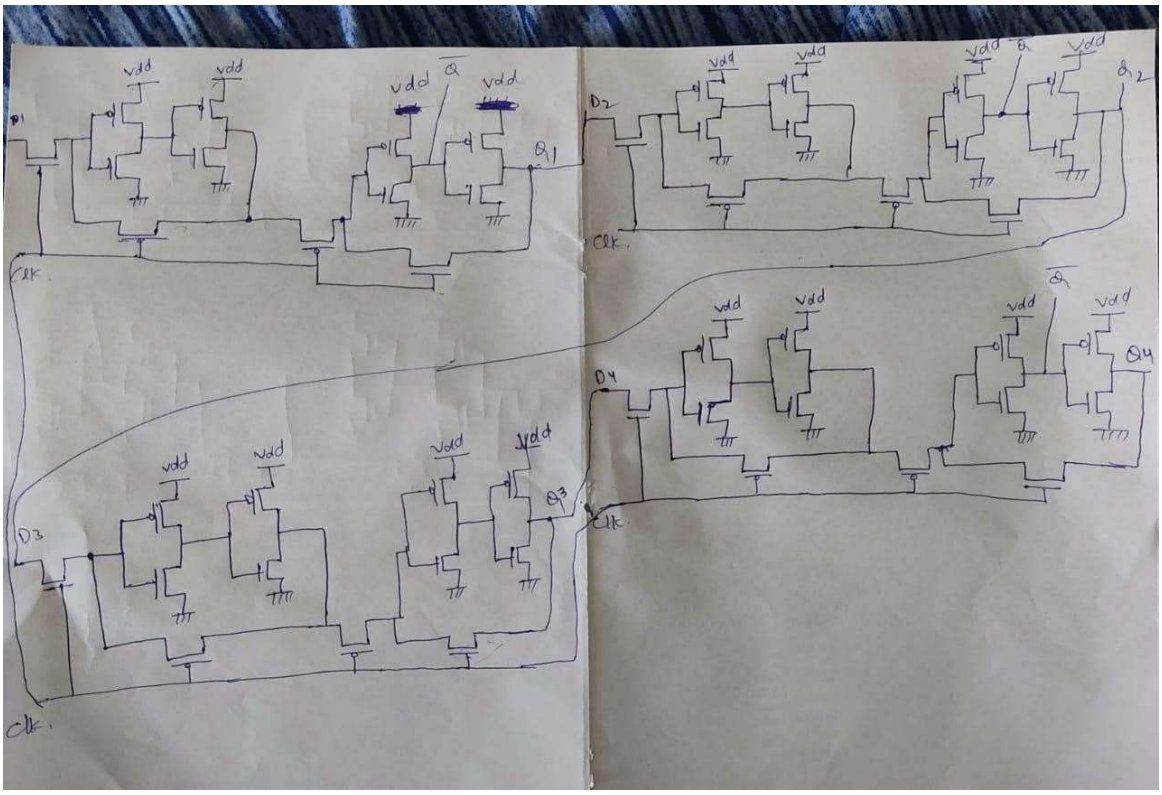
Serial-in/ parallel-out shift register waveforms

Circuit diagrams :-

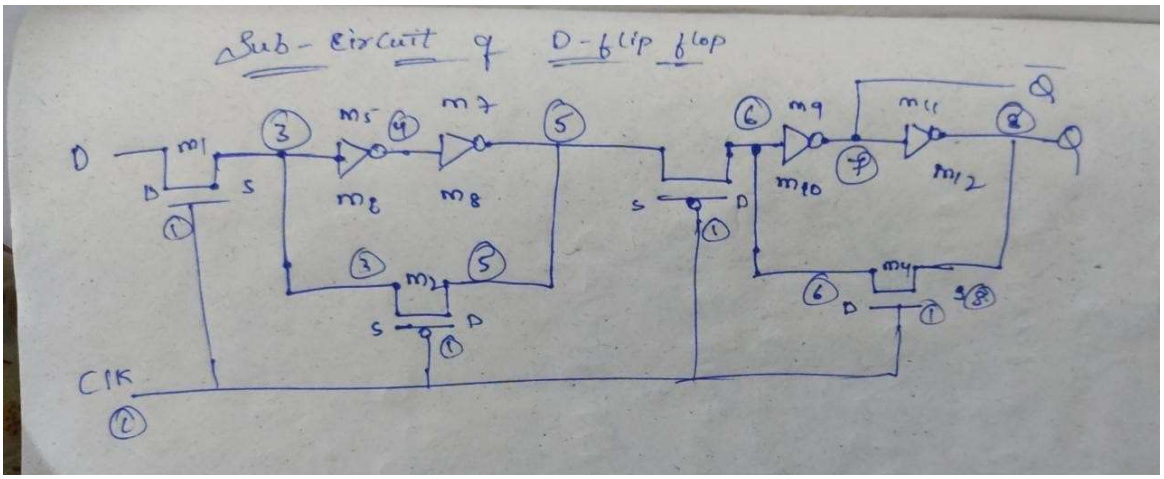
D FLIP FLOP (SIPO SHIFT REGISTER):-



SIPO USING PASS TRANSISTOR CIRCUIT :-



SUB-CIRCUIT OF D-FLIP FLOP:-



Serial in parallel in truth table :-

Clock Pulse	Q1	Q2	Q3	Q4
0	1	0	0	1
1	1	1	0	0
2	0	1	1	0
3	0	0	1	1

SOFTWARES USED:-

ngspice, Microwind.

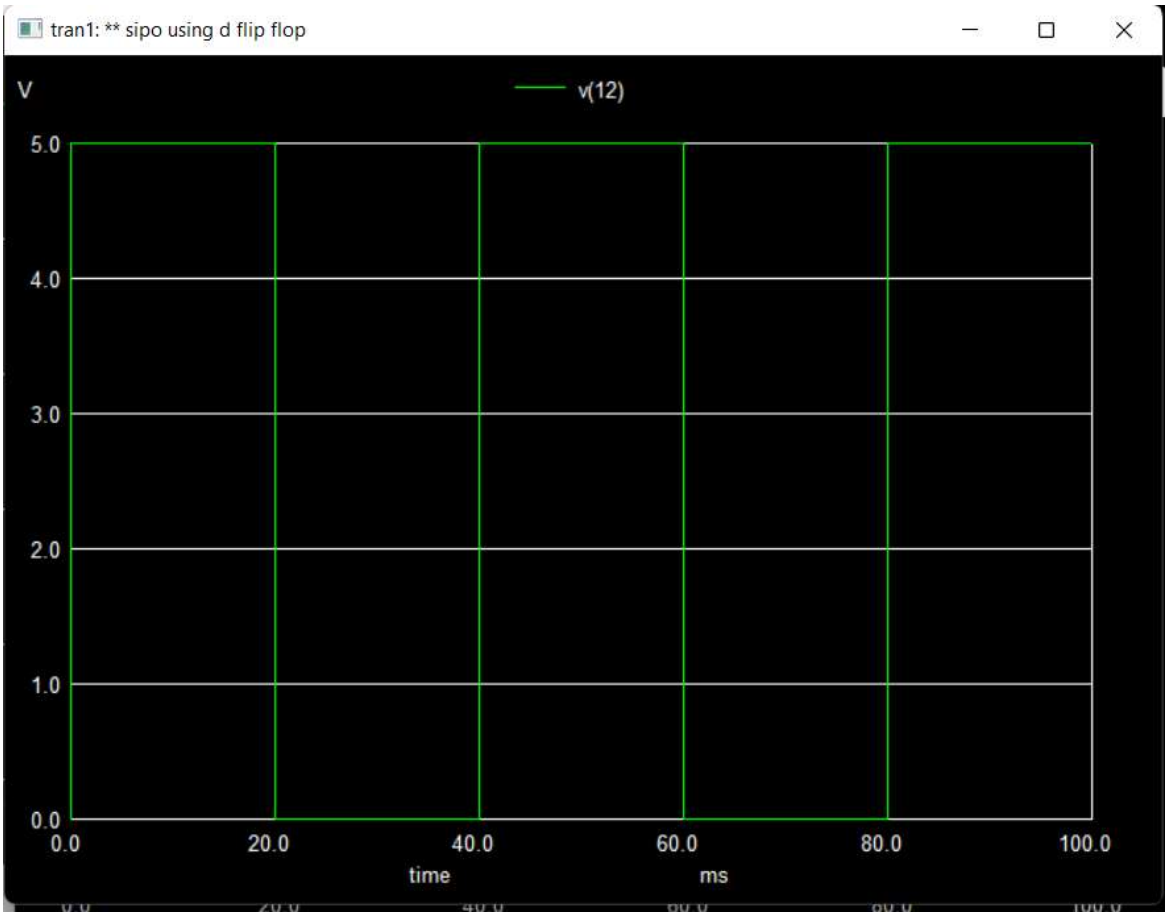
NGSPICE CODE :-

```
** SIPO using D flip flop
.subckt inverter 1 2 3
.model pmod pmos level=54 version=4.7
.model nmod nmos level=54 version=4.7
mp 2 1 3 3 pmod w=100u l=10u
mn 2 1 0 0 nmod w=100u l=10u
.ends

.subckt dff 1 2 7 8
.model pmod pmos level=54 version=4.7
.model nmod nmos level=54 version=4.7
m1 2 1 3 3 nmod w=100u l=10u
m2 5 1 3 3 pmod w=100u l=10u
m3 6 1 5 5 pmod w=100u l=10u
m4 6 1 8 8 nmod w=100u l=10u
m5 4 3 9 9 pmod w=100u l=10u
m6 4 3 0 0 nmod w=100u l=10u
m7 5 4 9 9 pmod w=100u l=10u
m8 5 4 0 0 nmod w=100u l=10u
m9 7 6 9 9 pmod w=100u l=10u
m10 7 6 0 0 nmod w=100u l=10u
m11 8 7 9 9 pmod w=100u l=10u
m12 8 7 0 0 nmod w=100u l=10u
.ends

Vd 1 0 dc 5v
Vp 11 0 pulse(0 5 0 0 0 10m 20m)
Vs 12 0 pulse(0 5 0 0 0 20m 40m)
xd1 11 12 17 13 dff
xd2 11 13 18 14 dff
xd3 11 14 19 15 dff
xd4 11 15 20 16 dff
.tran 0.01ms 100ms
```

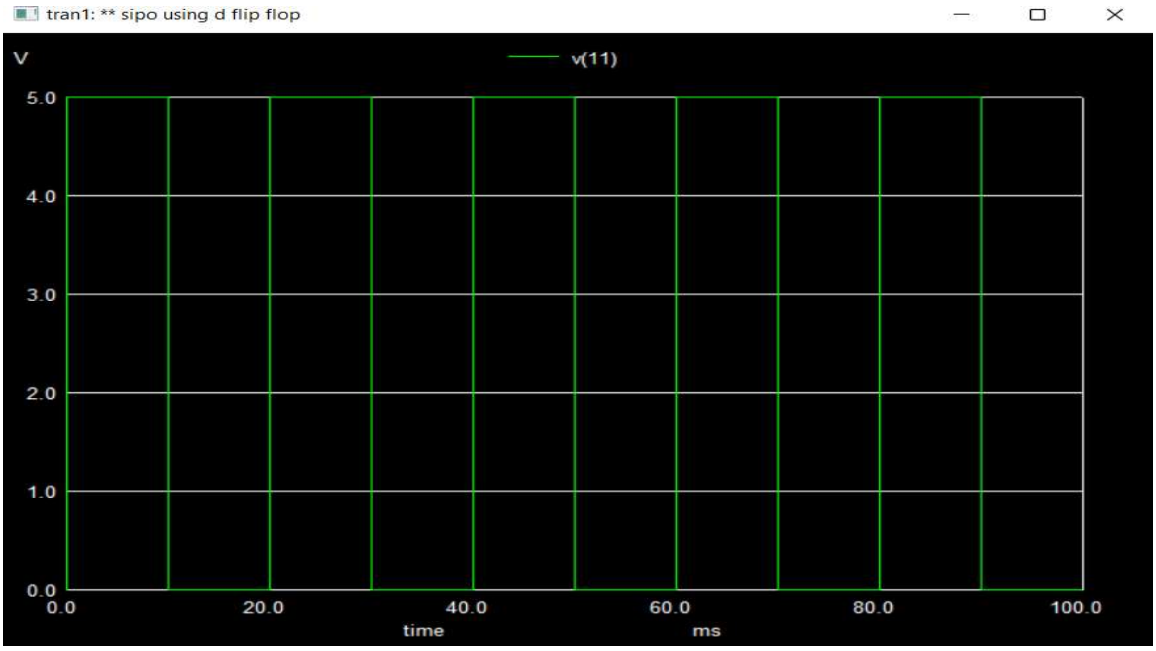
```
.control
run
plot V(11)
plot V(12)
plot V(13)
plot V(14)
plot V(15)
plot V(16)
.endc
.end
```

NGSPICE OUTPUT:-

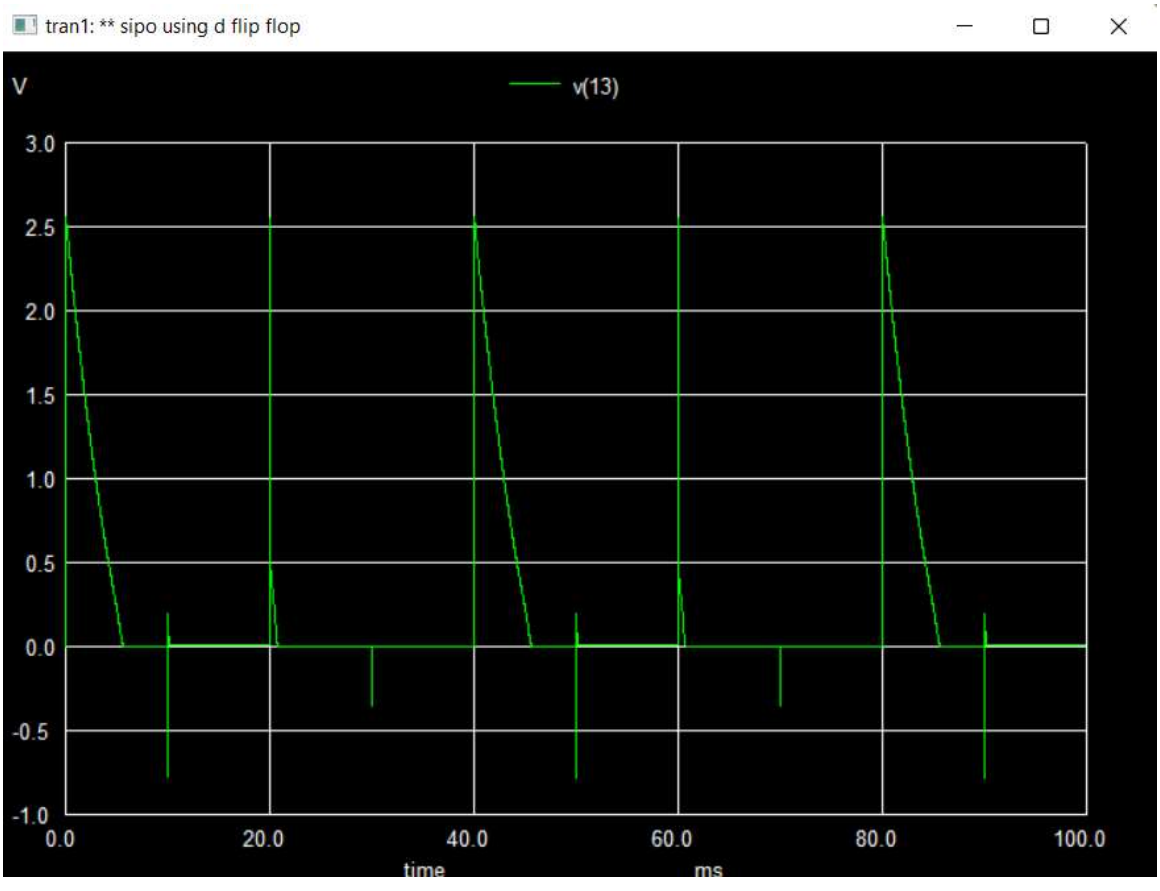
Input graphV(12):-



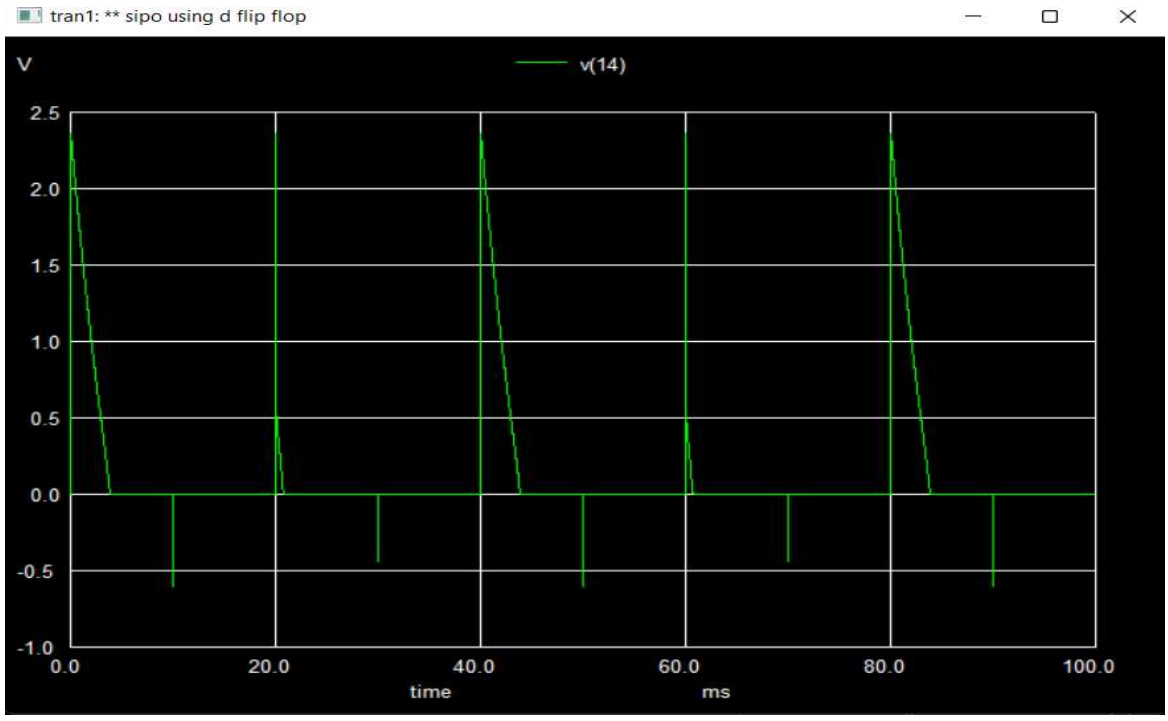
Clock graph(V11):-



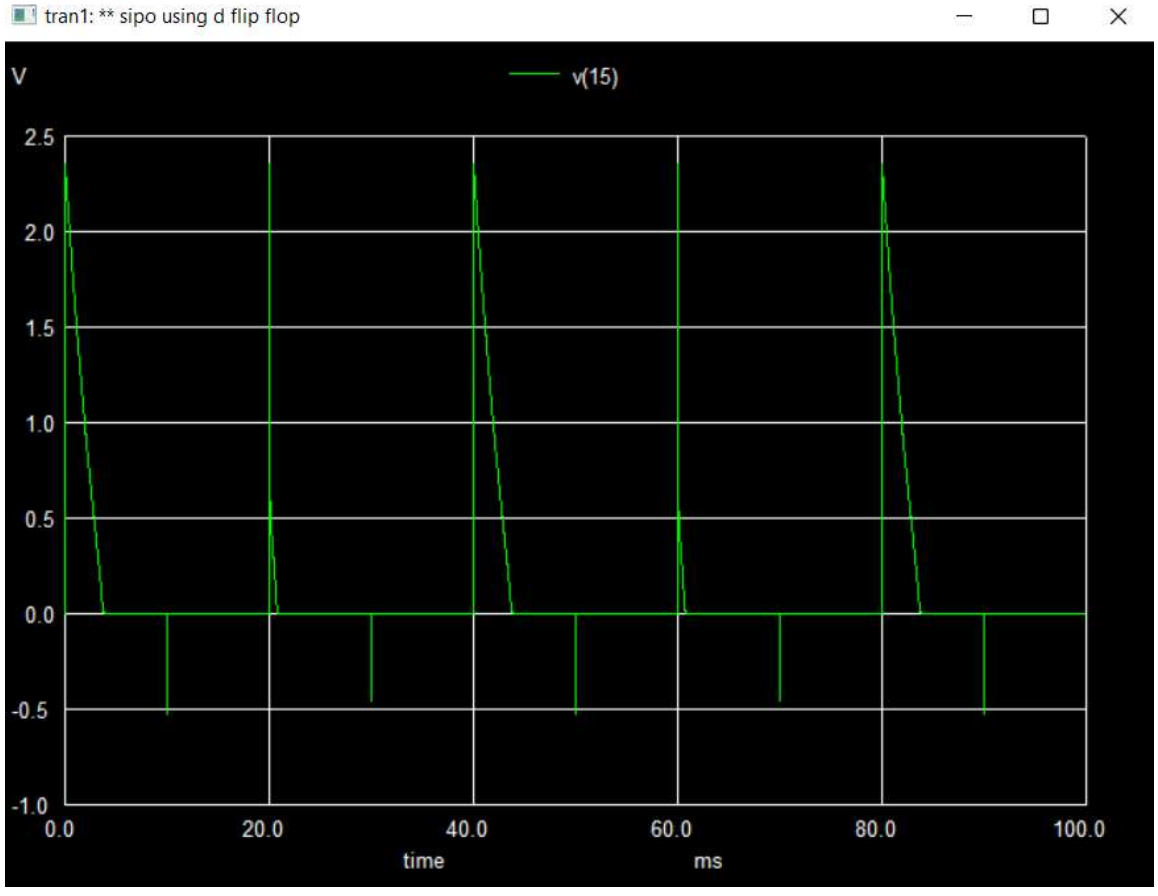
Output graph-1(Qa):-V13



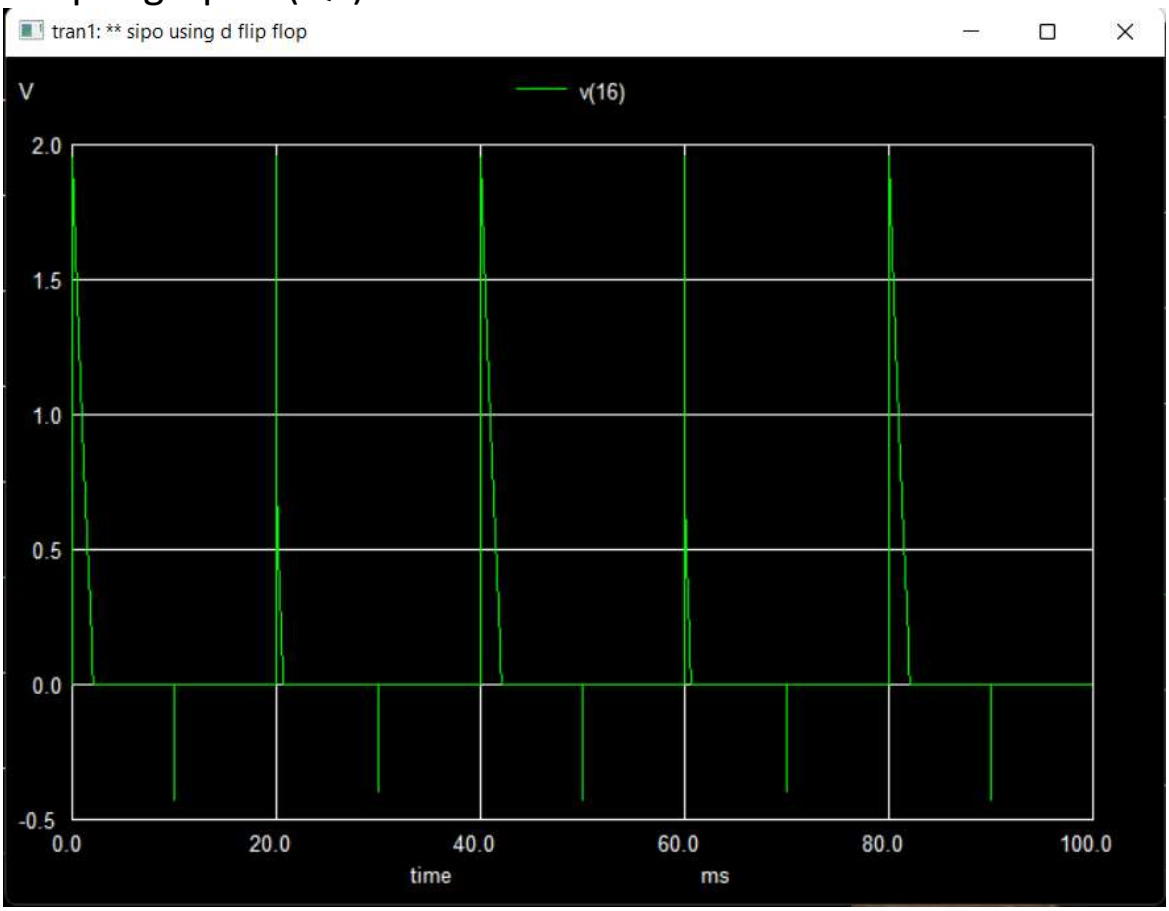
Output graph-2(Qa):-V14



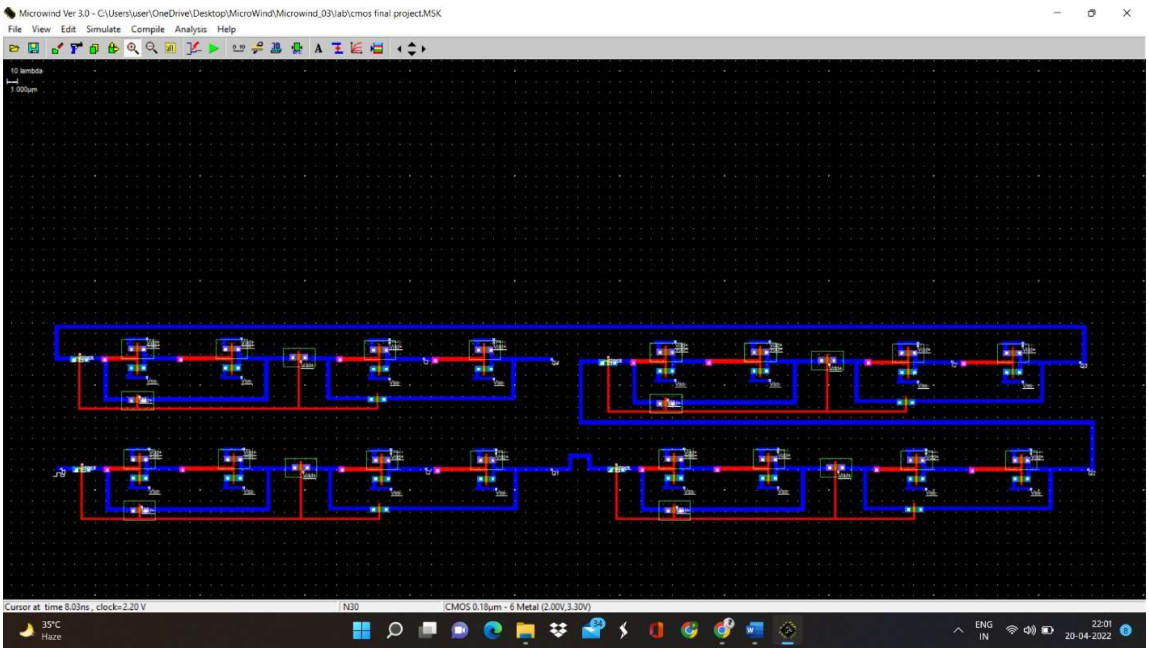
Output graph-3(Qa):-V15



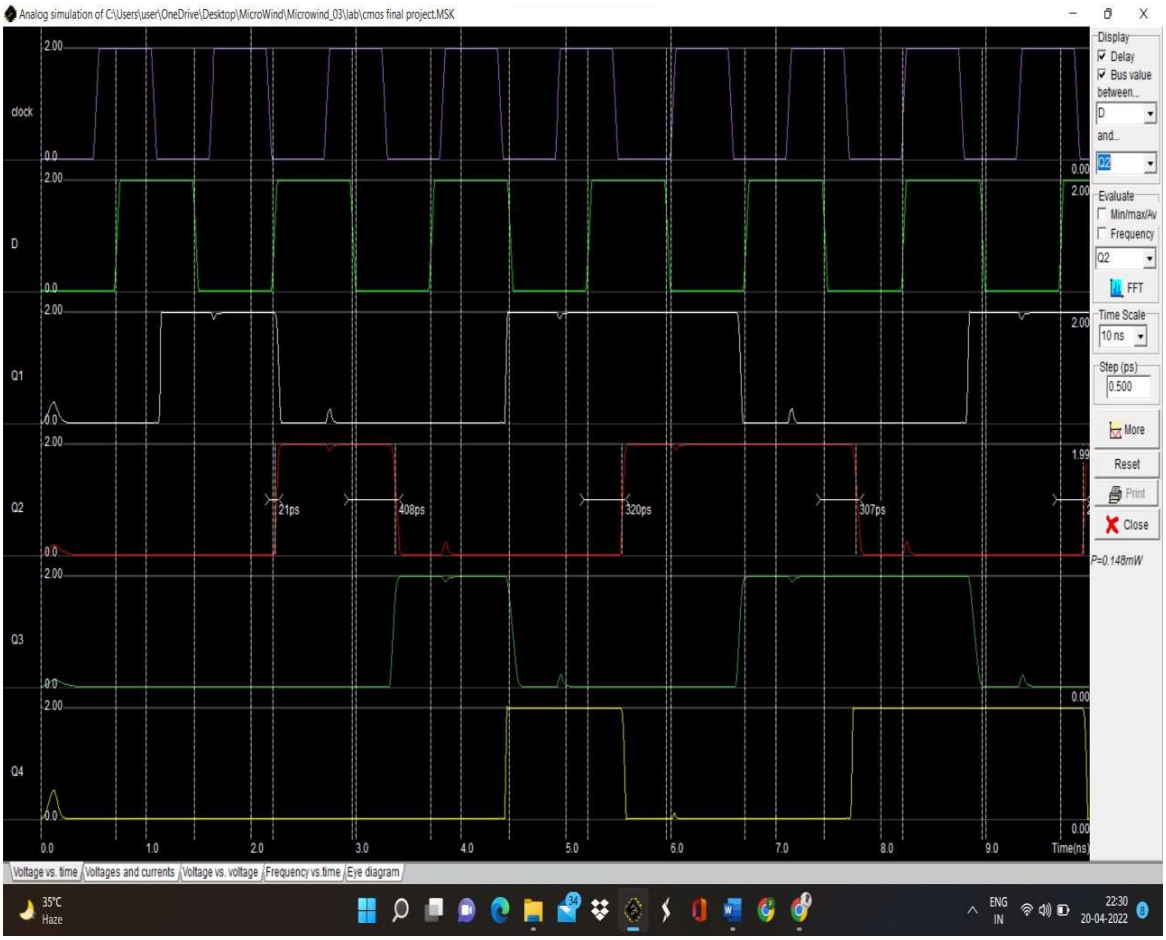
Output graph-4(Qa):-V16



Microwind layout :-



Microwind output :-



CONCLUSION :-

I have successfully completed the circuit design and verified it in ngspice and also designed the layout for it in microwind.