


[UEFI Practice] SlimBootloader Customization

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This article details the configuration mechanism of SBL (Slim Bootloader), including the basic configuration defined by YAML files, the overriding configuration of DLT files, and the use of configuration tools. YAML files contain settings such as memory and Silicon, while DLT files are used to customize according to specific boards. The configuration tool ConfigEditor.py provides a graphical interface for loading and editing configurations and generating binary configuration files. Post-build customization allows parameters to be adjusted after the SBL is built.

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Overview

One of the features of SBL is Customizable, which is divided into pre-build and post-build customization.

SBL has two types of configuration data, internal configuration data and external configuration data. Internal configuration data is the default data hard-coded in the code, and is used when external data cannot be obtained; external configuration data is generated through predefined files and configuration tools.

The predefined files and configuration tools in SBL include:

- YAML file: It defines the configuration;
- DLT (delta, which actually means variable data) file: Override data, used to override the configuration in the YAML file;
- Configuration operation tool: usually a Python script.

YAML File

The YAML file includes memory, Silicon, GPIO, startup strategy, security configuration, etc.

YAML files are usually included in a specific board directory, such as the ApolloLake platform:

slimbootloader > Platform > ApollolakeBoardPkg > CfgData			
名称	修改日期	类型	大小
CfgData_BootOption.yaml	2021/9/26 0:51	YAML 文件	1 KB
CfgData_CapsuleInformation.yaml	2021/9/26 0:51	YAML 文件	3 KB
CfgData_DeviceEnable.yaml	2021/9/26 0:51	YAML 文件	1 KB
CfgData_Ext_Gpmrb.dlt	2020/6/27 19:20	DLT 文件	27 KB
CfgData_Ext_JuniperHill.dlt	2020/6/27 19:20	DLT 文件	3 KB
CfgData_Ext_MB3.dlt	2020/6/27 19:20	DLT 文件	11 KB
CfgData_Ext_OxbHill.dlt	2020/6/27 19:20	DLT 文件	3 KB
CfgData_Ext_Up2.dlt	2021/9/26 0:51	DLT 文件	2 KB
CfgData_Features.yaml	2021/9/26 0:51	YAML 文件	1 KB
CfgData_Gpio.yaml	2021/9/26 0:51	YAML 文件	23 KB
CfgData_GpioPinOption.yaml	2021/9/26 0:51	YAML 文件	4 KB
CfgData_GpuConfig.yaml	2021/9/26 0:51	YAML 文件	3 KB
CfgData_Hdayaml	2021/9/26 0:51	YAML 文件	8 KB
CfgData_Int_LesHill.dlt	2020/6/27 19:20	DLT 文件	1 KB
CfgData_Memory.yaml	2021/9/26 0:51	YAML 文件	10 KB
CfgData_MemSpd.yaml	2021/9/26 0:51	YAML 文件	8 KB
CfgData_PcieRp.yaml	2021/9/26 0:51	YAML 文件	2 KB
CfgData_PidGpioPins.yaml	2021/9/26 0:51	YAML 文件	1 KB
CfgData_Power.yaml	2021/9/26 0:51	YAML 文件	5 KB
CfgData_Security.yaml	2021/9/26 0:51	YAML 文件	1 KB
CfgData_SgxConfig.yaml	2021/9/26 0:51	YAML 文件	3 KB
CfgData_Silicon.yaml	2021/9/26 0:51	YAML 文件	1 KB
CfgData_Usb.yaml	2021/9/26 0:51	YAML 文件	1 KB
CfgDataDef.yaml	2021/9/26 0:51	YAML 文件	5 KB
CfgDataDynamic.yaml	2021/9/26 0:51	YAML 文件	2 KB
Template_CfgData.yaml	2021/9/26 0:51	YAML 文件	10 KB
Template_DeviceEnable.yaml	2021/9/26 0:51	YAML 文件	14 KB
Template_PcieRp.yaml	2021/9/26 0:51	YAML 文件	6 KB
Template_Spd.yaml	2021/9/26 0:51	YAML 文件	1 KB

There are also some common YAML files in the Platform/CommonBoardPkg/CfgData directory:

slimbootloader > Platform > CommonBoardPkg > CfgData			
名称	修改日期	类型	大小
CfgData_Common.yaml	2021/9/26 0:51	YAML 文件	3 KB
CfgData_Default.dlt	2020/6/27 19:20	DLT 文件	1 KB
CfgData_Platform.yaml	2021/9/26 0:51	YAML 文件	2 KB
CfgData_Tcc.yaml	2021/9/26 0:51	YAML 文件	2 KB
Template_BootOption.yaml	2021/9/26 0:51	YAML 文件	6 KB

The configuration file entry required by the platform is `CfgDataDef.yaml` , and other configuration files are included as its sub-files `CfgDataDef.yaml` . For example, Platform/ApollolakeBoardPkg/CfgData/CfgDataDef.yaml:

yaml

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```
1 ## @file
2 #
3 # Slim Bootloader CFGDATA Default File.
4 #
5 # Copyright (c) 2020, Intel Corporation. All rights reserved.<BR>
6 # SPDX-License-Identifier: BSD-2-Clause-Patent
7 #
8 ##
9
10 variable:
11   COND_GPIO_SKIP           : ($GPIO_CFG_DATA.$(1)_Half0.GpioSkip == 0)
12   COND_GPIO_PID_ENABLE     : ($PID_GPIO_CFG_DATA.$(1).Enable==1) and ($PLATFORMID_CFG_DATA.PlatformId==0)
13   COND_PCIE_RP_Pwr_PIN_SKIP : ($PCIE_RP_CFG_DATA.PcieRpPowers$(1).Skip == 0)
14   COND_PCIE_RP_RST_PIN_SKIP : ($PCIE_RP_CFG_DATA.PcieRpResets$(1).Skip == 0)
15   COND_PCIE_RP_EN          : ($PCIE_RP_CFG_DATA.PcieRpFeatures$(1).En == 1)
16   COND_PCIE_RP_CLK_REQ_SUP : (($PCIE_RP_CFG_DATA.PcieRpFeatures$(1).ClrReqSup == 1) and ($PCIE_RP_CFG_DATA.PcieRpFeatures$(1).En == 1))
17   COND_HDA_EN              : ($HDA_CFG_DATA.HdaEnable == 1)
18   COND_HDA_DSP_EN          : (($HDA_CFG_DATA.HdaEnable == 1) and ($HDA_CFG_DATA.DspEnable == 1))
19
20 template:
21
22 twen
23 twen - !include Template_CfgData.yaml
24 twen
25 configs:
26   25 - $ACTION      :
27   26   page         : PLT::"Platform", MEM::"Memory Settings", SIL::"Silicon Settings", GEN::"General Settings", GIO::"Gpio Settings", OS::"OS Boot Options"
27   27 - Signature    :
28   28
```

```

29     length      : 0x04
30     value       : {'CFG0'}
31 - HeaderLength :
32     length      : 0x01
33     value       : 0x10
34 - Reserved     :
35     length      : 0x03
36     value       : {0,0,0}
37 - UsedLength   :
38     length      : 0x04
39     value       : _LENGTH_
40 - TotalLength  :
41     length      : 0x04
42     value       : 0x2000
43
44 - !include Platform/CommonBoardPkg/CfgData/CfgData_Platform.yaml
45
46 - $ACTION      :
47     page       : IOCUART:PLT:"IOC Uart Settings"
48 - $ACTION      :
49     page       : IOCUART
50 - IOC_UART_CFG_DATA :
51 - !expand { CFGHDR_TMPL : [ IOC_UART_CFG_DATA, 0x120, 0, 0 ] }
52 - DeviceIndex  :
53     name       : Device Index
54     type       : Combo
55     option     : 0:UART0, 1:UART1, 2:UART2, 3:UART3, 0xF:Disable
56     help       : >
57                 UART device index for IOC interface (0..3 or Disable)
58     length     : 0x01
59     value      : 0xF
60 - BaudRate     :
61     name       : Baud Rate
62     type       : Combo
63     option     : 0:9600, 1:19200, 2:38400, 3:57600, 4:115200, 5:921600, 6:1.5M
64     help       : >
65                 UART Baud Rate
66     length     : 0x01
67     value      : 0
68 - Retries      :
69     name       : Retries
70     type       : EditNum, HEX, (0x00,0xFF)
71     help       : >
72                 specify retry count
73     length     : 0x01
74     value      : 0
75 - TimeoutInitial :
76     name       : TimeoutInitial
77     type       : EditNum, HEX, (0x00,0xFF)
78     help       : >
79                 initial/setup time-out (in milliseconds)
80     length     : 0x01
81     value      : 0
82 - TimeoutXmit   :
83     name       : TimeoutXmit
84     type       : EditNum, HEX, (0x00,0xFF)
85     help       : >
86                 transmission time-out
87     length     : 0x01
88     value      : 0
89 - Rsvd          :
90     length     : 0x03
91     value      : 0
92
93 - $ACTION      :
94     page       : PSEL:PLT:"Payload Selection GPIO"
95 - $ACTION      :
96     page       : PSEL
97 - PLATFORM_CFG_DATA :
98 - !expand { CFGHDR_TMPL : [ PLATFORM_CFG_DATA, 0x280, 0, 0 ] }
99 - PayloadSelGpio :
100 - $STRUCT      :
101     name       : GPIO pin for switching payload
102     struct     : PAYLOAD_SEL_GPIO_PIN
103     length     : 0x04
104     value      : 0x000000c5
105 - PadInfo      :
106     name       : Pin Number
107     type       : Combo
108     option     : !include CfgData_GpioPinOption.yaml
109     condition  : ($PLATFORM_CFG_DATA.PayloadSelGpio.Enable > 0)
110     help       : >
111                 Specify GPIO Pin Number
112     length     : 24b
113 - Rsvd1        :
114     name       : Reserved
115     type       : Reserved
116     length     : 7b
117 - Enable       :
118     name       : Payload Selection Pin Enable
119     type       : Combo
120     option     : $EN_DIS
121     help       : >
122                 Enable/Disable this pin for payload selection.
123     order      : 0000.0000
124     length     : 1b
125
126 - !include CfgData_Memory.yaml
127 - !include CfgData_Silicon.yaml
128 - !include CfgData_Usb.yaml
129 - !include CfgData_Gpio.yaml
130 - !include Platform/CommonBoardPkg/CfgData/CfgData_Common.yaml
131 - !include CfgData_BootOption.yaml
132 - !include CfgData_PidGpioPins.yaml
133 - !include CfgData_PcieRp.yaml
134 - !include CfgData_GpuConfig.yaml
135 - !include CfgData_Features.yaml
136 - !include CfgData_DeviceEnable.yaml
137 - !include CfgData_Hda.yaml
138 - !include CfgData_CapsuleInformation.yaml

```

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You can see that it contains many `include` commands, specifying YAML files such as memory, Silicon, USB, GPIO, etc.

DLT File

The data in the DLT file is used to override the configuration in the YAML file.

The DLT file contains one PlatformId , such as Platform\ApollolakeBoardPkg\CfgData\CfgData_Ext_Up2.dlt:

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```
1 #
2 # Delta configuration values for platform ID 0x000E
3 #
4 PLATFORMID_CFG_DATA.PlatformId      | 0x000E
```

There can be multiple DLT files in a platform, each corresponding to one PlatformId and eventually matching a specific board. If PlatformId it is equal to 0, it means that it is applicable to all boards, which is equivalent to changing the YAML file itself. These DLT files correspond to BoardConfig.py:

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```
1 self._CFGDATA_EXT_FILE = ['CfgData_Ext_Gpmrb.dlt', 'CfgData_Ext_Up2.dlt','CfgData_Ext_0xbHill.dlt','CfgData_Ext_MB3.dlt','CfgData_Ext_JuniperHill.dlt']
```

If you need to add a single board, you usually do not modify the YAML file directly. Instead, you add a DLT file and modify the configuration to overwrite the original configuration, and add the DLT file to the above list.

By the way PlatformId , Intel's CRB board specifies several GPIO pins, and specifies a specific board through hardware configuration, so that the code can determine it by reading the GPIO value PlatformId . For the ApolloLake platform, the relevant code can be seen in Platform\ApollolakeBoardPkg\Library\Stage1BBoardInitLib\Stage1BBoardInitLib.c:

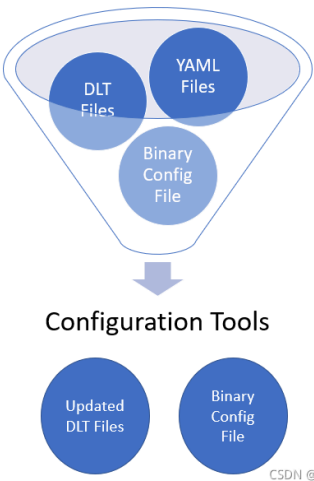
cAI generated projects登录复制run

```
1 /**
2  Detect board and configure PlatformID.
3
4  @retval EFI_SUCCESS    Configuration data was loaded successfully.
5  @retval Others         Failed to get configuration data blob.
6  */
7 EFI_STATUS
8 EFIAPI
9 PlatformIdInitialize (
10 IN VOID
11 )
12 {
13     UINT16    PlatformId;
14
15     PlatformId = (UINT16)GetBoardIdFromGpioPins ();
16
17     if (PlatformId != 0xFF) {
18         PlatformId += 0x10; // Customer board identified, assign Platform Ids from 16 to 31
19     } else {
20         PlatformId = (UINT16)GetEmbeddedBoardId ();
21         //Platform ID from GPIOs are read as 0 for Juniper hills due to GPIO pins
22         //on the board reduced from 4 to 3 (hardware change) hence translating here
23         //in the code.
24         if (PlatformId == 0){
25             DEBUG ((DEBUG_INFO, "GPIO returned platformID 0 translating to 8(JNH)\n"));
26             PlatformId = 0x8;
27         }
28         if ((PlatformId != PLATFORM_ID_0XH) && (PlatformId != PLATFORM_ID_LFH) && (PlatformId != PLATFORM_ID_JNH)) {
29             PlatformId = (UINT16)GetIvBoardId ();
30             if (PlatformId != PLATFORM_ID_GPMRB) {
31                 DEBUG ((DEBUG_ERROR, "BOARD NOT SUPPORTED: 0x%04X\n", PlatformId));
32                 CpuDeadLoop ();
33             }
34         }
35     }
36
37     SetPlatformId (PlatformId);
38     return EFI_SUCCESS;
39 }
```

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Configuration Tools

The way the configuration tool processes YAML and DLT files looks like this (note that binary files can be used as both input and output):

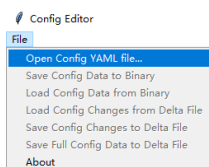


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So this section introduces the configuration tool, which is located in the BootloaderCorePkg\Tools directory. The most important one is ConfigEditor.py, which is a graphical tool. After opening it, it looks like this:



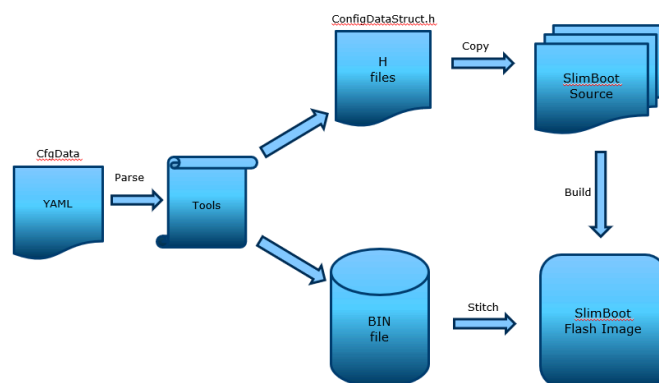
Click "File". For the first time, you can only select "Open Config YAML file...":



Here you can select the CfgDataDef.yaml mentioned above, which is the basic configuration file. After that, you can select "Load Config Changes from Delta File", so that the newly added DLT file will overwrite the original display, and then you can continue to modify and finally save the modified data. Such data can be a DLT file containing only the modified part, or a DLT file that covers all configurations, or directly generate a binary file.

In addition to ConfigEditor.py, there is also a configuration tool used to convert the YAML file into the header file Platform\XXXPkg\Include\ConfigDataStruct.h, which will be included in the SBL code to finally obtain and use the configuration through the code.

The final configuration tool usage process is as shown in the following figure:



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In general, the configuration of SBL is the basic configuration defined by the YAML file, and the DLT file modifies the configuration according to the actual board, and finally generates a binary configuration file, which will be placed in the SBL binary for subsequent retrieval. In the SBL code, the current one will be judged **PlatformId** and the required binary configuration file will be loaded to complete the final configuration.

Finally, even after the SBL binary is generated, its parameters can still be modified through tools, which is called post-build customization.