UEFI - Accessing PCI/PCIe devices (I)

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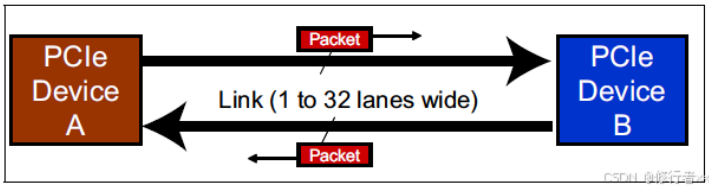
1. PCI/ PCIE

1.1 Introduction to PCI/PCIe

PCI (Peripheral Component Interconnect, PCI) in Chinese means peripheral component interconnect. The so-called peripheral components refer to devices other than CPU , memory and chipset. These devices are usually connected to the computer's motherboard through various interfaces to expand the computer's functions and performance, such as disks, network cards, sound cards, graphics cards, etc. Its main purpose is to connect peripheral devices and combine low-speed devices with high-speed processors to meet users' increasing requirements for data transmission rates. PCIe (PCI Express), PCI expansion is developed on the basis of PCI. The biggest difference is that PCI uses parallel transmission and PCIE uses serial.

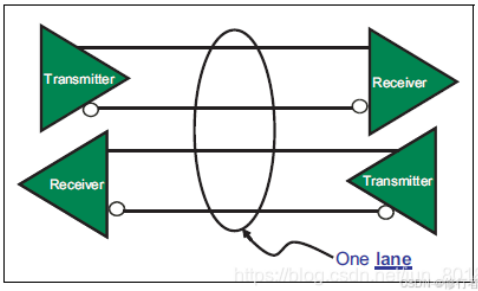
Link: A physical connection between two PCIe devices. A link consists of multiple lanes. The number of lanes determines the width of the link, i.e. the x value. For example, an 8x Link contains 8 lanes and a 16x Link contains 16 lanes.

Figure 2-1: Dual-Simplex Link



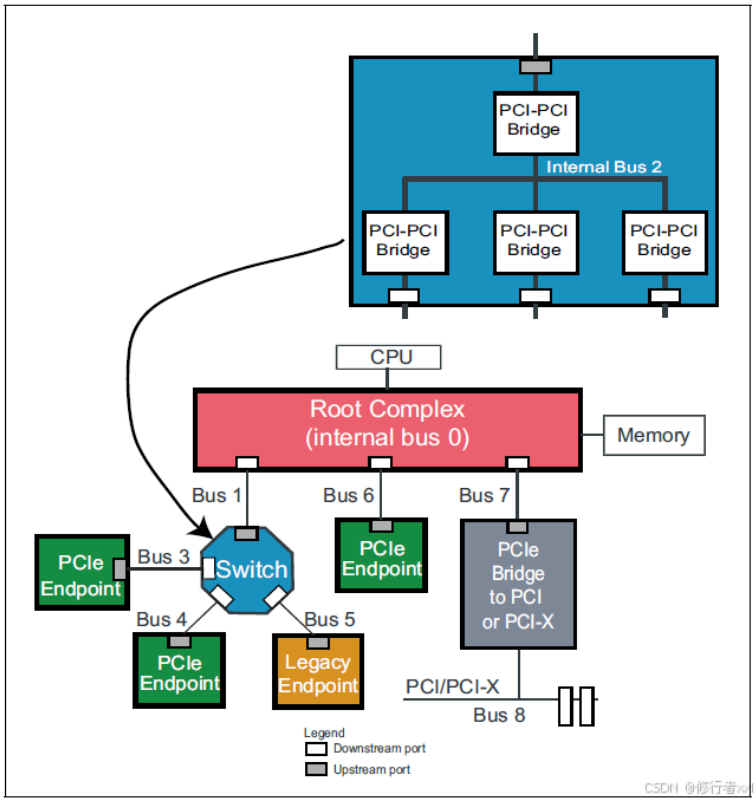
PCIe uses dual simplex mode for connection, that is, each lane has a single send path and a single receive path.

Figure 2-2: One Lane



1.2 PCIe topology

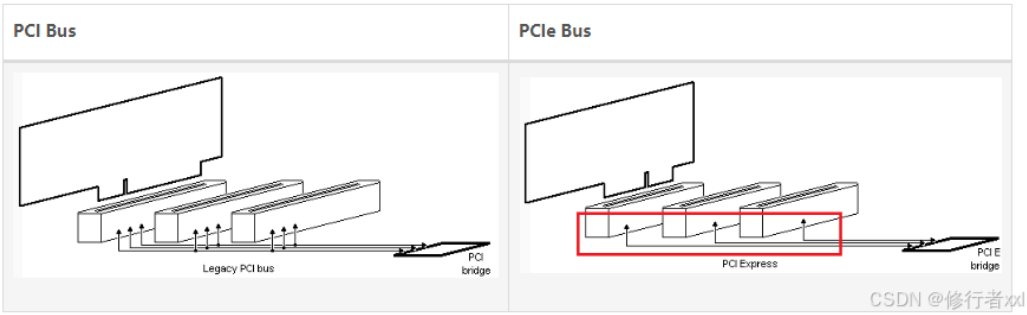
The topology of PCIe is shown in the following figure:



The PCIe topology is a tree topology, which mainly includes Root Complex, PCIe BUS, Endpoint, Port and Bridge, Switch

Root Complex: It is the root node of the PCIe device tree. The CPU is connected to the PCIe bus through it and ultimately to all PCIe devices. (Now it is basically integrated into the CPU) Although it is the root node of the device tree, there is more than one Root Complex.

PCIe Bus: Devices on PCIe are connected to each other through the PCIe Bus. PCIe Bus is a point-to-point network. When devices on the Root Complex or PCIe need to communicate, they will connect to each other directly or use a switching circuit for point-to-point signal transmission.



Endpoint: The endpoint is the device in the PCIe topology, not a switch or bridge, but a functional device.

Switch: The function of a switch is to expand the PCIe port and provide routing and forwarding functions for the devices mounted on it.

Port and Bridge:

A bridge provides an interface to other buses, such as PCI or PCI-X, or even another PCIe bus.
Bridging is the function of interconnecting a PCI/PCI-X bus segment or PCI Express Port with internal components or with another PCI/PCI-X bus segment or PCI Express Port virtually or physically.
A PCIe bridge can convert a PCIe bus to a PCI bus for connecting PCI devices.
A PCIe bridge can convert a PCI bus to a PCIe bus (reverse bridge) for connecting PCIe devices.

There are two types of PCIe devices: type 0 represents the end device, such as our common graphics card, network card, and sound card; type 1 represents a switch or root port, which is used to connect other PCIe devices

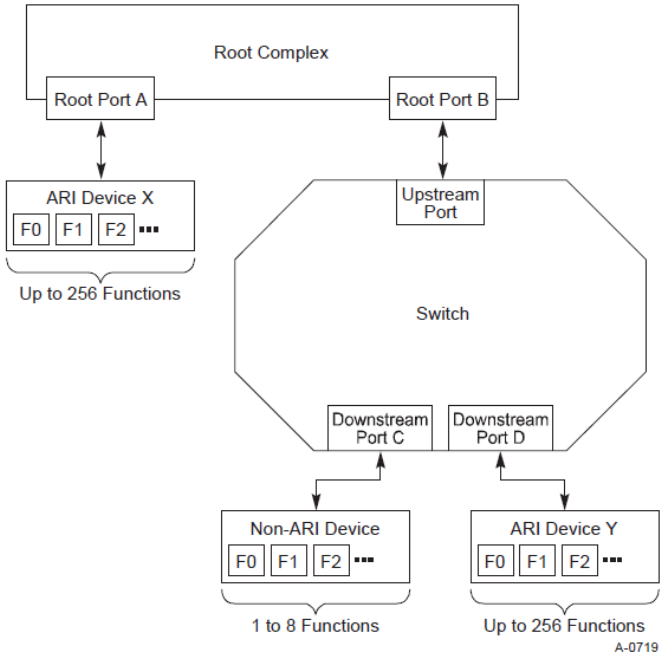


Figure 6-13: Example System Topology with ARI Devices

1.3 BDF

BNF (Bus Number, Device Number, Function Number), all devices on PCIe, whether type0 or type1, will be assigned a unique address when the system starts. It consists of three parts:

Bus Number: 8 bits, which means a maximum of 256 buses

Device Number: 5 bits, up to 32 devices

Function Number: 3 bits, up to 8 functions

2. Accessing PCI/PCIe devices in UEFI environment

2.1 Mechanisms for communicating with PCI/PCIe devices

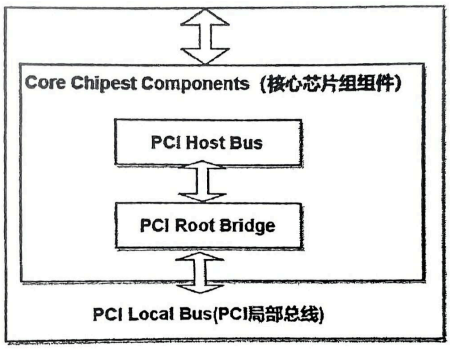
The main discussion here is about accessing PCi and PCIe devices in the UEFI environment. From the perspective of a software engineer, when accessing PCI/PCIe devices, you only need to answer two questions.

(1) How to find the device you want to access in the system

(2) After finding the device, how to access the registers or other resources in the device

2.1.1 How to find PCIe devices?

In the UEFI specification, the PCI system structure is abstracted. The PCI architecture of a typical desktop system is shown in the figure:



7-1 单 PCI Root Bridge 的桌面系

A general desktop system has only one PCI Host Bus, which is used to complete the data exchange between the CPU and PCI devices. There is also generally only one PCI Root Bridge, which manages a local bus and hangs a PCI bus tree under it. The PCI devices we want to access are hung on this bus tree, and they belong to the same bus space. As shown below:

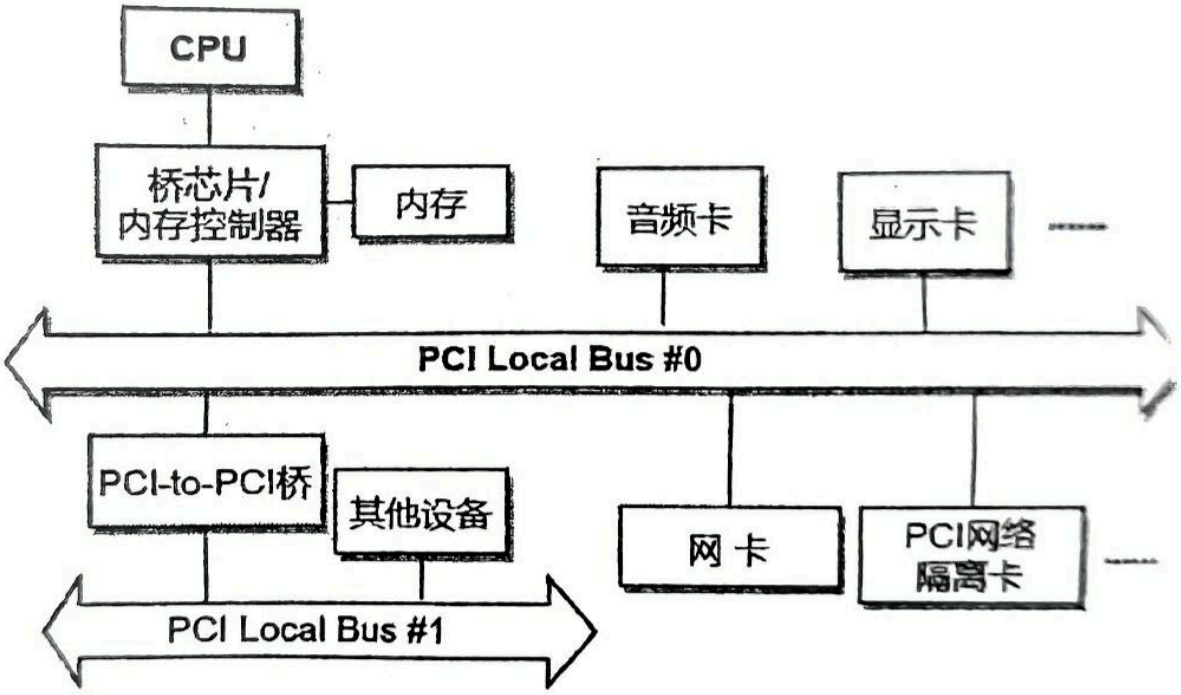


图 7-2　PCI 总线树

The PCI bus tree contains PCI buses, PCI bridges, and PCI devices. The system encodes through three-segment encoding, namely, Bus Number, Device Number, and Function. This encoding is generally referred to as BDF code. The BDF code is determined during the PCI bus scanning and enumeration process of the BIOS and can be used as an index to find PCI devices.

After finding a PCI device, how do you determine if this device is the one you are looking for? Each PCI device, except for the main bus bridge, implements a configuration space (PCIe configuration space), which contains the Vendor ID and Device ID used by the device manufacturer to identify itself. By comparing the Vendor ID and Device ID of the PCI device, you can determine whether the device you are looking for is the target device.

Taking the X86 platform as an example, the PCI device can be accessed in the form of BDF code through the CONFG_ADDR register (0xCF8) and the CONFG_DATA register (0xCFC) to obtain the configuration space of the device.

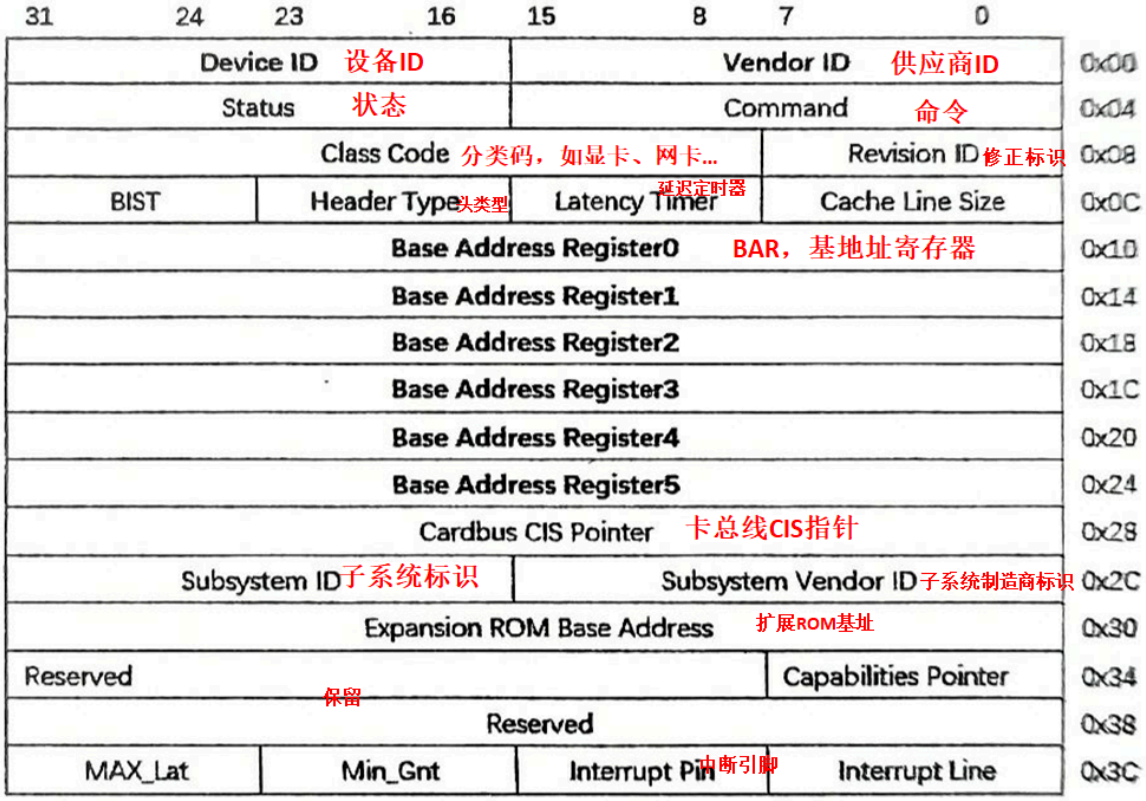


图 7-3　PCI 设备的配置空间

The basic configuration space of PCI devices consists of 64 bytes, with an address range of 0x00~0x3F, which is mainly used to identify devices and define how the host accesses PCI cards. It also contains 6 base address registers, which are called BARs. They store the base address of the address space used by PCI devices, that is, the address of the device in the PCI bus domain. Each device has up to 6 base address spaces, but not all of them are used.

BAR can address IO address space or memory address space. Its lowest bit is read-only bit, which shows which address space can be accessed.

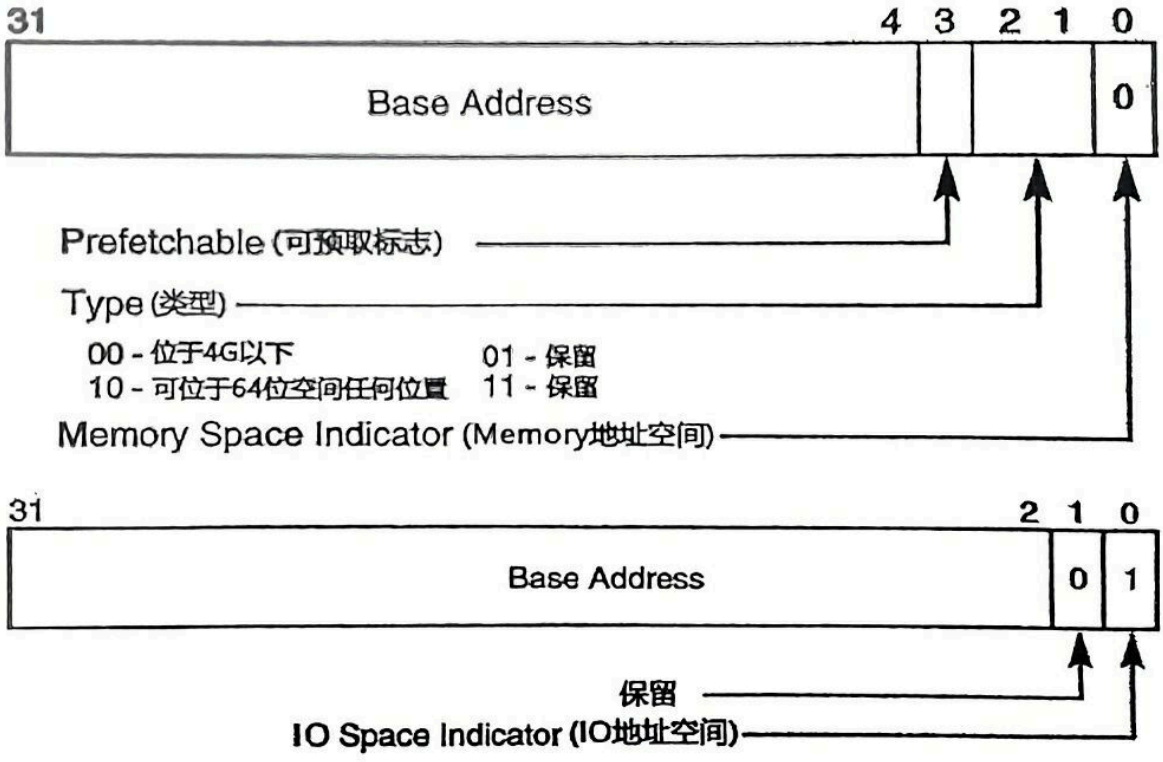


图 7-4　基地址寄存器的位分配

2.1.2 How to access registers and other resources in PCI devices?

The location of various registers or other resources in the PCIe device can be obtained through the BAR register and the offset address of the internal register relative to the BAR. Instructions for using the internal resources will be provided in the chip manual.