[UEFI Practice] SlimBootloader Usage



The summary is generated in C Know , supported by DeepSeek-R1 full version, go to experience>

illustrate

The basic contents of Slim Bootloader have been introduced in [UEFI Practice] Slim Bootloader Introduction, but because it is a long time ago, many contents have expired and cannot be used, so here is an updated version

Brief description

Intel® Slim Bootloader, referred to as Intel® SBL (hereinafter referred to as SBL), is a bootloader launched by Intel. A complete introduction to it can be found at the following website:

https://www.intel.com/content/www/us/en/design/products-and-solutions/technologies/slim-bootloader/overview.html . It can be considered as the Intel version of coreboot, which is more inclined to the x86 platform in terms of platform support, security, and scalability. Its features are as follows:



Fast

Optimized for systems with a critical reliance on boot speed.



Small

Small footprint means lower flash sizes requirements, reducing overall BOM cost. Allows fully redundant images for resilient solutions.



Customizable

Designed with modularity in mind, allowing for easy addition of differentiating



Secure

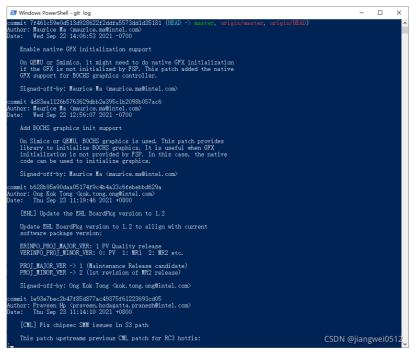
Supports verified boot, measured boot, and secure firmware updates. Build secure boot solutions when paired with Intel® Platform Protection Technology with Boot Guard. CSDN @jiangwei0512

It supports various common operating systems and is open source (using BSD license).

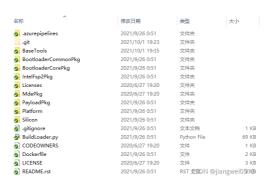
Source code download

 $The source code of SBL can be downloaded from \ https://github.com/slimbootloader/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . There is also a mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . The mirror on Gitee at \ https://gitee.com/jiangwei0512/slimbootloader . Th$

Since the SBL version is constantly evolving, the code may differ due to updates. Please refer to the actual downloaded code. The current version is:



The downloaded source code directory structure is as follows:



The following is a brief description of the main files or directories:

File or Directory	illustrate		
BaseTools	The actual tool used to generate the SBL binary is a part of the tools located in BootloaderCorePkglTools.		
BootloaderCommonPkg	Contains common library functions for use by SBL.		
BootloaderCorePkg	SBL divides the startup into several different stages, and their main codes are included in this directory: Stage1A: The initial stage, spanning from the Reset Vector to the setting of Case As RAM (CAR), it will call FSP-T; Stage1B: From the setting of CAR to the completion of memory initialization, it will call FSP-M; Stage2: Perform other platform initialization (CPU and Chipset-related initialization outside of memory), and jump to Payload, it will call FSP-S.		
IntelFsp2Pkg	FSP support package.		
MdePkg	EDKII universal code.		
PayloadPkg	Contains code for loading OS and upgrading firmware.		
Platform	The code supported by the platform.		
Silicon	SoC support code.		
BuildLoader.py	Generates the script used by the Slim Bootloader binary, which will set up the build chain, precompile, compile, and other operations after the build is completed.		

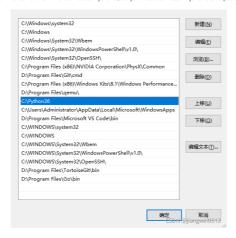
The code organization logic of SBL is to maintain the independence and scalability of the modules. The following requirements must be guaranteed:

- 1. BootloaderCorePkg and PayloadPkg should be independent and unrelated to each other;
- 2. PayloadPkg code should not depend on Platform or Silicon;
- 3. PayloadPkg should only depend on BootloaderCommonPkg

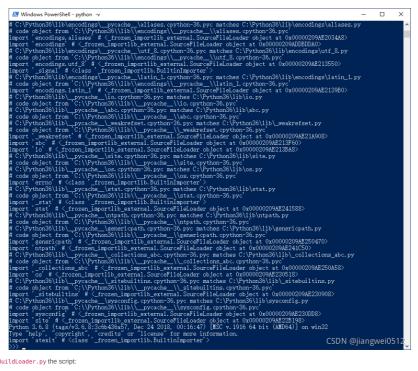
Building the SBL binary

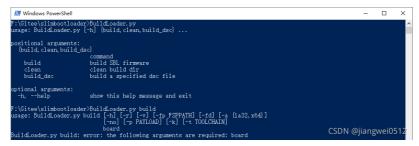
Windows 10 is used here to build SBL. Usually, the binary generated by compiling under Windows is smaller than that using GCC. For Intel platforms, UEFI development under Windows is more common, which is why Windows is used.

SBL uses Python scripts BuildLoader.py to complete the entire build process. The current SBL version uses Python3, so you need to install Python3 and put the execution path in the environment variable:



The version information is as follows (Ctrl+z + Enter exit Python interface):





The command used to build the SBL binary is (no XXX is specified in the above figure, so an error is reported):

BuildLoader.py The dependent tools and their version information will be checked, so the whole picture is very important. The above tools need to be installed in the current Windows environment. Because this machine was used for UEFI development before, most of the tools are available, but the versions of openssl, iasl and Visual Studio do not meet the requirements. The latest version of openssl can be downloaded from https://sourceforge.net/projects/openssl-tor-windows/, and the latest version of iasl can be downloaded from https://www.acpica.org/downloads/binary-tools. Visual Studio needs to use version 2015 or above. Here, the 2019 version is selected. You can download it from the official website and install it online. It should be noted that you need to select the following content during installation:



Here we can ensure that the tools required for SBL compilation (such as cl.exe, etc.) can be installed correctly. Execute the compilation command again, and the results are as follows

```
| E. Windows PowerShell | Coheckins Tool Chair Nations | Coheckins Tool Chair Varions | Cohec
```

You can see that the tool detection has passed, but it will still report an error in the end:

```
cl.exa -c /nologo /2i /c /02 /MT /W4 /WX /D CRT_SECURE_ND_DEPRECATE /D CRT_NONSTEC_ND_DEPRECATE -I . -I F:\Gi tee\slinbootloader\BaseTools\Source\C\Common Sdk\C\LzmaEnc.c -FoSdk\C\LzmaEnc.c b]

tee\slinbootloader\BaseTools\Source\C\Common Sdk\C\LzmaEnc.c -FoSdk\C\LzmaEnc.c b]

cl.exe -c /nologo /Zi /c /02 /MT /W4 /WX /D _CRT_SECURE_ND_DEPRECATE /D _CRT_NONSTEC_ND_DEPRECATE -I . -I F:\Gi tee\slinbootloader\BaseTools\Source\C\Common Sdk\C\LzmaEnc.c b]

tee\slinbootloader\BaseTools\Source\C\Common Sdk\C\LzmaEnc.c b]

cl.exe -c /nologo /Zi /c /02 /MT /W4 /WX /D _CRT_SECURE_ND_DEPRECATE /D _CRT_NONSTEC_ND_DEPRECATE -I . -I F:\Gi tee\slinbootloader\BaseTools\Source\C\Common Sdk\C\LzmaEnc.c b)

cl.exe -c /nologo /Zi /c /02 /MT /W4 /WX /D _CRT_SECURE_ND_DEPRECATE /D _CRT_NONSTEC_ND_DEPRECATE -I . -I F:\Gi tee\slinbootloader\BaseTools\Source\C\Common Sdk\C\Fz$tream.c b]

cl.exe -c /nologo /Zi /c /02 /MT /W4 /WX /D _CRT_SECURE_ND_DEPRECATE /D _CRT_NONSTEC_ND_DEPRECATE -I . -I F:\Gi tee\slinbootloader\BaseTools\Source\C\Common Sdk\C\Fz$tream.c b]

cl.exe -c /nologo /Zi /c /02 /MT /W4 /WX /D _CRT_SECURE_ND_DEPRECATE /D _CRT_NONSTEC_ND_DEPRECATE -I . -I F:\Gi tee\slinbootloader\BaseTools\Source\C\Common Sdk\C\Bra86.c -FoSdk\C\Bra86.c of FoSdk\C\Bra86.c of FoSd
```

The previous content is to build the compilation tool in BaseTools. You can see that it is completed. There is another step to generate the key before building the SBL binary. The command used is:

1 | F:\Gitee\slimbootloader>BootloaderCorePkg\Tools\GenerateKeys.py -k ..\SblKeys

The main reason is that the directory where the command is executed is specifically stated here. The reason is that SBL will place the key at the same level of the directory where it is located by default. The corresponding directory name is SblKeys by default. After executing the command, the following key is generated:

名称	修改日期	类型	大小
ConfigTestKey_Priv_RSA2048.pem	2021/10/1 22:29	PEM 文件	2 KB
ConfigTestKey_Priv_RSA3072.pem	2021/10/1 22:29	PEM 文件	3 KB
ContainerCompTestKey_Priv_RSA204	2021/10/1 22:29	PEM 文件	2 KB
ContainerCompTestKey_Priv_RSA307	2021/10/1 22:29	PEM 文件	3 KB
ContainerTestKey_Priv_RSA2048.pem	2021/10/1 22:29	PEM 文件	2 KB
ContainerTestKey_Priv_RSA3072.pem	2021/10/1 22:29	PEM 文件	3 KB
FirmwareUpdateTestKey_Priv_RSA204	2021/10/1 22:29	PEM 文件	2 KB
FirmwareUpdateTestKey_Priv_RSA307	2021/10/1 22:29	PEM 文件	3 KB
MasterTestKey_Priv_RSA2048.pem	2021/10/1 22:29	PEM 文件	2 KB
MasterTestKey_Priv_RSA3072.pem	2021/10/1 22:29	PEM 文件	3 KB
OS1_TestKey_Priv_RSA2048.pem	2021/10/1 22:29	PEM 文件	2 KB
OS1_TestKey_Priv_RSA3072.pem	2021/10/1 22:29	PEM 文件	3 KB
OS1_TestKey_Pub_RSA2048.pem	2021/10/1 22:29	PEM 文件	1 KB
OS1 TestKey Pub RSA3072.nem	2021/10/1 22:29	PEM EADN @	iiangwei05/k2

After the key is generated, you also need to generate FSP. Since the SBL binary for QEMU is built here, you need to generate FSP for QEMU. The details of FSP will not be explained here. For how to generate FSP, you can download https://gitee.com/jiangwei0512/edk2-beni , and then generate FSP through the BuildFsp.py script. The generated content is as follows:

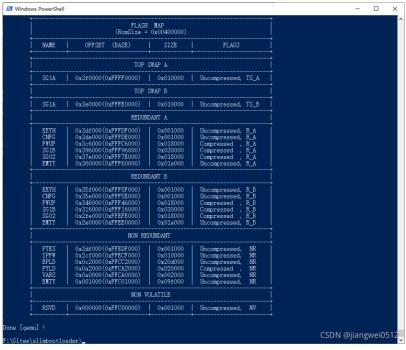
名称	修改日期	类型	大小
Fsp.bsf	2021/11/4 0:42	BSF 文件	5 KB
FspmUpd.h	2021/11/4 0:42	VisualStudio.h.1	4 KB
🛄 FspRel.bin	2021/11/4 0:42	BIN 文件	232 KB
FspsUpd.h	2021/11/4 0:42	VisualStudio.h.1	4 KB
FsptUpd.h	2021/11/4 0:42	VisualStudio.h.1	3 KB
FspUpd.h	2021/11/4 0:42	VisualStudio.h.1	2 KB

After that, you need to put the generated content into the SBL directory. The specific directory is as follows



Put the header file in the Include directory (if there is already a file with the same name, just overwrite it), and put Fsp.bsf and FspRel.bin in the FspBin directory

This completes the setup of the FSP binary, and then executes the previous build command to successfully complete the build:



The generated binary is Build\BootloaderCorePkg\DEBUG_VS2019\FV located at SlimBootloader.bin

49

Found Config TAG: 0x200 @ 0x0000ECDC

Because the SBL binary is built for QEMU, if you want to use it, you can directly start it through the QEMU command. Of course, QEMU needs to be installed separately, which can be downloaded from https://www.qemu.org/download/ The command to use is as follows:

登录复制 Al generated projects 1 | gemu-system-x86 64 -machine q35 -nographic -serial mon:stdio -pflash Build\BootloaderCorePkq\DEBUG VS2019\FV\SlimBootloader.bin

```
Here are the execution results:
                                                                                                                                                                                                                            Al generated projects
                                                                                                                                                                                                                                                         登录复制
        F:\Gitee\slimbootloader>qemu-system-x86_64 -machine q35 -nographic -serial mon:stdio -pflash Build\BootloaderCorePkg\DEBUG_V52019\FV\SlimBootloader.bin
        WARNING: Image format was not specified for 'Build\BootloaderCorePko\DEBUG VS2019\FV\SlimBootloader.bin' and probing guessed raw
                    Automatically detecting the format is dangerous for raw images, write operations on block \theta will be restricted.
                    Specify the 'raw' format explicitly to remove the restrictions.
                         = Intel Slim Bootloader STAGE1A ==
        SBID: SB OEMU
        ISVN: 001
IVER: 001.000.001.001.03646
   10
         SVER: 7F461C59E0D513D9
         FDBG: BLD(D IA32) FSP(R)
   12
        FSPV: ID($0EMFSP$) REV(00001000)
         Loader global data @ 0x00001C38
        Run STAGE1A @ 0x00070000
Load STAGE1B @ 0x00040000
   14
   15
16
         HASH verification for usage (0x00000001) with Hash Alg (0x2): Success
   17
                      ==== Intel Slim Bootloader STAGE1B =
        Host Bridge Device ID:0x29C0
   19
 20 Board ID:0x1 - Loading QEMU!
twen QEMU Flash: Attempting flash detection at FFC00000
 twen QemuFlashDetected => FD behaves as FLASH twen QemuFlashDetected => Yes
 twen SpiInstance = 0000E470
        Spiinstance = 0000047/0
Variable region: 0xFFCA0000:0x2000
SPI WRITE: FFCA0010 00000004
SPI WRITE: FFCA0011 00000001
SPI WRITE: FFCA0014 00000008
   25
   26
   27
   29
           SPI WRITE: FFCA001C 00000004
           SPI WRITE: FFCA0011 00000001
   31
         Loading Component KEYH: HS
        Registering container KEYH
HASH verification for usage (0x00000100) with Hash Alg (0x2): Success
   32
        SignType (0x2) SignSize (0x180) SignHashAlg (0x2)
RSA verification for usage (0x00000100): Success
HASH verification for usage (0x00000000) with Hash Alg (0x2): Success
   34
   36
        Append public key hash into store: Success
Load EXT CFG Data @ 0x0000EB54:0x0158 ... Success
   37
   38
        HASH verification for usage (0x00000200) with Hash Alg (0x2): Success SignType (0x2) SignSize (0x180) SignHashAlg (0x2)
   39
   41
        RSA verification for usage (0x00000200): Success
        BOOT: BPO
MODE: 0
   42
   43
   44
        BoardID: 0x01
        PlatformName: QEMU_01
   46
        Memory Init
        Found Config TAG: 0x180 @ 0x0000ECCC

MemCfg.Test1=11223344, MemCfg.Test2=11223346
   48
```

```
SilCfg.Test1=11223347, SilCfg.Test2=04030201
      Call FspMemoryInit ... Success
Loader global data @ 0x06EBFD70
 51
 53
      Load page table from memory @ 0x06B74000
 54
55
       Remapping Stage to 0x06B77000
FSP Resource HOB Range
                                                Type
                                                              0wner
 56
      58
 60
      000000006F00000-000000007000000 05 69A79759-1373-4367-A6C4-C7F59EFD986E
 61
      000000007000000-0000000008000000 05 D038747C-D00C-4980-B319-490199A47D55
 62
 63
      Switch to memory stack @ 0x06EEEE00
      Stage1 stack: 0x2000 (0xF28 used)
 65
      Stage1 heap: 0xE000 (0x1F14 used)
      Call FspTempRamExit ... Success
Memory FSP @ 0x06F00000
      Memory TOP @ 0x06B74000
Loading Component FLMP:SG02
 68
      HASH verification for usage (0x00000002) with Hash Alg (0x2): Success
 70
      Loaded STAGE2 @ 0x06E55000
 72
 73
                    === Intel Slim Bootloader STAGE2 =======
      Unmapping Stage
 75
      Board GPIO Init
      Get base platform GPIO table from board ID \boldsymbol{\theta}
      Programming 7 GPIO entries
      GPIO GPP_A00 DATA: 0x00000000 0x00000010
GPIO GPP_A02 DATA: 0x80000002 0x00000012
 78
 79
      GPIO GPP_A03 DATA: 0xC0000003 0x00000013
GPIO GPP_A04 DATA: 0xC1000004 0x0000014
GPIO GPP_A05 DATA: 0x41000005 0x00000015
 86
 82
      GPIO GPP_A06 DATA: 0x81000006 0x00000016
GPIO GPP_A07 DATA: 0xC1000007 0x00000017
 83
 84
      Test variable services
SPI WRITE: FFCA0020 00000004
SPI WRITE: FFCA0021 00000001
 85
 87
 88
         SPI WRITE: FFCA0024 00000008
SPI WRITE: FFCA002C 00000004
 89
         SPI WRITE: FFCA0011 00000001
SPI WRITE: FFCA0021 00000001
 96
 92
         SPT WRITE: FECA0011 00000001
 93
       Loading Component IPFW:TST3
 94
      Registering container IPFW
      HASH verification for usage (0x00001000) with Hash Alg (0x2): Success SignType (0x2) SignSize (0x180) SignHashAlg (0x2)
 95
      RSA verification for usage (0x00001000): Success
HASH verification for usage (0x00000000) with Hash Alg (0x2): Success
 97
 99
      SignType (0x2) SignSize (0x180) SignHashAlg (0x2)
100
101
      RSA verification for usage (0x00000000): Success
Load IP firmware @ 0:0x0 - Bad Buffer Size
      Silicon Init
Select VBT ImageId 0x00000001
102
104
      Call FspSiliconInit ...
105
106
      Graphics Info: 800 x 600 x 32 @ 0x80000000
107
108
      109
      MEM: 0000000000100000 0000000006A00000 00 1
      MEM: 000000006B00000 0000000000004000 01 2
MEM: 000000006B04000 0000000000068000 00 3
111
112
113
      MEM: 0000000006B6C000 00000000000008000 00 4
      MEM: 000000006B74000 00000000038C000 00 2
114
      MEM: 0000000006F00000 0000000000100000 00 2
      MEM: 0000000007000000 000000001000000 00 2
MEM: 00000000FC00000 000000000400000 00 2
116
117
118
      MP Init (Wakeup)
MP Init (Run)
119
      Detected 1 CPU threads
120
121
      CPU 0 APIC ID: 0
SMM rebase done on 1 CPUs
      PCI Enum
Call FspNotifyPhase(20) ... Success
122
123
      ACPI Init
Publish ACPI table: FACP
Publish ACPI table: HPET
Publish ACPI table: APIC
124
125
126
127
      Publish ACPI table: MCFG
128
      Publish ACPI table: FPDT
Publish ACPI table: BGRT
129
136
131
      Publish ACPT table: TEST
132
      ACPI Ret: Success
133
      Enable SMRR
      Loading Payload ID PYLD
Loading Component FLMP:PYLD
134
135
136
      HASH verification for usage (0x00000004) with Hash Alg (0x2): Success Load Payload ID 0x00000000 @ 0x06CB7000
138
      PE32 Format Payload
      HOB @ 0x06EC0000
Created 4 OS boot options (Current: 0)
139
140
141
      Stage2 stack: 0x40000 (stack used 0x9CC, HOB used 0xFB0, 0x3E684 free) Stage2 heap: 0x34C000 (0x209000 used, 0x143000 free)
143
      Pavload entry: 0x06CB7260
144
145
       Jump to payload
146
147
      Payload startup
148
      ACPI PmTimer Base: 0x408
      PCI Express Base: 0xE0000000
156
151
152
                   -----0s Loader-----
153
155
      Press any key within 1 second(s) to enter the command shell
156
      Boot options (in HEX):
157
158
      Idx|ImqType|DevType|DevNum|Flags|HwPart|FsType|SwPart|File/Lbaoffset
                                   0 | 0 | 0 | AUTO | 0 | iasimage.bin
0 | 0 | FF | AUTO | 0 | iasimage.bin
                  0| SD |
0| SATA |
160
         11
161
162
                        NVME
                                                     0 | AUTO
                                                    0 | AUTO |
         3|
                  0 |
                        USB
                                                                      0 | iasimage.bin
163
165
      ===== Try Booting with Boot Option 0 ====
```

```
166 | BootMediumPciBase(0x300)
          Getting boot image from SD
MMC global data init
167
168
169
          Use SDMA instead of ADMA2
170
171
          MMC Phase 1 init
SdMmcHcReset: reset done with Time out
         SoMmcHcReset: reset done with lime out
SoMmcHcReset Fail Status = 0x80000012
Failed to init media - Time out
Failed to Initialize Boot Device - Type 1, Instance 0
Payload normal heap: 0x2000000 (0x8000 used)
172
173
174
175
176
          Payload reserved heap: 0x4000 (0x0 used)
Payload stack: 0x10000 (0x4D4 used)
177
178
179
180
                       === Try Booting with Boot Option 1 ======
 181
          BootMediumPciBase(0x1F02)
          Getting boot image from SATA
Init AHCI controller E00FA000
182
          AHCI port [2] has a [cdrom]
Try to find boot partition
184
185
186
          AhciDeviceRead Status = Device Error
Partition type: UNKNOWN (1 logical partitions)
Find partition success
187
188
          Find partition success
Init File system
AhciDeviceRead Status = Device Error
AhciDeviceRead Status = Device Error
No partitions found, Status = Device Error
Failed to Initialize Boot File System - SwPart 0
189
 191
192
193
          Payload normal heap: 0x2000000 (0x10F000 used)
Payload reserved heap: 0x4000 (0x0 used)
Payload stack: 0x10000 (0x664 used)
194
 195
196
197
198
          Deinit AHCI controller 0
199
200
201
           Not a AHCI controller or Disabled
          ======= Try Booting with Boot Option 2 =======
BootMediumPciBase(0x300)
Getting boot image from NVME
202
204
205
           NvmExpressDriverBindingStart: start
           NymeControllerInit: the controller doesn't support NVMe command set
          NVmeLontrollerinit: the controller doesn't support NVP
NVmeExpresspriverBindingStart: end with Unsupported
Failed to init media - Unsupported
Failed to Initialize Boot Device - Type 6, Instance 0
Payload normal heap: 0x2000000 (0x10F000 used)
Payload reserved heap: 0x4000 (0x0 used)
Payload stack: 0x10000 (0x664 used)
206
207
208
209
210
211
212
213
214
215
           ====== Try Booting with Boot Option 3 =====
          BootMediumPciBase(0x400)
          Getting boot image from USB
Failed to initialize USB bus !
216
         Failed to initialize Usa Dus!
Failed to init media - Unsupported
Failed to Initialize Boot Device - Type 5, Instance 0
Payload normal heap: 0x20000000 (0x10F000 used)
Payload reserved heap: 0x40000 (0x604 used)
Payload stack: 0x10000 (0x664 used)
218
219
220
221
223
224
225 Shell>
```

收起 へ

Finally entered the UEFI Shell.

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