

UEFI - Accessing PCI/PCIE devices (Part 2)

原创

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1. Protocol that supports access to PCI/ PCIE devices

UEFI provides two main modules to support PCI bus, one is PCI Host Bridge controller driver, the other is PCI bus driver. These two modules are bound to specific platform hardware. Under this mechanism, the differences between different CPU architectures are shielded, providing software developers with a relatively consistent Protocol interface.

The UEFI standard provides two types of protocols for accessing PCI/PCIE devices: **EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL** and **EFI_PCI_IO_PROTOCOL**. The former provides an abstract IO function for the PCI root bridge, which is generated by the PCI Host Bus Controller (PCI main bus driver) and is generally used by the PCI/PCle bus driver to enumerate devices, obtain Option ROM, allocate PCI device resources, etc.; the latter is generated by the PCI/PCIE bus driver for PCI/PCIE devices, and is generally used by PCI/PCIE device drivers to access the IO space, memory space, and configuration space of PCI/PCIE devices.

1.1 EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL

EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL provides basic memory, input/output (I/O), PCI configuration, and direct memory access interfaces that are used to abstract access to the PCI root bridge controller behind the PCI controller.

```
typedef struct _EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL;
```

```
1  /// Provides the basic Memory, I/O, PCI configuration, and DMA interfaces that are
2  /// used to abstract accesses to PCI controllers behind a PCI Root Bridge Controller.
3  ///提供了基本内存, I/O, PCI配置和直接内存访问 (DMA) 接口, 这些接口用于抽象PCI控制器后PCI根桥的访问
4  struct _EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL {
5      ///
```

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```

6 |   /// The EFI_HANDLE of the PCI Host Bridge of which this PCI Root Bridge is a member. 7 |
   |   /// 这是PCI根桥所属的PCI主机桥的EFI_HANDLE 8 |
   |   EFI_HANDLE                                RootHandle; //包含这个PCT根桥的PCT主机桥的Handle
                                     展开 ∨

```

Here we only introduce the interface Mem for accessing memory, the interface Io for accessing I/O space, and the interface Pci for accessing PCI configuration space. The parameter types of these three interfaces are the same, all of which are EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL_ACCESS

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```

1 | typedef struct {
2 |
3 |   /// Read PCI controller registers in the PCI root bridge memory space.
4 |   /// 读数据
5 |   EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL_IO_MEM    Read;
6 |
7 |   /// Write PCI controller registers in the PCI root bridge memory space.
8 |   /// 写数据
9 |   EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL_IO_MEM    Write;
10 | } EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL_ACCESS;
11 |
12 | typedef
13 | EFI_STATUS
14 | (EFIAPI *EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL)(
15 |     IN EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL    *This, //指向protocol实例
16 |     IN     EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL_WIDTH Width, //标识内存操作的宽度，一般有8位、16位、32位、64位几种
17 |     IN     UINT64 Address, //内存操作的基地址
18 |     IN     UINTN Count, //读写的数据个数，以width为单位
19 |     IN OUT VOID *Buffer
20 | );

```

收起 ^

The parameter Address is different when accessing I/O space, memory space, and configuration space.


For the configuration space, Address is determined by the BDF address and Register offset, and the macro EFI_PCI_ADDR Register offset. In EDK2, the macro definition is as follows:

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```

1 #define EFI_PCI_ADDRESS(bus, dev, func, reg) \
2   (UINT64) ( \
3     (((UINTN) bus) << 24) | \
4     (((UINTN) dev) << 16) | \
5     (((UINTN) func) << 8) | \
6     (((UINTN) (reg)) < 256 ? ((UINTN) (reg)) : (UINT64) (LShiftU64 ((UINT64) (reg), 32))))

```

For IO space, the parameter Address refers to the IO address of the PCI device IO space;

For the Memory space, the parameter Address refers to the Memory address of the PCI device Memory space.

They are determined by BAR and offset.

1.2 EFI_PCI_IO_PROTOCOL

In PCI/PCIE device drivers, EFI_PCI_IO_PROTOCOL is generally used to access the internal resources of the device. The Protocol is mounted on the PCI/PCIE controller and runs in the EFI boot environment to access the memory space and I/O space of the PCI/PCIE device.

```

1 /// Global ID for the PCI I/O Protocol
2 ///
3 #define EFI_PCI_IO_PROTOCOL_GUID \
4   { \
5     0x4cf5b200, 0x68b8, 0x4ca5, {0x9e, 0xec, 0xb2, 0x3e, 0x3f, 0x50, 0x2, 0x9a } \
6   }
7
8 typedef struct _EFI_PCI_IO_PROTOCOL EFI_PCI_IO_PROTOCOL;

```

The interface of EFI_PCI_IO_PROTOCOL is as follows:

```

1 ///
2 /// The EFI_PCI_IO_PROTOCOL provides the basic Memory, I/O, PCI configuration,
3 /// and DMA interfaces used to abstract accesses to PCI controllers.
4 /// There is one EFI_PCI_IO_PROTOCOL instance for each PCI controller on a PCI bus.
5 /// A device driver that wishes to manage a PCI controller in a system will have to


```

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```

6  |  /// retrieve the EFI_PCI_IO_PROTOCOL instance that is associated with the PCI controller.
7  |  ///
8  struct _EFI_PCI_IO_PROTOCOL {
9      EFI_PCI_IO_PROTOCOL_POLL_IO_MEM      PollMem;
10     EFI_PCI_IO_PROTOCOL_POLL_IO_MEM      PollIo;
11     EFI_PCI_IO_PROTOCOL_ACCESS            Mem;
12     EFI_PCI_IO_PROTOCOL_ACCESS            Io;
13     EFI_PCI_IO_PROTOCOL_CONFIG_ACCESS     Pci;
14     EFI_PCI_IO_PROTOCOL_COPY_MEM          CopyMem;
15     EFI_PCI_IO_PROTOCOL_MAP               Map;
16     EFI_PCI_IO_PROTOCOL_UNMAP             Unmap;
17     EFI_PCI_IO_PROTOCOL_ALLOCATE_BUFFER   AllocateBuffer;
18     EFI_PCI_IO_PROTOCOL_FREE_BUFFER       FreeBuffer;
19     EFI_PCI_IO_PROTOCOL_FLUSH             Flush;
20     EFI_PCI_IO_PROTOCOL_GET_LOCATION       GetLocation;
21     EFI_PCI_IO_PROTOCOL_ATTRIBUTES         Attributes;
22     EFI_PCI_IO_PROTOCOL_GET_BAR_ATTRIBUTES GetBarAttributes;
23     EFI_PCI_IO_PROTOCOL_SET_BAR_ATTRIBUTES SetBarAttributes;
24
25     ///
26     /// The size, in bytes, of the ROM image.
27     ///
28     UINT64 RomSize;
29
30     ///
31     /// A pointer to the in memory copy of the ROM image. The PCI Bus Driver is responsible
32     /// for allocating memory for the ROM image, and copying the contents of the ROM to memory.
33     /// The contents of this buffer are either from the PCI option ROM that can be accessed
34     /// through the ROM BAR of the PCI controller, or it is from a platform-specific location.
35     /// The Attributes() function can be used to determine from which of these two sources
36     /// the RomImage buffer was initialized.
37     ///
38     VOID      *RomImage;
39 };

```

收起 ^


【Note!!!】 It should be noted here that there is only one instance of EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL in most office global pointer variable gPCIRootBridgeIO; while there are multiple instances of EFI_PCI_IO_PROTOCOL, generally there are :

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so the global pointer array gPCIIOArray[256] is used to store these instances.

2. Simple implementation of accessing PCI/PCIE devices

2.1 EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL traverses PCI devices

When using EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL to obtain PCI/PCIE devices, you first need to obtain all handles of EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL. You can use the gBS->LocateHandleBuffer() function to obtain the handle. After obtaining the handle, use the gBS->HandleProtocol() function to obtain the protocol instance, and then you can call the function interface in it. Use BDF to find a device and read the device's configuration space.

The configuration space of the PCI device is represented by the structure PCI_TYPE00, and its code prototype is:

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```
1  /// PCI Device Configuration Space
2
3  typedef struct {
4      PCI_DEVICE_INDEPENDENT_REGION    Hdr;
5      PCI_DEVICE_HEADER_TYPE_REGION    Device;
6  } PCI_TYPE00;
```

Hdr represents the general header area of the PCI configuration space, which includes the following fields:

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```
1  // Common header region in PCI Configuration Space
2
3  typedef struct {
4      UINT16    VendorId;
5      UINT16    DeviceId;
6      UINT16    Command;
7      UINT16    Status;
8      UINT8     RevisionID;
9      UINT8     ClassCode[3];
10     UINT8     CacheLineSize;
11     UINT8     LatencyTimer;
12     UINT8     HeaderType;
13     UINT8     BIST;
14 } PCI_DEVICE_INDEPENDENT_REGION;
```

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Device represents the header area in the PCI device configuration space

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```
1  /// PCI Device header region in PCI Configuration Space
2
3  typedef struct {
4      UINT32    Bar[6];
5      UINT32    CISPtr;
6      UINT16    SubsystemVendorID;
7      UINT16    SubsystemID;
8      UINT32    ExpansionRomBar;
9      UINT8     CapabilityPtr;
10     UINT8     Reserved1[3];
11     UINT32    Reserved2;
12     UINT8     InterruptLine;
13     UINT8     InterruptPin;
14     UINT8     MinGnt;
15     UINT8     MaxLat;
16 } PCI_DEVICE_HEADER_TYPE_REGION;
```

收起 ^

Simple implementation of application using EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL to access PCIe devices:

Write the MyPCIEProtocol.c code:


```
1  #include <Uefi.h>
2  #include <Library/UefiBootServicesTableLib.h>
3  #include <Library/ShellCEntryLib.h>
4  #include <Library/DebugLib.h>
5
6  #include <Protocol/PciIo.h>
7  #include <Protocol/PciRootBridgeIo.h>
8  #include <IndustryStandard/Pci.h>
```

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```


9 |
10 |
11 | EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL *gPciRootBridgeIo; //创建一个EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL类型的指针变量
12 |
13 | EFI_STATUS LocatePciRootBridgeIo(void); //函数声明, 告诉编译器函数名称、返回值类型、参数类型; 如果函数定义在函数调用之后, 那么在函数调用之前必须进行函数声明
14 |
15 | //函数声明
16 | EFI_STATUS PciDevicePresent(
17 |     IN EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL * PciRootBridgeIo,
18 |     OUT PCI_TYPE00 * Pci,
19 |     IN UINT8 Bus,
20 |     IN UINT8 Device,
21 |     IN UINT8 Func
22 | );
23 |
24 | EFI_STATUS ListPciInformation(void); //函数声明
25 |
26 |
27 | EFI_STATUS
28 | EFIAPI
29 | UefiMain (
30 |     IN EFI_HANDLE ImageHandle,
31 |     IN EFI_SYSTEM_TABLE *SystemTable
32 | )
33 | {
34 |     EFI_STATUS Status;
35 |
36 |
37 |     Status = LocatePciRootBridgeIo(); //调用LocatePciRootBridgeIo()函数, 定位根桥
38 |     if(EFI_ERROR(Status))
39 |     {
40 |         DEBUG((DEBUG_ERROR, "[CSDN]Call LocatePciRootBridgeIo failed,Can't find protocol!\n"));
41 |     }
42 |     else
43 |     {
44 |         DEBUG((DEBUG_ERROR, "[CSDN]Call LocatePciRootBridgeIo succeeded,Find protocol!\n"));
45 |     }
46 |
47 |     //列出PCI设备的信息
48 |     ListPciInformation();


```

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```


49 | 50 | return EFI_SUCCESS;
51 | }
52 |
53 | EFI_STATUS LocatePciRootBridgeIo()
54 | {
55 |     EFI_STATUS Status;
56 |     EFI_HANDLE *PciHandleBuffer = NULL;
57 |     UINTN      HandleIndex = 0;
58 |     UINTN      HandleCount = 0;
59 |
60 |     //获取 EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL的所有句柄
61 |     Status = gBS->LocateHandleBuffer(
62 |         ByProtocol, //查找句柄的方式, 这里采用返回指定协议的句柄
63 |         &gEfiPciRootBridgeIoProtocolGuid, //要查找的协议的GUID
64 |         NULL,
65 |         &HandleCount, //输出参数, 缓冲区中返回的句柄数量
66 |         &PciHandleBuffer //输出参数, 指向用于返回支持协议的请求句柄数组的缓冲区的指针。
67 |     );
68 |
69 |     if(EFI_ERROR(Status)) return Status; //如果没成功找到, 直接结束程序
70 |
71 |     //查找支持 EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL句柄的protocol实例
72 |     for(HandleIndex = 0; HandleIndex < HandleCount; HandleIndex++)
73 |     {
74 |         Status = gBS->HandleProtocol(
75 |             PciHandleBuffer[HandleIndex],
76 |             &gEfiPciRootBridgeIoProtocolGuid,
77 |             (VOID **)&gPciRootBridgeIo
78 |         );
79 |         if(EFI_ERROR(Status)) continue; //如果没找到就继续寻找
80 |         else return EFI_SUCCESS; //如果找到了就退出程序
81 |         //这里找到就退出的原因是大部分办公用的个人电脑中就只存在一个EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL
82 |     }
83 |
84 |     return Status;
85 |
86 | }
87 |
88 | EFI_STATUS ListPciInformation()
89 | {


```

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```


90  EFI_STATUS Status = EFI_SUCCESS; g1 |   PCI_TYPE00 Pci; //PCI_TYPE00是一个结构体, 表示PCI的配置空间
92  UINT16 Dev, Func, Bus, PciDevicecount = 0;
93
94  DEBUG((DEBUG_ERROR, "[CSDN] PciDeviceNo\tBus\tDev\tFunc | Vendor.Device.ClassCode\n"));
95  for(Bus=0; Bus<256; Bus++)
96      for(Dev=0; Dev<= PCI_MAX_DEVICE; Dev++)
97          for(Func=0; Func<=PCI_MAX_FUNC; Func++)
98              {
99                  //判断设备是否存在
100                 Status = PciDevicePresent(gPciRootBridgeIo, &Pci, (UINT8)Bus, (UINT8)Dev, (UINT8)Func);
101                 if(Status == EFI_SUCCESS)
102                     {
103                         //如果找到了设备, PCI设备数量加1
104                         PciDevicecount++;
105                         //打印设备信息
106                         DEBUG((DEBUG_ERROR, "[CSDN] %d\t\t%x\t%x\t%x\t", PciDevicecount, (UINT8)Bus, (UINT8)Dev, (UINT8)Func));
107                         DEBUG((DEBUG_ERROR, "%x\t%x\t%x\n", Pci.Hdr.VendorId, Pci.Hdr.DeviceId, Pci.Hdr.ClassCode[0]));
108                     }
109             }
110
111  return EFI_SUCCESS;
112 }
113
114 EFI_STATUS
115 PciDevicePresent (
116     IN  EFI_PCI_ROOT_BRIDGE_IO_PROTOCOL    *PciRootBridgeIo,
117     OUT PCI_TYPE00                          *Pci,
118     IN  UINT8                               Bus,
119     IN  UINT8                               Device,
120     IN  UINT8                               Func
121 )
122 {
123     UINT64      Address;
124     EFI_STATUS  Status;
125
126     //
127     // Create PCI address map in terms of Bus, Device and Func
128     //
129     Address = EFI_PCI_ADDRESS (Bus, Device, Func, 0);
130

```

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```





131 //132 | // Read the Vendor ID register
133 //
134 Status = PciRootBridgeIo->Pci.Read (
135         PciRootBridgeIo,
136         EfiPciWidthUint32,
137         Address,
138         1,
139         Pci
140         );
141
142 if (!EFI_ERROR (Status) && (Pci->Hdr).VendorId != 0xffff) { //0xffff通常标识一个无效的, 未分配的VendorId,如果能读取设备信息就进行打印。
143     //
144     // Read the entire config header for the device
145     //
146     Status = PciRootBridgeIo->Pci.Read (
147         PciRootBridgeIo,
148         EfiPciWidthUint32,
149         Address,
150         sizeof (PCI_TYPE00) / sizeof (UINT32),
151         Pci
152         );
153
154     return EFI_SUCCESS;
155 }
156
157 return EFI_NOT_FOUND;
158 }

```

收起 ^

Write an INF file and run it. The result is:

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```

InstallProtocolInterface: 752F3136-4E16-4FDC-A22A-E5F46812F4CA FE6D828
[CSDN]Call LocatePciRootBridgeIo succeeded,Find protocol!
[CSDN] PciDeviceNo      Bus    Dev    Func | Vendor.Device.ClassCode
[CSDN] 1                0      0      0   | 8086 1237 0
[CSDN] 2                0      1      0   | 8086 7000 0
[CSDN] 3                0      1      1   | 8086 7010 80
[CSDN] 4                0      1      2   | 8086 7020 0
[CSDN] 5                0      1      3   | 8086 7113 0
[CSDN] 6                0      2      0   | 1234 1111 0
FSOpen: Open '\\' Success
FS0:\>

```

CSDN @修行者xkl

2.2 EFI_PCI_IO_PROTOCOL traverses PCI devices

It is relatively simple to traverse the device using EFI_PCI_IO_PROTOCOL. Therefore, the instance of the Protocol obtained previously is generated for the PCI/PCIE device. In fact, it is equivalent to finding the host device. You only need to print out the device information.

```

1  #include <Uefi.h>
2  #include <Library/UefiBootServicesTableLib.h>
3  #include <Library/ShellCEntryLib.h>
4  #include <Library/DebugLib.h>
5
6  #include <Protocol/PciIo.h>
7  #include <Protocol/PciRootBridgeIo.h>
8  #include <IndustryStandard/Pci.h>
9
10
11  EFI_PCI_IO_PROTOCOL *gPciIoArray[256];
12  UINTN gPciIoCount = 0;
13  EFI_STATUS LocatePciIo(void);
14
15  EFI_STATUS ListPciInformation(void);
16
17
18  EFI_STATUS
19  EFIAPI
20  UefiMain (
21      IN EFI_HANDLE          ImageHandle,
22      IN EFI_SYSTEM_TABLE    *SystemTable
23  )
24  {


```

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```

25 | EFI_STATUS Status;
    | 26 |
27 |
28 | Status = LocatePciIo();
29 | if(EFI_ERROR(Status))
30 | {
31 |     DEBUG((DEBUG_ERROR, "[CSDN]Call LocatePciIo failed,Can't find protocol!\n"));
32 | }
33 | else
34 | {
35 |     DEBUG((DEBUG_ERROR, "[CSDN]Call LocatePciIo succeeded,Find protocol!\n"));
36 | }
37 |
38 | ListPciInformation();
39 |
40 | return EFI_SUCCESS;
41 | }
42 |
43 | EFI_STATUS LocatePciIo()
44 | {
45 |     EFI_STATUS Status;
46 |     EFI_HANDLE *PciHandleBuffer = NULL;
47 |     UINTN      HandleIndex = 0;
48 |     UINTN      HandleCount = 0;
49 |
50 |     Status = gBS->LocateHandleBuffer(
51 |         ByProtocol,
52 |         &gEfiPciIoProtocolGuid,
53 |         NULL,
54 |         &HandleCount,
55 |         &PciHandleBuffer
56 |     );
57 |     if(EFI_ERROR(Status)) return Status;
58 |
59 |     gPciIoCount = HandleCount;
60 |     DEBUG((DEBUG_ERROR, "[CSDN] the number of PCIn devices is %d", HandleCount));
61 |
62 |     for(HandleIndex = 0; HandleIndex < HandleCount; HandleIndex++)
63 |     {
64 |         Status = gBS->HandleProtocol(
65 |             PciHandleBuffer[HandleIndex],

```

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```

66         &gEfiPciIoProtocolGuid,
67         (VOID **)&(gPciIoArray[HandleIndex])
68     );
69 }
70
71 return Status;
72
73 }
74
75 EFI_STATUS ListPciInformation()
76 {
77     UINTN i, count = 0;
78     PCI_TYPE00 Pci;
79     DEBUG((DEBUG_ERROR, "[CSDN] PciDeviceNo VendorID DeviceID ClassCode\n"));
80     for (i = 0; i < gPciIoCount;i++)
81     {
82         gPciIoArray[i]->Pci.Read(gPciIoArray[i],EfiPciIoWidthUint32,0,sizeof(Pci)/sizeof(PCI_TYPE00),&Pci);
83         ++count;
84         DEBUG((DEBUG_ERROR, "[CSDN] %d\t\t%x\t%x\t%x\n", count, Pci.Hdr.VendorId, Pci.Hdr.DeviceId, Pci.Hdr.ClassCode[0]));
85     }
86
87     return EFI_SUCCESS;
88 }

```

The running results are as follows. It is found that the data of Class Code[0] read is different. I don't know why?

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