[UEFI Basics] NorFlash, NandFlash and SpiFlash

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NorFlash and NandFlash

Whether it is NorFlash or NanFlash, when we mention them, we are referring to memory chips.

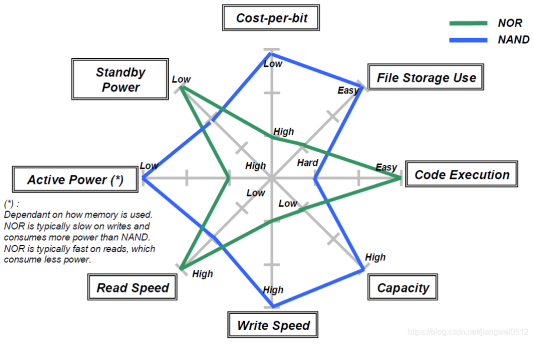
The main difference between the two is in the implementation principle. As for the principle, it is not the focus of this article, but it should be explained that whether it is NorFlash or NandFlash, it needs to be erased before writing data (NorFlash is slightly better, and it does not need to be erased to write a BIT from 1 to 0, but because most of the time we cannot operate only one BIT, so erasing is inevitable). Since this is related to Flash programming, it is still necessary to understand.

The following is a comparison between NorFlash and NandFlash:

characteristic	NorFlash	NandFlash
Proposed Company	Intel (not really)	Toshiba
Time of submission	1988	1989
capacity	Smaller	Larger
Reading speed	soon	quick
Write speed	slow	quick
Erasable times	less	More
Access method	Random Access	Block Access
price	Higher	Lower

The following figure is a comparison chart provided by Toshiba:

Fig. 1 Comparison of NOR and NAND Flash



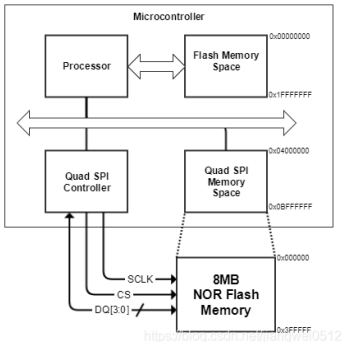
A few points need to be explained here:

1. In fact, both NorFlash and NandFlash were proposed by Toshiba. What happened in between is not the focus of this article.

2. The access methods of NorFlash and NandFlash are different, which is very important. Although NandFlash can also perform any access, NorFlash is more convenient in this regard, which enables it to easily complete XIP.

XIP

The full name of XIP is eXecute In Place. It means that the code on Flash can be executed without moving it to the memory first. At this time, the address space of the processor is directly mapped to Flash, so for the processor, Flash is just like ordinary memory, and data can be read from it (whether it can be written is uncertain, and it seems to have no application), as shown in the following figure:



This state is very important for BootLoader (such as BIOS), because when the system is powered on, there is no available memory, and the address contained in the Flash needs to be executed in place. In order to support XIP, it is necessary to ensure that both the Flash and the system controller (such as the SPI Flash controller on the PCH) support XIP mode. It is also necessary to explain here that the XIP mode has no direct relationship with NorFlash and NandFlash. Both can support XIP, but NorFlash is more suitable for XIP mode because it supports random access.

SPI Flash

We have introduced NorFlash and NandFlash before, but what about SPI Flash? Is it another type of Flash? No.

SPI Flash is just Flash that uses the SPI bus interface. It can be NorFlash or NandFlash. SPI stands for Serial Peripheral Interface, a serial bus interface that focuses on how the system accesses data. The data can be in Flash or in other memories, such as EEPROM. However, in BIOS development, SPI Flash usually refers to SPI NorFlash, because the BIOS is stored in this memory. After power-on, the BIOS runs in this chip until the memory is available, and then the BIOS data is moved to the memory to continue execution.

Summarize

NorFlash and NandFlash are storage chips with different features due to different implementation principles. SPI Flash can be used to store BIOS, usually NorFlash, and needs to support XIP.