

Lab 4 – Implementation

This contains coreb design => MBIST , EDT & OCC, SYNTHESIS , SCAN (with wrappers) , ATPG , SIMULATIONS (Need to be setup by user)

Step 1: MBIST Insertion

```
1 set_context dft -rtl -design_id rtl1
2 set_tsdb_output_directory ../../tsdb_outdir
3
4 open_tsdb ../../../../Lab3/corea/tsdb_outdir/
5
6 read_cell_library ../../../../library/adk.tcelllib
7 read_verilog ../../../../library/mems/SYNC_1R1W_16x8.v -exclude_from_file_dictionary
8
9 read_verilog ./design/coreb.v
10
11 read_design corea -design_id gate -view graybox -verbose
12
13 set_current_design coreb
14
15 set_design_level physical_block
16
17 add_clocks clka -period 10ns
18 add_clocks clkcb -period 13.2ns
19 add_clocks clkcc -period 14ns
20
21 set_dft_specification_requirements -memory_test on
22 check_design_rules
23 stop
24
25 set spec [create_dft_spec]
26 report_config_dat $spec
27 process_dft_spec
28 extract_icl
29 |
30 set_defaults_value /PatternsSpecification/SignoffOptions/simulate_instruments_in_lower_physical_instances on
31
32 set spec [create_patterns_spec]
33 report_config_data $spec
34 process_patterns_specification
35
36 set_simulation_library_sources -v ../../library/adk.v -y ../../library/mems/ -extension v
37
38 run_testbench_simulations
```

Why we have to specify design id?

- Because in the tsdb_out directory another sub directory will be created with design id name and all the output files if this particular run, it will be stored into tsdb output directory.

Line 2: it will give by default our tsdb output directory will be formed in our current directory. But if we won't give this command, the tsdb output directory will be created in the MBIST insertion directory, so we are specifying this command ... so that tsdb output directory will be created in the coreb directory ...

Line 4: we have to tell the tool in which tsdb output directory we will be able to find the corea related files.

Line 6: reading the library file

Line 7: Reading the memory related files

Line 9: Reading the coreb design netlist.

Line 11: corea is the top module name and gate is design id of Lab3 scan insertion. So we are asking the tool to read the graybox netlist.... While doing coreb level insertions, corea graybox netlist will be read while doing he coreb level insertion and icl, pdl and tcd file of corea will be read... so we have to tell the tool in which tsdb_output directory file will find the corea related files

Line 13: doing the elaboration

Line 15: doing the design level

Line 17 to 19: declaring all the clocks

Line 21: -memory_test on which means we are telling the tool that we are going to the mbist insertion ... so all the DRC which has to be checked before doing mbist insertion that will be checked and also the test hardware which has to be inserted for this particular run that will be included along with the dft specification line 25 ... when we give create dft specification command.

Line 22:

Line 25: create_dft_spec - what test hardware will be inserted into your design and it will be stored in spec

Line 26: the dft specification it will be displayed on the terminal

Line 27: validate the test hardware and dft specifications and it will generate the files and it will write it out into the instruments dir. Of tsdb output directory so it will write out the rtl, icl description of SIBs TDRs controllers and BAPs. It will also insert the test logic in coreb netlist and modified coreb netlist it will write it out into dft insertion direc

Line 28: the design file icl file will be generated so the coreb icl file will be generated.

Line 30: To validate the corea level mbist and icl network as well. So we are telling the tool to validate the corea level IJTAG and MBIST network.

Line 32: compare go on, reduce address count on, compare go id on that is pattern specs will be created.

Line 33: we will be going to see the pattern specs on terminal.

Line 34: it will validate the patterns specs and test benches.

Line 36: we are running adk files and mems files with extension v.

Line 38: it will run testbench simulations and it will give us the results.

```

/home/vinayakp/aug23/level3/Lab4/coreb/1.insert_mbist>>tessent -shell -dofile coreb_dft_rtl1.tcl
// Warning: Tessent user documentation not found
// Tessent Shell 2021.1   Fri Feb 26 20:45:56 GMT 2021
// Copyright 2011-2021 Mentor Graphics Corporation
//
// All Rights Reserved.
//
// THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION WHICH
// IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS AND IS
// SUBJECT TO LICENSE TERMS.
//
// Mentor Graphics software executing under x86-64 Linux on Mon Feb 05 14:49:16 IST 2024.
// 64 bit version
// Host: vlsiguru (64168 MB RAM, 32191 MB Swap)
//
// command: set_context dft -rtl -design_id rtl1
// command: set_tsdb_output_directory ..../tsdb_outdir
// command: open_tsdb ../../Lab3/corea/tsdb_outdir/
// command: read_cell_library ../../library/adk.tcelllib
// Reading DFT Library file ../../library/adk.tcelllib
// Finished reading file ../../library/adk.tcelllib
// command: read_verilog ../../library/mems/SYNC_1R1W_16x8.v -exclude_from_file_dictionary
// command: read_verilog ./design/coreb.v
// command: read_design corea -design_id gate -view graybox -verbose
// sub-command: set_read_design_tag corea
// sub-command: read_verilog ../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted_design/corea.vg_graybox -no_duplicate_modules_warnings
// sub-command: set_read_design_tag ""
// sub-command: read_icl ../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted_design/corea.icl -no_notes
// sub-command: source ../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted_design/corea.pdl

// sub-command: read_core_descriptions ../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted_design/corea.tcd
// command: set_current_design coreb
// Reading core description file ../../Lab3/corea/tsdb_outdir/instruments/corea_rtl2_edt.instrument/corea_rtl2_tessent_edt_c1.tcd
// command: set_design_level physical_block
// command: add_clocks clka -period 10ns
// command: add_clocks clkcb -period 13.2ns
// command: add_clocks clkcc -period 14ns
// command: set_dft_specification_requirements -memory_test on
// command: check_design_rules
// -----
// Begin RTL synthesis.
// -----
// Synthesized modules=1, Time=1.58 sec.
// Note: There was 1 module selectively synthesized. There were also 3 sub-modules created by synthesis.
//       Use 'get_module -filter is_synthetized' to see them.
//       You can also use 'set_quick_synthesis_options -verbose on' to have the synthesis step report the
//       synthesized module name in the transcript as it is being synthesized.
// -----
// Warning: Rule FN4 violation occurs 1340 times
// Flattening process completed, cell instances=5938, gates=16239, PIs=68, P0s=64, CPU time=0.07 sec.
// -----
// Begin circuit learning analyses.
// -----
// Learning completed, CPU time=0.04 sec.
// command: set spec [create_dft_spec]
// sub-command: create_dft_specification
// -----
// Begin creation of DftSpecification(coreb,rtl1)
//   Creation of RtlCells wrapper
//   Creation of IjtagNetwork wrapper

```

```
// Creation of MemoryBist wrapper
// Creation of MemoryBisr wrapper
//
// Done creation of DftSpecification(coreb,rtl1)
//
// command: report_config_data $spec

DftSpecification(coreb,rtl1) {
    IJtagNetwork {
        HostScanInterface(iJtag) {
            Sib(sri) {
                Attributes {
                    tesson_dft_function : scan_resource_instrument_host;
                }
            }
            Sib(pb1) {
                DesignInstance(corea_i1) {
                    scan_interface : iJtag;
                }
            }
            Sib(pb2) {
                DesignInstance(corea_i2) {
                    scan_interface : iJtag;
                }
            }
            Sib(pb3) {
                DesignInstance(corea_i3) {
                    scan_interface : iJtag;
                }
            }
            Sib(pb4) {
                DesignInstance(corea_i4) {
                    scan_interface : iJtag;
                }
            }
        }
    }
}
```

```

    Sib(sti) {
        Attributes {
            tesson_dft_function : scan_tested_instrument_host;
        }
        Sib(mbist) {
        }
    }
}

MemoryBist {
    ijttag_host_interface : Sib(mbist);
    Controller(c1) {
        clock_domain_label : clka;
        Step {
            MemoryInterface(m1) {
                instance_name : ram1;
            }
        }
    }
}
}

// command: process_dft_specification
//
// Begin processing of /DftSpecification(coreb,rtl1)
// --- IP generation phase ---
// Validation of IjtagNetwork
// Validation of MemoryBist
// Processing of RtlCells
// Generating Verilog RTL Cells
//     Verilog RTL : ../tsdb_outdir/instruments/coreb_rtl1_cells.instrument/coreb_rtl1_tesson_posedge_syncronizer_reset.v
//
// Loading the generated RTL verilog files (1) to enable instantiating the contained modules
// into the design.
// Processing of IjtagNetwork
// Generating design files for IJTAG SIB module coreb_rtl1_tesson_sib_1
//     Verilog RTL : ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tesson_sib_1.v
//     IJTAG ICL : ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tesson_sib_1.icl
//     TCD Scan : ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tesson_sib_1.tcd_scan
//     CTL : ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tesson_sib_1.ctl
//     TCD : ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tesson_sib_1.tcd
//     PDL : ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tesson_sib_1.pdl
// Generating design files for IJTAG SIB module coreb_rtl1_tesson_sib_2
//     Verilog RTL : ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tesson_sib_2.v
//     IJTAG ICL : ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tesson_sib_2.icl
// Generating design files for IJTAG SIB module coreb_rtl1_tesson_sib_3
//     Verilog RTL : ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tesson_sib_3.v
//     IJTAG ICL : ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tesson_sib_3.icl
// Generating design files for IJTAG SIB module coreb_rtl1_tesson_sib_4
//     Verilog RTL : ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tesson_sib_4.v
//     IJTAG ICL : ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tesson_sib_4.icl

```

```
// Loading the generated RTL verilog files (4) to enable instantiating the contained modules
// into the design.
// Processing of MemoryBist
// Generating the IJTAG ICL for the memories.
// Generating design files for MemoryBist Controller(c1)
// Warning: There are warnings issued while generating design files for MemoryBist controller(s).
// Review the messages in the following generation log files:
//     ..../tsdb_outdir/instruments/coreb_rtl1_mbist.instrument/coreb_rtl1_tessent_mbist_c1.generation_log
// Generating design files for Bist Access Port
//
// Loading the generated RTL verilog files (3) to enable instantiating the contained modules
// into the design.
// Generating design files for MemoryBist controller assembly
// --- Instrument insertion phase ---
// Inserting instruments of type 'ijtag'
// Inserting instruments of type 'memory_bist'
//
// Writing out modified source design in ..../tsdb_outdir/dft_inserted_designs/coreb_rtl1.dft_inserted_design
// Writing out specification in ..../tsdb_outdir/dft_inserted_designs/coreb_rtl1.dft_spec
//
// Done processing of DftSpecification(coreb,rtl1)
//
// command: extract_icl
// Note: Updating the hierarchical data model to reflect RTL design changes.
// Writing design source dictionary : ..../tsdb_outdir/dft_inserted_designs/coreb_rtl1.dft_inserted_design/coreb.
design_source_dictionary
// -----
// Begin RTL synthesis.
// -----
// Synthesized modules=1, Time=1.64 sec.
// Note: There was 1 module selectively synthesized. There were also 3 sub-modules created by synthesis.
// Use 'get_module -filter is_synthetized' to see them.
// You can also use 'set_quick_synthesis_options -verbose on' to have the synthesis step report the
//
// synthesized module name in the transcript as it is being synthesized.
// -----
// Warning: Rule FN1 violation occurs 1024 times
// Warning: Rule FN4 violation occurs 1344 times
// Warning: Rule FP13 violation occurs 153 times
// Flattening process completed, cell instances=6011, gates=16489, PIs=75, P0s=65, CPU time=0.11 sec.
// -----
// Begin circuit learning analyses.
// -----
// Learning completed, CPU time=0.01 sec.
// -----
// Begin ICL extraction.
// -----
// ICL extraction completed, ICL instances=15, CPU time=0.19 sec.
// -----
// -----
// Begin ICL elaboration and checking.
// -----
// ICL elaboration completed, CPU time=0.16 sec.
// -----
// Writing ICL file : ..../tsdb_outdir/dft_inserted_designs/coreb_rtl1.dft_inserted_design/coreb.icl
// Writing consolidated PDL file: ..../tsdb_outdir/dft_inserted_designs/coreb_rtl1.dft_inserted_design/coreb.pdl
//
// Writing SDC file: ..../tsdb_outdir/dft_inserted_designs/coreb_rtl1.dft_inserted_design/coreb.sdc
// Writing DFT info dictionary: ..../tsdb_outdir/dft_inserted_designs/coreb_rtl1.dft_inserted_design/coreb.dft_in
fo_dictionary
// command: set_defaults_value /PatternsSpecification/SignoffOptions/simulate_instruments_in_lower_physical_ins
tances_on
// command: set spec [create_patterns_spec]
// sub-command: create_patterns_specification
// Creating '/PatternsSpecification(coreb,rtl1,signoff)'
// Getting patterns specifications for the 'ijtag' instrument type
```

```
//  Getting patterns specifications for the 'memory_bist' instrument type
//  command: report_config_data $spec

PatternsSpecification(coreb,rtl1,signoff) {
    Patterns(ICLNetwork) {
        ICLNetworkVerify(coreb) {
            }
    }
    Patterns(ICLNetwork1) {
        ICLNetworkVerify(coreb) {
            }
        SimulationOptions {
            LowerPhysicalBlockInstances {
                corea_i1 : full;
            }
        }
    }
    Patterns(ICLNetwork2) {
        ICLNetworkVerify(coreb) {
            }
        SimulationOptions {
            LowerPhysicalBlockInstances {
                corea_i2 : full;
            }
        }
    }
    Patterns(ICLNetwork3) {
        ICLNetworkVerify(coreb) {
            }
        SimulationOptions {
            LowerPhysicalBlockInstances {
                corea_i3 : full;
            }
        }
    }
}
```

```
    }
}

Patterns(ICLNetwork4) {
    ICLNetworkVerify(coreb) {
    }
    SimulationOptions {
        LowerPhysicalBlockInstances {
            corea_i4 : full;
        }
    }
}
Patterns(MemoryBist_P1) {
    ClockPeriods {
        clkb : 13.2ns;
        clka : 10.0ns;
    }
    SimulationOptions {
        LowerPhysicalBlockInstances {
            corea_il : full;
        }
    }
}
TestStep(run_time_prog) {
    MemoryBist {
        run_mode : run_time_prog;
        reduced_address_count : on;
        Controller(corea_il.corea_rtl1_tessent_mbist_cl_controller_inst) {
            DiagnosisOptions {
                compare_go : on;
                compare_go_id : on;
            }
        }
    }
}
```

```
        }
    }
Controller(corea_il.corea_rtl1_tessent_mbist_c2_controller_inst) {
    DiagnosisOptions {
        compare_go : on;
        compare_go_id : on;
    }
}
}
}
}
Patterns(MemoryBist_ParallelRetentionTest_P1) {
ClockPeriods {
    clkb : 13.2ns;
    clka : 10.0ns;
}
SimulationOptions {
    LowerPhysicalBlockInstances {
        corea_il : full;
    }
}
TestStep(ParallelRetentionTest) {
    MemoryBist {
        run_mode : hw_default;
        parallel_retention_time : 0;
        reduced_address_count : on;
        Controller(corea_il.corea_rtl1_tessent_mbist_c1_controller_inst) {
            parallel_retention_group : 1;
            DiagnosisOptions {
                compare_go_id : on;
            }
        }
    }
}
```

```
Controller(corea_il.corea_rtl1_tessent_mbist_c2_controller_inst) {
    DiagnosisOptions {
        compare_go : on;
        compare_go_id : on;
    }
}
}
}
Patterns(MemoryBist_ParallelRetentionTest_P1) {
    ClockPeriods {
        clkb : 13.2ns;
        clka : 10.0ns;
    }
    SimulationOptions {
        LowerPhysicalBlockInstances {
            corea_il : full;
        }
    }
}
TestStep(ParallelRetentionTest) {
    MemoryBist {
        run_mode : hw_default;
        parallel_retention_time : 0;
        reduced_address_count : on;
        Controller(corea_il.corea_rtl1_tessent_mbist_cl_controller_inst) {
            parallel_retention_group : 1;
            DiagnosisOptions {
                compare_go_id : on;
            }
        }
        Controller(corea_il.corea_rtl1_tessent_mbist_c2_controller_inst) {
            parallel_retention_group : 1;
            DiagnosisOptions {
```

```
DiagnosisOptions {
    compare_go_id : on;
}
}
Controller(corea_i1.corea_rtl1_tessent_mbist_c2_controller_inst) {
    parallel_retention_group : 1;
    DiagnosisOptions {
        compare_go_id : on;
    }
}
}
}
Patterns(MemoryBist_P2) {
    ClockPeriods {
        clkb : 13.2ns;
        clka : 10.0ns;
    }
    SimulationOptions {
        LowerPhysicalBlockInstances {
            corea_i2 : full;
        }
    }
}
TestStep(run_time_prog) {
    MemoryBist {
        run_mode : run_time_prog;
        reduced_address_count : on;
        Controller(corea_i2.corea_rtl1_tessent_mbist_c1_controller_inst) {
            DiagnosisOptions {
                compare_go : on;
                compare_go_id : on;
            }
        }
    }
}
```

```
Controller(corea_i2.corea_rtl1_tessent_mbist_c2_controller_inst) {
    DiagnosisOptions {
        compare_go : on;
        compare_go_id : on;
    }
}
}
}
}
Patterns(MemoryBist_ParallelRetentionTest_P2) {
    ClockPeriods {
        clkb : 13.2ns;
        clka : 10.0ns;
    }
    SimulationOptions {
        LowerPhysicalBlockInstances {
            corea_i2 : full;
        }
    }
}
TestStep(ParallelRetentionTest) {
    MemoryBist {
        run_mode : hw_default;
        parallel_retention_time : 0;
        reduced_address_count : on;
        Controller(corea_i2.corea_rtl1_tessent_mbist_c1_controller_inst) {
            parallel_retention_group : 1;
            DiagnosisOptions {
                compare_go_id : on;
            }
        }
        Controller(corea_i2.corea_rtl1_tessent_mbist_c2_controller_inst) {
            parallel_retention_group : 1;
            DiagnosisOptions {
                compare_go_id : on;
```

```
        }
    }
}
Patterns(MemoryBist_P3) {
    ClockPeriods {
        clk_b : 13.2ns;
        clk_a : 10.0ns;
    }
    SimulationOptions {
        LowerPhysicalBlockInstances {
            corea_i3 : full;
        }
    }
TestStep(run_time_prog) {
    MemoryBist {
        run_mode : run_time_prog;
        reduced_address_count : on;
        Controller(corea_i3.corea_rtll_tessent_mbist_c1_controller_inst) {
            DiagnosisOptions {
                compare_go : on;
                compare_go_id : on;
            }
        }
        Controller(corea_i3.corea_rtll_tessent_mbist_c2_controller_inst) {
            DiagnosisOptions {
                compare_go : on;
                compare_go_id : on;
            }
        }
    }
}
```

```
Patterns(MemoryBist_ParallelRetentionTest_P3) {
    ClockPeriods {
        clkb : 13.2ns;
        clka : 10.0ns;
    }
    SimulationOptions {
        LowerPhysicalBlockInstances {
            corea_i3 : full;
        }
    }
    TestStep(ParallelRetentionTest) {
        MemoryBist {
            run_mode : hw_default;
            parallel_retention_time : 0;
            reduced_address_count : on;
            Controller(corea_i3.corea_rtl1_tessent_mbist_c1_controller_inst) {
                parallel_retention_group : 1;
                DiagnosisOptions {
                    compare_go_id : on;
                }
            }
            Controller(corea_i3.corea_rtl1_tessent_mbist_c2_controller_inst) {
                parallel_retention_group : 1;
                DiagnosisOptions {
                    compare_go_id : on;
                }
            }
        }
    }
}
```

```
Patterns(MemoryBist_P4) {
    ClockPeriods {
        clkb : 13.2ns;
        clka : 10.0ns;
    }
    SimulationOptions {
        LowerPhysicalBlockInstances {
            corea_i4 : full;
        }
    }
    TestStep(run_time_prog) {
        MemoryBist {
            run_mode : run_time_prog;
            reduced_address_count : on;
            Controller(corea_i4.corea_rtl1_tessent_mbist_c1_controller_inst) {
                DiagnosisOptions {
                    compare_go : on;
                    compare_go_id : on;
                }
            }
            Controller(corea_i4.corea_rtl1_tessent_mbist_c2_controller_inst) {
                DiagnosisOptions {
                    compare_go : on;
                    compare_go_id : on;
                }
            }
        }
    }
}
```

```
Patterns(MemoryBist_ParallelRetentionTest_P4) {
    ClockPeriods {
        clk_b : 13.2ns;
        clk_a : 10.0ns;
    }
    SimulationOptions {
        LowerPhysicalBlockInstances {
            corea_i4 : full;
        }
    }
    TestStep(ParallelRetentionTest) {
        MemoryBist {
            run_mode : hw_default;
            parallel_retention_time : 0;
            reduced_address_count : on;
            Controller(corea_i4.corea_rtll_tessent_mbist_c1_controller_inst) {
                parallel_retention_group : 1;
                DiagnosisOptions {
                    compare_go_id : on;
                }
            }
            Controller(corea_i4.corea_rtll_tessent_mbist_c2_controller_inst) {
                parallel_retention_group : 1;
                DiagnosisOptions {
                    compare_go_id : on;
                }
            }
        }
    }
}
```

```
Patterns(MemoryBist_P5) {
    ClockPeriods {
        clka : 10.0ns;
    }
    TestStep(run_time_prog) {
        MemoryBist {
            run_mode : run_time_prog;
            reduced_address_count : on;
            Controller(coreb_rtl1_tessent_mbist_cl_controller_inst) {
                DiagnosisOptions {
                    compare_go : on;
                    compare_go_id : on;
                }
            }
        }
    }
}
Patterns(MemoryBist_ParallelRetentionTest_P5) {
    ClockPeriods {
        clka : 10.0ns;
    }
    TestStep(ParallelRetentionTest) {
        MemoryBist {
            run_mode : hw_default;
            parallel_retention_time : 0;
            reduced_address_count : on;
            Controller(coreb_rtl1_tessent_mbist_cl_controller_inst) {
                parallel_retention_group : 1;
                DiagnosisOptions {
                    compare_go_id : on;
                }
            }
        }
    }
}
```

```
// command: process_patterns_specification
//
// Begin processing of /PatternsSpecification(coreb,rtl1,signoff)
//
// Processing of /PatternsSpecification(coreb,rtl1,signoff)/Patterns(ICLNetwork)
//
// Creation of pattern 'ICLNetwork'
// Solving ICLNetworkVerify(coreb)
//
// Writing pattern file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/ICLNetwork.v'
//
// Processing of /PatternsSpecification(coreb,rtl1,signoff)/Patterns(ICLNetwork1)
//
// Creation of pattern 'ICLNetwork1'
// Solving ICLNetworkVerify(coreb)
//
// Writing pattern file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/ICLNetwork1.v'
//
// Processing of /PatternsSpecification(coreb,rtl1,signoff)/Patterns(ICLNetwork2)
//
// Creation of pattern 'ICLNetwork2'
// Solving ICLNetworkVerify(coreb)
//
// Writing pattern file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/ICLNetwork2.v'
//
// Processing of /PatternsSpecification(coreb,rtl1,signoff)/Patterns(ICLNetwork3)
//
// Creation of pattern 'ICLNetwork3'
// Solving ICLNetworkVerify(coreb)
//
// Writing pattern file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/ICLNetwork3.v'

// Processing of /PatternsSpecification(coreb,rtl1,signoff)/Patterns(ICLNetwork4)
//
// Creation of pattern 'ICLNetwork4'
// Solving ICLNetworkVerify(coreb)
//
// Writing pattern file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/ICLNetwork4.v'

// Processing of /PatternsSpecification(coreb,rtl1,signoff)/Patterns(MemoryBist_P1)
// Processing of TestStep(run_time_prog) instrument 'memory_bist'
//
// Creation of pattern 'MemoryBist_P1'
// Solving TestStep(run_time_prog)
//
// Writing pattern file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/MemoryBist_P1.v'

// Processing of /PatternsSpecification(coreb,rtl1,signoff)/Patterns(MemoryBist_P2)
// Processing of TestStep(run_time_prog) instrument 'memory_bist'
//
// Creation of pattern 'MemoryBist_P2'
// Solving TestStep(run_time_prog)
//
// Writing pattern file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/MemoryBist_P2.v'

// Processing of /PatternsSpecification(coreb,rtl1,signoff)/Patterns(MemoryBist_P3)
// Processing of TestStep(run_time_prog) instrument 'memory_bist'
//
// Creation of pattern 'MemoryBist_P3'
// Solving TestStep(run_time_prog)
//
// Writing pattern file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/MemoryBist_P3.v'
```

```
// Processing of /PatternsSpecification(coreb,rtl1,signoff)/Patterns(MemoryBist_P4)
//   Processing of TestStep(run_time_prog) instrument 'memory_bist'
//
// Creation of pattern 'MemoryBist_P4'
//   Solving TestStep(run_time_prog)
//
// Writing pattern file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/MemoryBist_P4.v'
//
// Processing of /PatternsSpecification(coreb,rtl1,signoff)/Patterns(MemoryBist_P5)
//   Processing of TestStep(run_time_prog) instrument 'memory_bist'
//
// Creation of pattern 'MemoryBist_P5'
//   Solving TestStep(run_time_prog)
//
// Writing pattern file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/MemoryBist_P5.v'
//
// Processing of /PatternsSpecification(coreb,rtl1,signoff)/Patterns(MemoryBist_ParallelRetentionTest_P1)
//   Processing of TestStep(ParallelRetentionTest) instrument 'memory_bist'
//
// Creation of pattern 'MemoryBist_ParallelRetentionTest_P1'
//   Solving TestStep(ParallelRetentionTest)
//
// Writing pattern file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/MemoryBist_ParallelRetentionTe
st_P1.v'
//
// Processing of /PatternsSpecification(coreb,rtl1,signoff)/Patterns(MemoryBist_ParallelRetentionTest_P2)
//   Processing of TestStep(ParallelRetentionTest) instrument 'memory_bist'
//
// Creation of pattern 'MemoryBist_ParallelRetentionTest_P2'
//   Solving TestStep(ParallelRetentionTest)
//
// Writing pattern file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/MemoryBist_ParallelRetentionTe
st_P2.v'
//
// Processing of /PatternsSpecification(coreb,rtl1,signoff)/Patterns(MemoryBist_ParallelRetentionTest_P3)
//   Processing of TestStep(ParallelRetentionTest) instrument 'memory_bist'
//
// Creation of pattern 'MemoryBist_ParallelRetentionTest_P3'
//   Solving TestStep(ParallelRetentionTest)
//
// Writing pattern file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/MemoryBist_ParallelRetentionTe
st_P3.v'
//
// Processing of /PatternsSpecification(coreb,rtl1,signoff)/Patterns(MemoryBist_ParallelRetentionTest_P4)
//   Processing of TestStep(ParallelRetentionTest) instrument 'memory_bist'
//
// Creation of pattern 'MemoryBist_ParallelRetentionTest_P4'
//   Solving TestStep(ParallelRetentionTest)
//
// Writing pattern file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/MemoryBist_ParallelRetentionTe
st_P4.v'
//
// Processing of /PatternsSpecification(coreb,rtl1,signoff)/Patterns(MemoryBist_ParallelRetentionTest_P5)
//   Processing of TestStep(ParallelRetentionTest) instrument 'memory_bist'
//
// Creation of pattern 'MemoryBist_ParallelRetentionTest_P5'
//   Solving TestStep(ParallelRetentionTest)
//
// Writing pattern file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/MemoryBist_ParallelRetentionTe
st_P5.v'
//   Writing simulation data dictionary file '../tsdb_outdir/patterns/coreb_rtl1.patterns_signoff/simulation.
data_dictionary'
//
// Done processing of /PatternsSpecification(coreb,rtl1,signoff)
```

```
// Writing configuration data file '../tsdb_outdir/patterns/coreb_rtl1.patterns_spec_signoff'.
// command: set_simulation_library_sources -v ../../library/adk.v -y ../../library/mems/ -extension v
// command: run_testbench_simulations
Starting 15 simulations for ./simulation_outdir/coreb_rtl1.simulation_signoff
// Waiting for the simulation(s) to complete

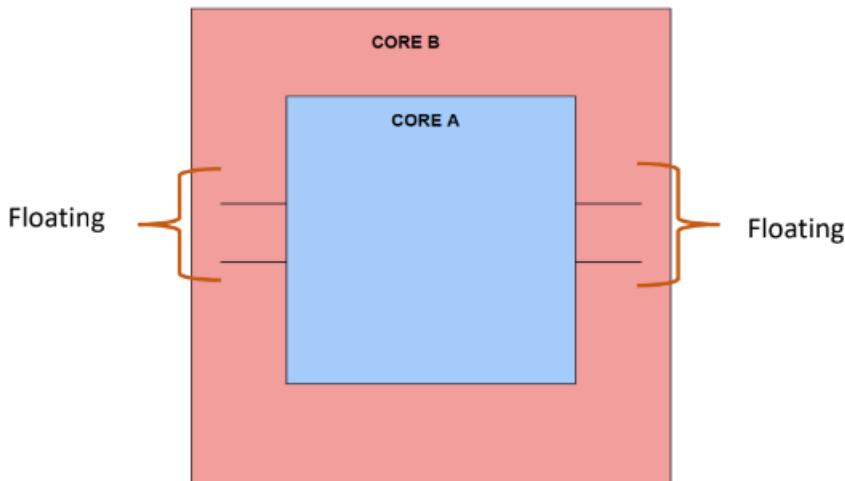
unscheduled 0 queued 0 running 0 pass 15 fail 0
SETUP ■
```

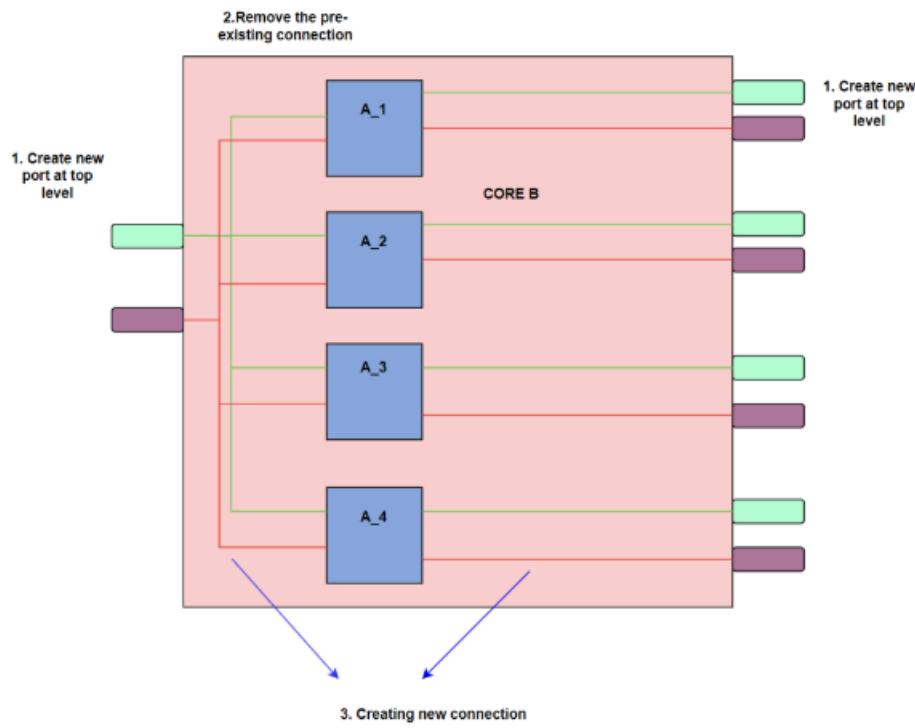
Step 2: EDT and OCC insertion

```
1
2 proc process_dft_specification.post_insertion {coreb args} {
3
4   create_port coreb_to_corea_edt_channels_in[1:0] -direction input
5   create_port corea_i1_to_coreb_edt_channels_out[1:0] -direction output
6   create_port corea_i2_to_coreb_edt_channels_out[1:0] -direction output
7   create_port corea_i3_to_coreb_edt_channels_out[1:0] -direction output
8   create_port corea_i4_to_coreb_edt_channels_out[1:0] -direction output
9
10  delete_connections /corea_i1/corea_rtl2_controller_c1_edt_channels_in
11  delete_connections /corea_i2/corea_rtl2_controller_c1_edt_channels_in
12  delete_connections /corea_i3/corea_rtl2_controller_c1_edt_channels_in
13  delete_connections /corea_i4/corea_rtl2_controller_c1_edt_channels_in
14
15  delete_connections /corea_i1/corea_rtl2_controller_c1_edt_channels_out
16  delete_connections /corea_i2/corea_rtl2_controller_c1_edt_channels_out
17  delete_connections /corea_i3/corea_rtl2_controller_c1_edt_channels_out
18  delete_connections /corea_i4/corea_rtl2_controller_c1_edt_channels_out
19
20  create_connections coreb_to_corea_edt_channels_in /corea_i1/corea_rtl2_controller_c1_edt_channels_in
21  create_connections coreb_to_corea_edt_channels_in /corea_i2/corea_rtl2_controller_c1_edt_channels_in
22  create_connections coreb_to_corea_edt_channels_in /corea_i3/corea_rtl2_controller_c1_edt_channels_in
23  create_connections coreb_to_corea_edt_channels_in /corea_i4/corea_rtl2_controller_c1_edt_channels_in
24
25  create_connections /corea_i1/corea_rtl2_controller_c1_edt_channels_out corea_i1_to_coreb_edt_channels_out
26  create_connections /corea_i2/corea_rtl2_controller_c1_edt_channels_out corea_i2_to_coreb_edt_channels_out
27  create_connections /corea_i3/corea_rtl2_controller_c1_edt_channels_out corea_i3_to_coreb_edt_channels_out
28  create_connections /corea_i4/corea_rtl2_controller_c1_edt_channels_out corea_i4_to_coreb_edt_channels_out
29 }
```

We are creating 1 input port and 4 output ports

EXPLANATION OF ‘post_dft_insertion_procedure’ FILE In EDT insertion RUN (Lab4)





```

1 set_context dft -rtl -design_id rtl2
2 set_tsdb_output_directory ..../tsdb_outdir
3 open_tsdb ..../..../Lab3/corea/tsdb_outdir
4
5 read_design coreb -design_id rtl1 -verbose
6 read_design corea -design_id gate -view graybox -verbose
7
8 read_cell_library ../../library/adk.tcelllib
9 read_verilog ../../library/mems/SYNC_1R1W_16x8.v -exclude_from_file_dictionary
10 |
11 set_current_design coreb
12 set_dft_specification_requirements -logic_test on
13
14 add_dft_signal memory_bypass_en tck_occ_en
15 add_dft_signal ltest_en int_mode ext_mode
16 add_dft_signal test_clock edt_update scan_en -source_node {my_test_clock my_edt_update my_scan_en}
17 add_dft_signal edt_clock shift_capture_clock -create_from_other_signals
18 add_dft_signal int_ltest_en ext_ltest_en
19
20 set_static_dft_signal_values ext_mode 1 -instance corea_i1
21 set_static_dft_signal_values ext_mode 1 -instance corea_i2
22 set_static_dft_signal_values ext_mode 1 -instance corea_i3
23 set_static_dft_signal_values ext_mode 1 -instance corea_i4
24
25 check_design_rules
26
27 set spec [create_dft_spec -sri_sib_list {occ edt}]
28
29 read_config_data -in_wrapper $spec -from_string {
30   Occ {
31     ijttag_host_interface : Sib(occ);
32     Controller(clka) {
33       clock_intercept_node : clka;

```

```

34 }
35 Controller(clkb) {
36     clock_intercept_node : clkb;
37 }
38 Controller(clkc) {
39     clock_intercept_node : clkc;
40 }
41 }
42 Edt {
43     ijtag_host_interface : Sib(edt);
44     Controller(c1) {
45         longest_chain_range      : 10, 50;
46         scan_chain_count        : 15;
47         input_channel_count    : 2;
48         output_channel_count   : 1;
49     }
50 }
51 }
52
53 source post_dft_insertion_procedure.tcl
54
55 process_dft_specification
56 extract_icl
57
58 set_defaults_value /PatternsSpecification/SignoffOptions/simulate_instruments_in_lower_physical_instances on
59 set spec [create_patterns_spec]
60 report_config_data $spec
61 process_patterns_specification
62
63 set_simulation_library_sources -v ../../library/adk.v -y ../../library/mems/ -extension v
64
65 run_testbench_simulations
66 write_design_import_script -use_relative_path_to . -replace
67
68

```

Line 58: we are telling the tool to validate the corea level ijtag network and mbist

Line 59: creating the pattern specifications and it will be stored into variable called as spec

Line 60: we are able to see the pattern spec on terminal

Line 61: it will validate all the patterns and it will write it out into the pattern spec of tsdb out directory

Line 66: what are all the files read during the synthesis run, the path of all these files will be written out.

```
/home/vinayakp/aug23/level3/Lab4/coreb/2.insert_edt_occ>>tessent -shell -dofile coreb_dft_rtl2.tcl
// Warning: Tessent user documentation not found
// Tessent Shell 2021.1 Fri Feb 26 20:45:56 GMT 2021
// Copyright 2011-2021 Mentor Graphics Corporation
//
// All Rights Reserved.
//
// THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION WHICH
// IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS AND IS
// SUBJECT TO LICENSE TERMS.
//
// Mentor Graphics software executing under x86-64 Linux on Fri Feb 09 00:39:52 IST 2024.
// 64 bit version
// Host: vlsiguru (64168 MB RAM, 32191 MB Swap)
//
// command: set_context dft -rtl -design_id rtl2
// command: set_tsdb_output_directory ../tsdb_outdir
// command: open_tsdb ../../Lab3/coreb/tsdb_outdir
// command: read_design coreb -design_id rtl1 -verbose
// sub-command: set_tool_options -reapply_settings_after_reelaboration On
// sub-command: set_read_design_tag coreb
// sub-command: ##### read1 #####
set_design_include_directories \
{../../1.insert_mbist}

set_design_macros -clear

set_design_sources -format verilog -clear
read_verilog \
{../tsdb_outdir/dft_inserted_designs/coreb_rtl1.dft_inserted_design/modified_rtl_files/coreb.v} \
-in_library work \
-format 2001 \
-no_duplicate_modules_warnings

// sub-command: ##### read2 #####
set_design_include_directories \
{../../1.insert_mbist}

set_design_macros -clear

set_design_sources -format verilog -clear
read_verilog \
{../tsdb_outdir/instruments/coreb_rtl1_cells.instrument/coreb_rtl1_tessent_posedge_synchronizer_reset.v} \
-in_library work \
-format 2001 \
-no_duplicate_modules_warnings

// sub-command: ##### read3 #####
set_design_include_directories \
{../../1.insert_mbist}

set_design_macros -clear
```

```

set_design_sources -format verilog -clear
read_verilog \
{../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tessent_sib_1.v
 ..../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tessent_sib_2.v
 ..../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tessent_sib_3.v
 ..../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tessent_sib_4.v} \
-in_library work \
-format 2001 \
-no_duplicate_modules_warnings

// sub-command: ##### read4 #####
set_design_include_directories \
{..../1.insert_mbist}

set_design_macros -clear

set_design_sources -format verilog -clear
read_verilog \
{../tsdb_outdir/instruments/coreb_rtl1_mbist.instrument/coreb_rtl1_tessent_mbist_bap.v
 ..../tsdb_outdir/instruments/coreb_rtl1_mbist.instrument/coreb_rtl1_tessent_mbist_c1_controller.v
 ..../tsdb_outdir/instruments/coreb_rtl1_mbist.instrument/coreb_rtl1_tessent_mbist_c1_interface_m1.v} \
-in_library work \
-format 2001 \
-no_duplicate_modules_warnings

// sub-command: set_read_design_tag ""
// sub-command: set_design_sources -format verilog -clear
// sub-command: set_design_include_directories -clear
// sub-command: set_design_macros -clear
// sub-command: set_tool_options -reapply_settings_after_reelaboration off
// sub-command: read_icl ../tsdb_outdir/dft_inserted_designs/coreb_rtl1.dft_inserted_design/coreb.icl -skip_chi
ld_blocks -no_notes
// sub-command: source ../tsdb_outdir/dft_inserted_designs/coreb_rtl1.dft_inserted_design/coreb.pdl
// sub-command: read_core_descriptions ../tsdb_outdir/dft_inserted_designs/coreb_rtl1.dft_inserted_design/coreb
.tcd
// command: read_design corea -design_id gate -view graybox -verbose
// sub-command: set_read_design_tag corea
// sub-command: read_verilog ../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted_desig
n/corea.vg_graybox -no_duplicate_modules_warnings
// sub-command: set_read_design_tag ""
// sub-command: read_icl ../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted_design/co
rea.icl -no_notes
// sub-command: source ../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted_design/core
a.pdl
// sub-command: read_core_descriptions ../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inse
rted_design/corea.tcd
// command: read_cell_library ../../library/adk.tcelllib
// Reading DFT Library file ../../library/adk.tcelllib
// Finished reading file ../../library/adk.tcelllib
// command: read_verilog ../../library/mems/SYNC_1R1W_16x8.v -exclude_from_file_dictionary
// command: set_current_design coreb
// -----
// Begin ICL elaboration and checking.
// -----
// ICL elaboration completed, CPU time=0.17 sec.
// -----

```

```

// Reading core description file ../../Lab3/corea/tsdb_outdir/instruments/corea_rtl2_edt.instrument/corea_rt
l2_tessent_edt.tcd
// command: set_dft_specification_requirements -logic_test on
// command: add_dft_signals memory_bypass_en tck_occ_en
// command: add_dft_signals ltest_en int_mode ext_mode
// command: add_dft_signals test_clock edt_update scan_en -source_node {my_test_clock my_edt_update my_scan_en}
// command: add_dft_signals edt_clock shift_capture_clock -create_from_other_signals
// command: add_dft_signals int_ltest_en ext_ltest_en
// command: set_static_dft_signal_values ext_mode 1 -instance corea_i1
// command: set_static_dft_signal_values ext_mode 1 -instance corea_i2
// command: set_static_dft_signal_values ext_mode 1 -instance corea_i3
// command: set_static_dft_signal_values ext_mode 1 -instance corea_i4
// command: check_design_rules
// Warning: Primary input 'corea_i1/edt_update_pport' is added at pin '/corea_i1/edt_update'
// Warning: Primary input 'corea_i2/edt_update_pport' is added at pin '/corea_i2/edt_update'
// Warning: Primary input 'corea_i3/edt_update_pport' is added at pin '/corea_i3/edt_update'
// Warning: Primary input 'corea_i4/edt_update_pport' is added at pin '/corea_i4/edt_update'
// Note: Inferred 12 'add_dft_control_points <pin>' commands to connect the DFT signals pins
// on the child block instances. Use report_dft_control_points to see them.
// -----
// Begin RTL synthesis.
// -----
// Synthesized modules=26, Time=3.39 sec.
// -----
// Warning: Rule FN4 violation occurs 1348 times
// Flattening process completed, cell instances=20425, gates=37122, PIs=75+9(pseudo ports), P0s=65, CPU time=0.
18 sec.
// -----
// Begin circuit learning analyses.
// -----
// Learning completed, CPU time=0.12 sec.
// Begin simulation of test_setup procedure with 99 cycles.
// Simulation of test_setup procedure completed, CPU time=0.0 sec.

// -----
// Begin simulation of auto-generated load_unload procedure.
// Simulation of load_unload procedure completed, CPU time=0.0 sec.
// Scan segment = ext_mode/corea_i1/ts_ext_mode_so[4] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i1/ts_ext_mode_so[3] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i1/ts_ext_mode_so[2] successfully traced with scan_cells = 28.
// Scan segment = ext_mode/corea_i1/ts_ext_mode_so[1] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i1/ts_ext_mode_so[0] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i2/ts_ext_mode_so[4] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i2/ts_ext_mode_so[3] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i2/ts_ext_mode_so[2] successfully traced with scan_cells = 28.
// Scan segment = ext_mode/corea_i2/ts_ext_mode_so[1] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i2/ts_ext_mode_so[0] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i3/ts_ext_mode_so[4] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i3/ts_ext_mode_so[3] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i3/ts_ext_mode_so[2] successfully traced with scan_cells = 28.
// Scan segment = ext_mode/corea_i3/ts_ext_mode_so[1] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i3/ts_ext_mode_so[0] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i4/ts_ext_mode_so[4] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i4/ts_ext_mode_so[3] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i4/ts_ext_mode_so[2] successfully traced with scan_cells = 28.
// Scan segment = ext_mode/corea_i4/ts_ext_mode_so[1] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i4/ts_ext_mode_so[0] successfully traced with scan_cells = 27.
// Scan segment = /coreb_rtl1_tessent_sib_sti_inst/ltest_so successfully traced with scan_cells = 7.
// 551 scan cells have been identified in 21 scan segments.
// Longest scan segment has 28 scan cells.
// Warning: 1 edge-triggered clock ports set to stable high. (D7)
// command: set spec [create_dft_spec -sri_sib_list {occ edt}]
// sub-command: create_dft_specification -sri_sib_list "occ edt"
//

```

```

// Begin creation of DftSpecification(coreb,rtl2)
// Creation of RtlCells wrapper
// Creation of IjtagNetwork wrapper
//
// Done creation of DftSpecification(coreb,rtl2)
//
// command: read_config_data -in_wrapper $spec -from_string {
Occ {
    ijtag_host_interface : Sib(occ);
    Controller(clka) {
        clock_intercept_node : clka;
    }
    Controller(clkb) {
        clock_intercept_node : clkb;
    }
    Controller(clkc) {
        clock_intercept_node : clkc;
    }
}
Edt {
    ijtag_host_interface : Sib(edt);
    Controller(c1) {
        longest_chain_range      : 10, 50;
        scan_chain_count         : 15;
        input_channel_count      : 2;
        output_channel_count     : 1;
    }
}
}

// command: source post_dft_insertion_procedure.tcl
// command: process_dft_specification
//
// Begin processing of /DftSpecification(coreb,rtl2)
// --- IP generation phase ---
// Validation of IjtagNetwork
// Validation of OCC
// Validation of EDT
// Processing of RtlCells
// Generating Verilog RTL Cells
// Verilog RTL : ../tsdb_outdir/instruments/coreb_rtl2_cells.instrument/coreb_rtl2_tessent_posedge_syncronizer_reset.v
//
// Loading the generated RTL verilog files (1) to enable instantiating the contained modules
// into the design.
// Processing of IjtagNetwork
// Generating design files for IJTAG SIB module coreb_rtl2_tessent_sib_1
// Verilog RTL : ../tsdb_outdir/instruments/coreb_rtl2_ijtag.instrument/coreb_rtl2_tessent_sib_1.v
// IJTAG ICL   : ../tsdb_outdir/instruments/coreb_rtl2_ijtag.instrument/coreb_rtl2_tessent_sib_1.icl
// Generating design files for IJTAG Tdr module coreb_rtl2_tessent_tdr_sri_ctrl
// Verilog RTL : ../tsdb_outdir/instruments/coreb_rtl2_ijtag.instrument/coreb_rtl2_tessent_tdr_sri_ctrl.v
// IJTAG ICL   : ../tsdb_outdir/instruments/coreb_rtl2_ijtag.instrument/coreb_rtl2_tessent_tdr_sri_ctrl.i
cl
//
// Loading the generated RTL verilog files (2) to enable instantiating the contained modules
// into the design.
// Processing of OCC
// Generating design files for OCC module coreb_rtl2_tessent_occ
// Verilog RTL : ../tsdb_outdir/instruments/coreb_rtl2_occ.instrument/coreb_rtl2_tessent_occ.v
// IJTAG ICL   : ../tsdb_outdir/instruments/coreb_rtl2_occ.instrument/coreb_rtl2_tessent_occ.icl
// IJTAG PDL   : ../tsdb_outdir/instruments/coreb_rtl2_occ.instrument/coreb_rtl2_tessent_occ.pdl
// TCD       : ../tsdb_outdir/instruments/coreb_rtl2_occ.instrument/coreb_rtl2_tessent_occ.tcd
// TCD Scan  : ../tsdb_outdir/instruments/coreb_rtl2_occ.instrument/coreb_rtl2_tessent_occ.tcd_scan
// CTL       : ../tsdb_outdir/instruments/coreb_rtl2_occ.instrument/coreb_rtl2_tessent_occ.ctl

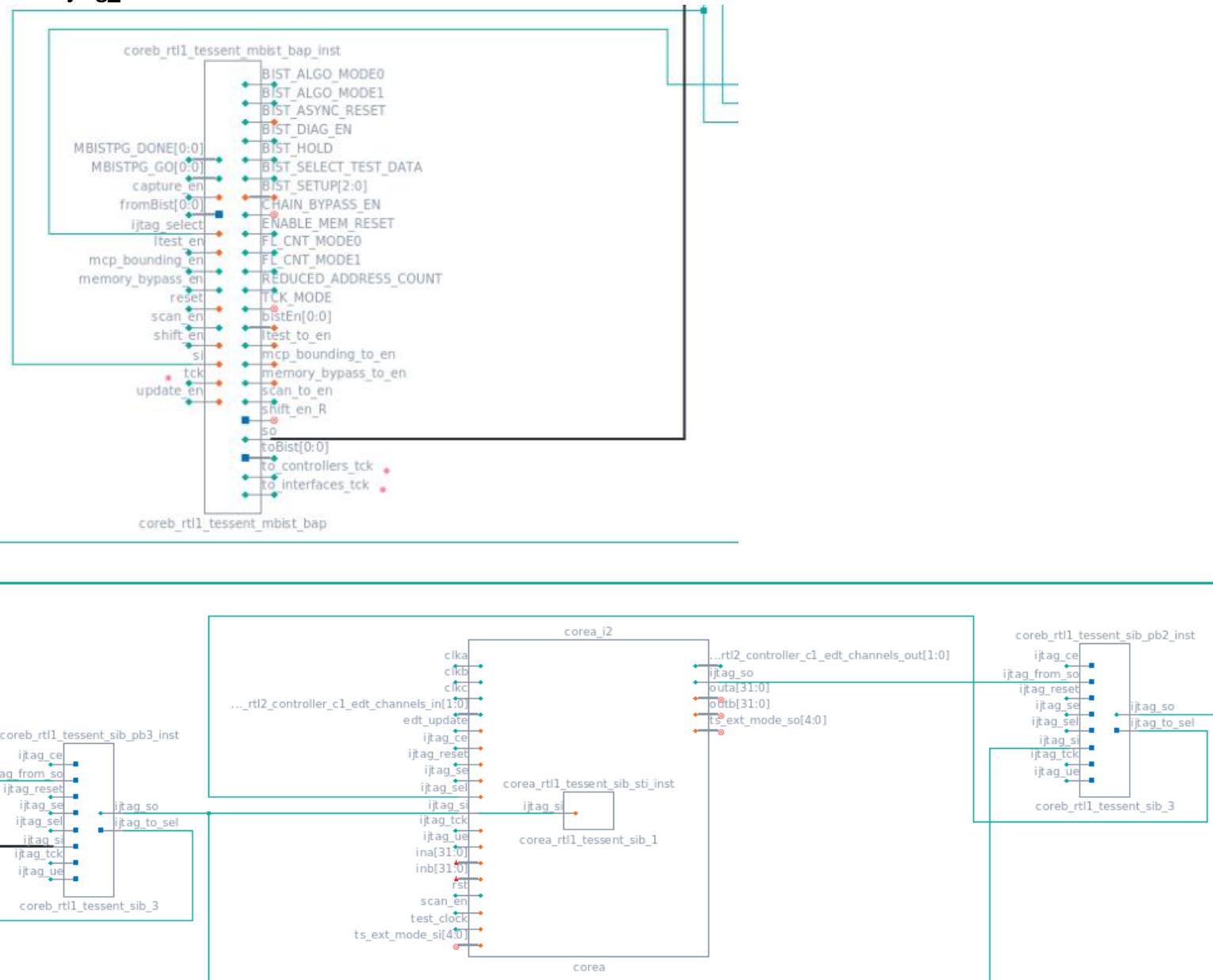
```

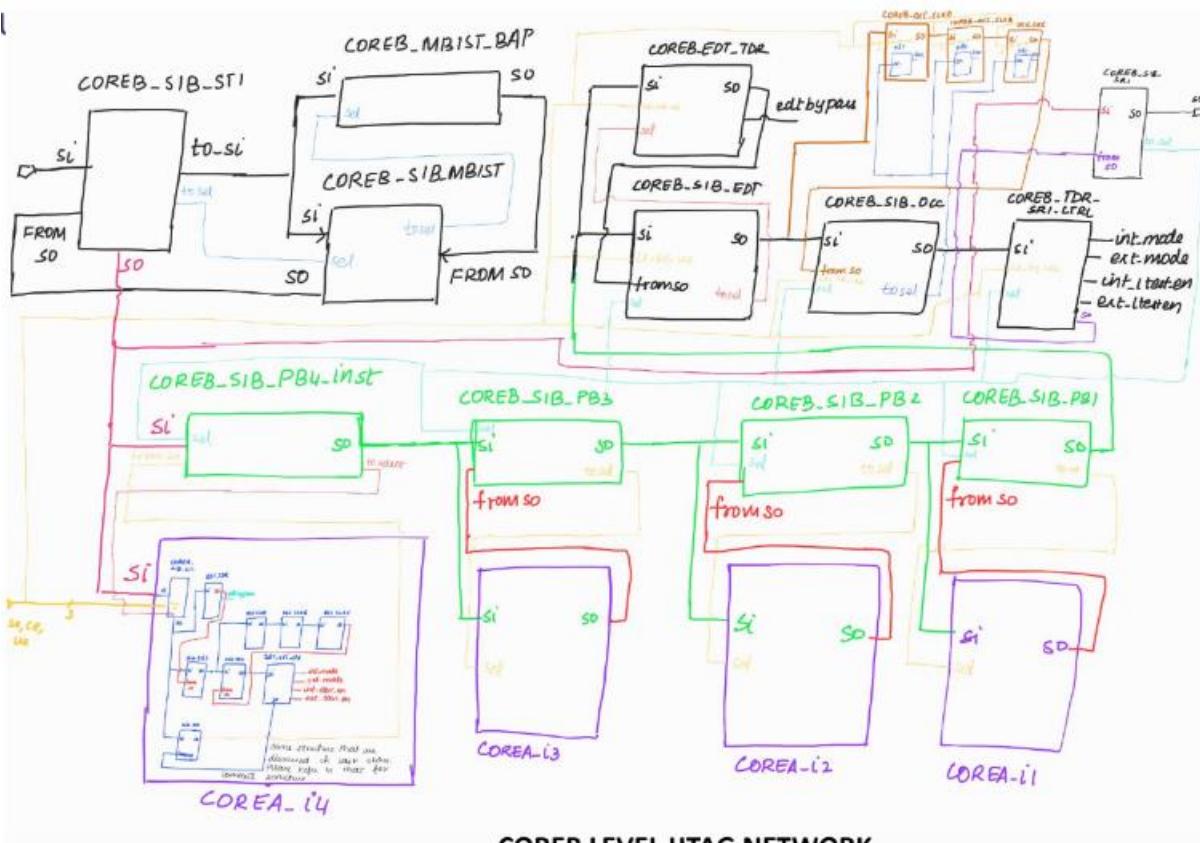
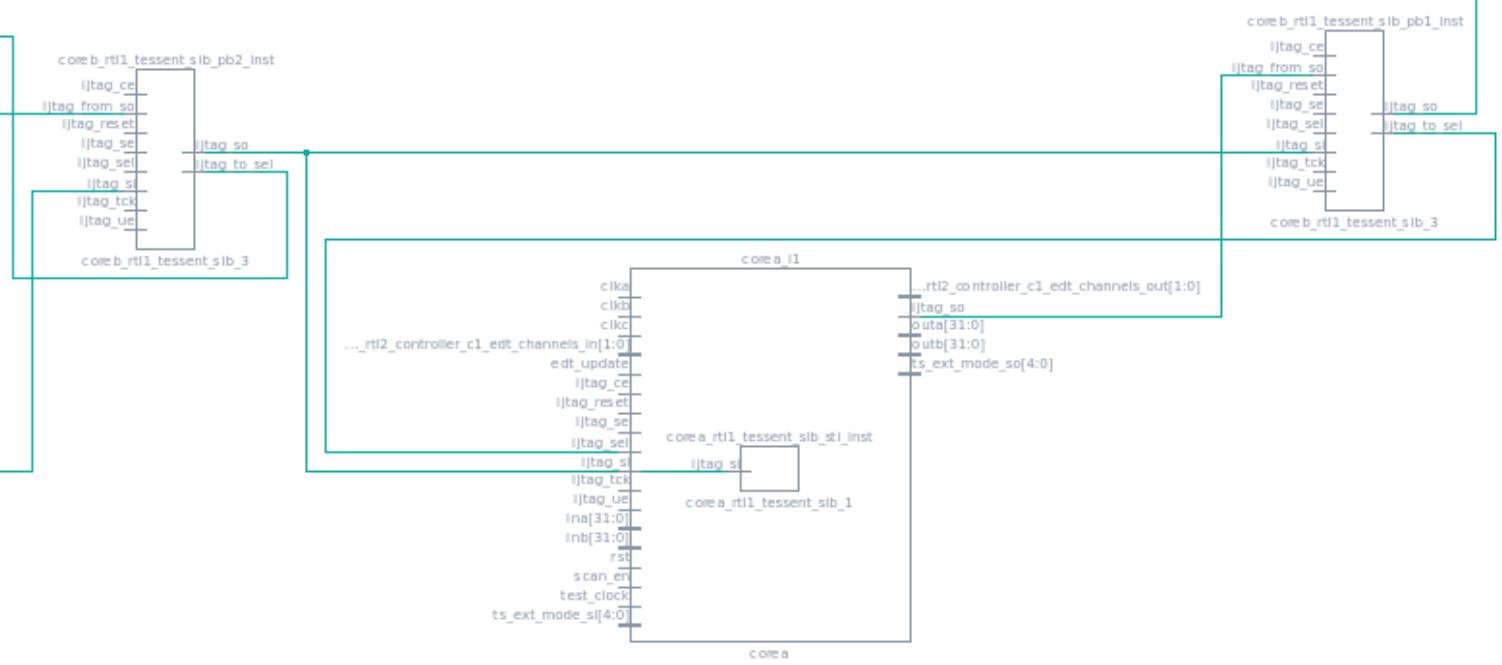
```

// Loading the generated RTL verilog files (1) to enable instantiating the contained modules
// into the design.
// Processing of EDT
// Generating design files for EDT Tdr module coreb_rtl2_tessent_edt_c1_tdr
// Verilog RTL : ../tsdb_outdir/instruments/coreb_rtl2_edt.instrument/coreb_rtl2_tessent_edt_c1_tdr.v
// IJTAG ICL   : ../tsdb_outdir/instruments/coreb_rtl2_edt.instrument/coreb_rtl2_tessent_edt_c1_tdr.icl
// Generating design files for EDT module coreb_rtl2_tessent_edt_c1
// Verilog RTL : ../tsdb_outdir/instruments/coreb_rtl2_edt.instrument/coreb_rtl2_tessent_edt_c1.v
// IJTAG ICL   : ../tsdb_outdir/instruments/coreb_rtl2_edt.instrument/coreb_rtl2_tessent_edt_c1.icl
// IJTAG PDL   : ../tsdb_outdir/instruments/coreb_rtl2_edt.instrument/coreb_rtl2_tessent_edt_c1.pdl
// TCD        : ../tsdb_outdir/instruments/coreb_rtl2_edt.instrument/coreb_rtl2_tessent_edt_c1.tcd
//
// Loading the generated RTL verilog files (2) to enable instantiating the contained modules
// into the design.
// --- Instrument insertion phase ---
// Inserting instruments of type 'ijtag'
// Inserting instruments of type 'occ'
// Inserting instruments of type 'edt'
// Running proc 'process_dft_specification.post_insertion' supplied by the user
//
// Writing out modified source design in ../tsdb_outdir/dft_inserted_designs/coreb_rtl2.dft_inserted_design
// Writing out specification in ../tsdb_outdir/dft_inserted_designs/coreb_rtl2.dft_spec
//
// Done processing of DftSpecification(coreb,rtl2)
//
// command: extract_icl
// Note: Updating the hierarchical data model to reflect RTL design changes.
// Writing design source dictionary : ../tsdb_outdir/dft_inserted_designs/coreb_rtl2.dft_inserted_design/coreb.design_source_dictionary
// -----
// Begin RTL synthesis.
// -----
// Synthesized modules=1, Time=1.59 sec.
// Note: There was 1 module selectively synthesized. There were also 3 sub-modules created by synthesis.
//       Use 'get_module -filter is_synthesized' to see them.
//
// You can also use 'set_quick_synthesis_options -verbose on' to have the synthesis step report the
// synthesized module name in the transcript as it is being synthesized.
// -----
// Warning: Rule FN1 violation occurs 1233 times
// Warning: Rule FN3 violation occurs 20 times
// Warning: Rule FN4 violation occurs 1355 times
// Warning: Rule FP13 violation occurs 139 times
// Flattening process completed, cell instances=6091, gates=16764, PIs=82, P0s=74, CPU time=0.11 sec.
// -----
// Begin circuit learning analyses.
// -----
// Learning completed, CPU time=0.01 sec.
// -----
// Begin ICL extraction.
// -----
// ICL extraction completed, ICL instances=23, CPU time=0.15 sec.
// -----
// -----
// Begin ICL elaboration and checking.
// -----
// ICL elaboration completed, CPU time=0.20 sec.
// -----
// Writing ICL file : ../tsdb_outdir/dft_inserted_designs/coreb_rtl2.dft_inserted_design/coreb.icl
// Writing consolidated PDL file: ../tsdb_outdir/dft_inserted_designs/coreb_rtl2.dft_inserted_design/coreb.pdl
//
// Writing SDC file: ../tsdb_outdir/dft_inserted_designs/coreb_rtl2.dft_inserted_design/coreb.sdc
// Writing DFT info dictionary: ../tsdb_outdir/dft_inserted_designs/coreb_rtl2.dft_inserted_design/coreb.dft_info_dictionary
// command: stop
// Error: Command 'stop' is unknown
// 'DOFile coreb dft rtl2.tcl' aborted at line 57

```

source ijttag_network.tcl





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For example if we do CoreB inttest and CoreA extest

- **SIB SRI of CoreB**
- **If SIB SRI is programmed with 1**
- **SIB STI is related to memories and SIB SRI is related to core logic control**

Step 3: Synthesis

```
1 sh mkdir -p -v outputs
2
3 set design_name coreb
4
5 ## Define the library files
6 set target_library "../../../../library/adk.db"
7 set link_library "../../../../library/adk.db" $target_library
8 read_db $target_library
9
10 # Bus naming style for Verilog
11 set bus_naming_style {%-s[%d]}
12
13 # Read input design files
14 source ../../insert_edt_occ/${design_name}.dc_shell_import_script
15
16 # Synthesize the top module
17 elaborate ${design_name}
18 set_size_only [get_cells tessent_persistent_cell_* -hier -filter {is_hierarchical==false}] -all_instances
19 link
20
21 # Check design for inconsistencies
22 check_design
23
24 # Timing specification
25 create_clock -period 10 -waveform {0 5} clka
26 create_clock -period 10 -waveform {0 5} clkb
27
28 # Avoid assign statements in the synthesized netlist.
29 set_fix_multiple_port_nets -feedthroughs -outputs -buffer_constants
30
31 # Compile design
32 uniquify
33 compile -map_effort medium
34
35 # Report design results for TOP design
36 report_area > outputs/${design_name}_dc_script_report.out
37 report_constraint -all_violators -verbose >> outputs/${design_name}_dc_script_report.out
38 report_timing -path full -delay max >> outputs/${design_name}_dc_script_report.out
39 report_reference >> outputs/${design_name}_dc_script_report.out
40
41 write -f verilog -hierarchy -o outputs/${design_name}_top_gate.v
42
43 sh rm *.syn *.pvl *.mr
44
45 exit
```

```
/home/vinayakp/aug23/level3/Lab4/coreb/3.synthesis>>dc_shell -f synthesis.tcl | tee syn_log
```

```
Design Compiler Graphical
    DC Ultra (TM)
    DFTMAX (TM)
Power Compiler (TM)
    DesignWare (R)
    DC Expert (TM)
Design Vision (TM)
HDL Compiler (TM)
VHDL Compiler (TM)
    DFT Compiler
Design Compiler(R)
```

```
Version S-2021.06-SP2 for linux64 - Aug 24, 2021
```

```
Copyright (c) 1988 - 2021 Synopsys, Inc.
```

```
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```

```
Note: Symbol # after min delay cost means estimated hold TNS across all active scenarios
```

```
Optimization Complete
-----
1
# Report design results for TOP design
report_area > outputs/${design_name}_dc_script_report.out
report_constraint -all_violators -verbose >> outputs/${design_name}_dc_script_report.out
report_timing -path full -delay max >> outputs/${design_name}_dc_script_report.out
report_reference >> outputs/${design_name}_dc_script_report.out
write -f verilog -hierarchy -o outputs/${design_name}_top_gate.v
Warning: Design 'coreb' has '2' unresolved references. For more detailed information, use the "link" command. (U ID-341)
Writing verilog file '/home/vinayakp/aug23/level3/Lab4/coreb/3.synthesis/outputs/coreb_top_gate.v'.
Warning: Verilog 'assign' or 'tran' statements are written out. (VO-4)
Warning: Verilog writer has added 5 nets to module coreb_rtl1_tessent_mbist_c1_controller using SYNOPSYS_UNCONNECTED as prefix. Please use the change_names command to make the correct changes before invoking the verilog writer. (VO-11)
1
sh rm *.syn *.pvl *.mr
exit

Memory usage for this session 148 Mbytes.
Memory usage for this session including child processes 148 Mbytes.
CPU usage for this session 19 seconds ( 0.01 hours ).
Elapsed time for this session 20 seconds ( 0.01 hours ).
```

```
Compiling source file ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tessent_sib_1.v
Compiling source file ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tessent_sib_2.v
Compiling source file ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tessent_sib_3.v
Compiling source file ../tsdb_outdir/instruments/coreb_rtl1_ijtag.instrument/coreb_rtl1_tessent_sib_4.v
Presto compilation completed successfully.
Running PRESTO HDLC
Compiling source file ../tsdb_outdir/instruments/coreb_rtl1_mbist.instrument/coreb_rtl1_tessent_mbist_bap.v
Compiling source file ../tsdb_outdir/instruments/coreb_rtl1_mbist.instrument/coreb_rtl1_tessent_mbist_cl_controller.v
Compiling source file ../tsdb_outdir/instruments/coreb_rtl1_mbist.instrument/coreb_rtl1_tessent_mbist_cl_interface_m1.v
Presto compilation completed successfully.
Running PRESTO HDLC
Compiling source file ../tsdb_outdir/instruments/coreb_rtl2_cells.instrument/coreb_rtl2_tessent_posedge_synchronizer_reset.v
Presto compilation completed successfully.
Running PRESTO HDLC
Compiling source file ../tsdb_outdir/instruments/coreb_rtl2_ijtag.instrument/coreb_rtl2_tessent_sib_1.v
Compiling source file ../tsdb_outdir/instruments/coreb_rtl2_ijtag.instrument/coreb_rtl2_tessent_tdr_sri_ctrl.v
Presto compilation completed successfully.
Running PRESTO HDLC
Compiling source file ../tsdb_outdir/instruments/coreb_rtl2_occ.instrument/coreb_rtl2_tessent_occ.v
Presto compilation completed successfully.
Running PRESTO HDLC
Compiling source file ../tsdb_outdir/instruments/coreb_rtl2_edt.instrument/coreb_rtl2_tessent_edt_c1.v
Compiling source file ../tsdb_outdir/instruments/coreb_rtl2_edt.instrument/coreb_rtl2_tessent_edt_c1_tdr.v
Presto compilation completed successfully.
I
# Synthesize the top module
elaborate ${design_name}
Running PRESTO HDLC
```

Step 4: Scan Insertion

```
1 set_context dft -scan -design_id gate -hier
2 set_tsdb_output_directory ../tsdb_outdir
3 open_tsdb ../../Lab3/corea/tsdb_outdir
4
5 read_design corea -design_id gate -view graybox -verbose
6 read_verilog ../synthesis/outputs/coreb_top_gate.v
7 read_design coreb -design_id rtl2 -icl_only -verbose
8
9 read_cell_library ../../library/adk.tcelllib
10 read_verilog ../../library/mems/SYNC_1R1W_16x8.v -exclude_from_file_dictionary
11
12
13 set_current_design coreb
14
15 set_static_dft_signal_values ext_mode 1 -icl_instances corea_i1
16 set_static_dft_signal_values ext_mode 1 -icl_instances corea_i2
17 set_static_dft_signal_values ext_mode 1 -icl_instances corea_i3
18 set_static_dft_signal_values ext_mode 1 -icl_instances corea_i4
19 set_static_dft_signal_values ltest_en 1
20
21 check_design_rules
22
23
24 set_wrapper_analysis_options -exclude_ports [get_ports *edt_channel*]
25 set_dedicated_wrapper_cell_options on -ports rst
26
27 analyze_wrapper_cells
28
29 add_scan_mode int_mode -edt_instances coreb_rtl2_tessent_edt_c1_inst
30
31 ## Stitching OCC bits in wrapper chains.
32 set wrapper_cells_occ_bits [get_scan_elements -class wrapper]
33 append_to_collection wrapper_cells_occ_bits [get_scan_elements coreb.*occ*]

34 add_scan_mode ext_mode -chain_length 32 -include_elements $wrapper_cells_occ_bits
35 analyze_scan_chains
36
37 insert_test_logic
38
39
40 set_context patterns -scan
41
42 set tck_port [get_single_name [get_icl_port -filter ijtag_function==tck]]
43 foreach_in_collection mode_wrapper [get_config_elements Core(coreb)/Scan/Mode -part tcd -silent] {
44   set mode_name [get_config_value $mode_wrapper -id <0>]
45   set mode_type [get_config_value type -in $mode_wrapper]
46   import_scan_mode $mode_name
47   check_design_rules
48   if {$mode_type eq "external"} {
49     report_scan_cells
50     analyze_graybox
51     write_design -tsdb -graybox
52   }
53   set_system_mode setup
54
55 }
```

```

/home/vinayakp/aug23/level3/Lab4/coreb/4.scan_insertion>>tessent -shell -dofile coreb_dft_gate.tcl
// Warning: Tessent user documentation not found
// Tessent Shell 2021.1 Fri Feb 26 20:45:56 GMT 2021
// Copyright 2011-2021 Mentor Graphics Corporation
//
// All Rights Reserved.
//
// THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION WHICH
// IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS AND IS
// SUBJECT TO LICENSE TERMS.
//
// Mentor Graphics software executing under x86-64 Linux on Sun Feb 11 22:37:42 IST 2024.
// 64 bit version
// Host: vlsiguru (64168 MB RAM, 32191 MB Swap)
//
// command: set_context dft -scan -design_id gate -hier
// command: set_tsdb_output_directory ../tsdb_outdir
// command: open_tsdb ../../Lab3/corea/tsdb_outdir
// command: read_design corea -design_id gate -view graybox -verbose
// sub-command: set_read_design_tag corea
// sub-command: read_verilog ../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted_design/corea.vg_graybox -no_duplicate_modules_warnings
// sub-command: set_read_design_tag ""
// sub-command: read_icl ../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted_design/corea.icl -no_notes
// sub-command: source ../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted_design/corea.pdl
// sub-command: read_core_descriptions ../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted_design/corea.tcd
// command: read_verilog ./3.synthesis/outputs/coreb_top_gate.v
// command: read_design coreb -design_id rtl2 -icl_only -verbose
// sub-command: read_icl ./tsdb_outdir/dft_inserted_designs/coreb_rtl2.dft_inserted_design/coreb.icl -skip_chi
ld_blocks -no_notes

// sub-command: source ./tsdb_outdir/dft_inserted_designs/coreb_rtl2.dft_inserted_design/coreb.pdl
// sub-command: read_core_descriptions ./tsdb_outdir/dft_inserted_designs/coreb_rtl2.dft_inserted_design/coreb.tcd
// command: read_cell_library ../../library/adk.tcelllib
// Reading DFT Library file ../../library/adk.tcelllib
// Finished reading file ../../library/adk.tcelllib
// command: read_verilog ../../library/mems/SYNC_1R1W_16x8.v -exclude_from_file_dictionary
// Warning: File: ../../library/mems/SYNC_1R1W_16x8.v, Line: 2: Module 'SYNC_1R1W_16x8' includes RTL constr
ucts that are discarded since the tool is expecting a gate-level design. This module therefore cannot be modifie
d, and will be omitted when the design is written out.
// command: set_current_design coreb
// Warning: 97 cases: Undriven net in netlist module
// Warning: 123 cases: Floating input on instance in netlist
// Warning: 174 cases: Net in netlist not connected
// Note: Issue set_current_design with the -show_elaboration_warnings option to see more details about previous
warnings
// -----
// Begin ICL elaboration and checking.
// -----
// ICL elaboration completed, CPU time=0.19 sec.
// -----
// Reading core description file ../../Lab3/corea/tsdb_outdir/instruments/corea_rtl2_edt.instrument/corea_rt
l2_tessent_edt_c1.tcd
// Warning: Primary input 'tessent_persistent_cell_shift_capture_clock/GCK_pport' is added at pin '/tessent_per
sistent_cell_shift_capture_clock/GCK'
// Note: Specified test clock connection point tessent_persistent_cell_shift_capture_clock/GCK will be mapped t
o internal clock tessent_persistent_cell_shift_capture_clock/GCK_pport
// command: set_static_dft_signal_values ext_mode 1 -icl_instances corea_i1
// command: set_static_dft_signal_values ext_mode 1 -icl_instances corea_i2
// command: set_static_dft_signal_values ext_mode 1 -icl_instances corea_i3
// command: set_static_dft_signal_values ext_mode 1 -icl_instances corea_i4
// command: set_static_dft_signal_values ltest_en 1

```

```
// command: check_design_rules
// Warning: Rule FN1 violation occurs 284 times
// Warning: Rule FN3 violation occurs 20 times
// Warning: Rule FN4 violation occurs 1978 times
// Warning: Rule FP13 violation occurs 123 times
// Flattening process completed, cell instances=11103, gates=21222, PIs=82+5(pseudo ports), P0s=74, CPU time=0.
10 sec.
//
// -----
// Begin circuit learning analyses.
// -----
// Learning completed, CPU time=0.06 sec.
//
// -----
// Begin scan chain identification process, memory elements = 1978,
sequential library cells = 1978.
//
// -----
// Begin simulation of test_setup procedure with 233 cycles.
// Simulation of test_setup procedure completed, CPU time=0.0 sec.
// Begin simulation of auto-generated load_unload procedure.
// Simulation of load_unload procedure completed, CPU time=0.0 sec.
// Scan segment = ext_mode/corea_i1/ts_ext_mode_so[4] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i1/ts_ext_mode_so[3] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i1/ts_ext_mode_so[2] successfully traced with scan_cells = 28.
// Scan segment = ext_mode/corea_i1/ts_ext_mode_so[1] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i1/ts_ext_mode_so[0] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i2/ts_ext_mode_so[4] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i2/ts_ext_mode_so[3] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i2/ts_ext_mode_so[2] successfully traced with scan_cells = 28.
// Scan segment = ext_mode/corea_i2/ts_ext_mode_so[1] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i2/ts_ext_mode_so[0] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i3/ts_ext_mode_so[4] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i3/ts_ext_mode_so[3] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i3/ts_ext_mode_so[2] successfully traced with scan_cells = 28.
// Scan segment = ext_mode/corea_i3/ts_ext_mode_so[1] successfully traced with scan_cells = 27.
// Scan segment = ext mode/corea i3/ts ext mode so[2] successfully traced with scan cells = 28.

// Scan segment = ext_mode/corea_i3/ts_ext_mode_so[1] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i3/ts_ext_mode_so[0] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i4/ts_ext_mode_so[4] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i4/ts_ext_mode_so[3] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i4/ts_ext_mode_so[2] successfully traced with scan_cells = 28.
// Scan segment = ext_mode/corea_i4/ts_ext_mode_so[1] successfully traced with scan_cells = 27.
// Scan segment = ext_mode/corea_i4/ts_ext_mode_so[0] successfully traced with scan_cells = 27.
// Scan segment = /coreb_rtl1_tessent_sib_sti_inst/ltest_so successfully traced with scan_cells = 7.
// Scan segment = /coreb_rtl2_tessent_occ_clkc_inst/scan_out successfully traced with scan_cells = 3.
// Scan segment = /coreb_rtl2_tessent_occ_clkb_inst/scan_out successfully traced with scan_cells = 3.
// Scan segment = /coreb_rtl2_tessent_occ_clka_inst/scan_out successfully traced with scan_cells = 3.
// 3 external shadows that use shift clocking have been identified.
// 560 scan cells have been identified in 24 scan segments.
// Longest scan segment has 28 scan cells.
// Warning: 4 edge-triggered clock ports set to stable high. (D7)
// Warning: Model 'nlatch' has no muxscan scan equivalent and is treated as nonscan model
// Warning: Model 'latch' has no muxscan scan equivalent and is treated as nonscan model
//
// -----
// 929 sequential library cells are treated as non-scan.
// -----
// 6 sequential library cells missing mux-scan equivalent.
// 835 sequential library cells below hard module.
// 88 sequential library cells defined non-scan.
// -----
// Begin scannability rules checking for 451 sequential library cells
and 24 scan segments. The scan segments contain 598 additional cells.
// -----
// 451 sequential library cells and 24 scan segments identified as scannable.
// -----
// Begin transparent latch checking for 93 latches.
// -----
// Warning: 4 latches not transparent due to all clocks off. (D6)
```

```
// Warning: 29 latches not transparent due to unobservable. (D6)
// Number transparent latches = 60.
//
// Begin scan clock rules checking.
//
// 10 scan clock/set/reset lines have been identified.
// All scan clocks successfully passed off-state check.
// 717 sequential cells passed clock stability checking.
// There were 135 clock rule C3 fails (clock may capture data affected by its captured data).
// Note: Trailing edge triggered device can capture data affected by leading edge.
//
// 960 non-scan memory elements are identified.
//
// 323 non-scan memory elements are identified as TIE-0. (D5)
// 87 non-scan memory elements are identified as TIE-1. (D5)
// 29 non-scan memory elements are identified as TIE-X. (D5)
// 24 non-scan memory elements are identified as INIT-0. (D5)
// 437 non-scan memory elements are identified as INIT-X. (D5)
// 60 non-scan memory elements are identified as TLA. (D5)
//
// Begin shift register identification for 451 sequential library cells.
//
// Number of shift register flops recorded for scan insertion: 21 (1.06%)
// Number of shift registers recorded for scan insertion: 10
// Longest shift register has 3 flops.
// Shortest shift register has 2 flops.
// Potential number of nonscan flops to be converted to scan cells: 10
// Potential number of scan cells to be converted to nonscan flops: 0
// Number of targeted sequential library cells = 451
// command: set_wrapper_analysis_options -exclude_ports [get_ports *edt_channel*]
// command: set_dedicated_wrapper_cell_options on -ports rst

// command: analyze_wrapper_cells
//
// Port information and user constraints:
//
//      Input ports:    82 total,     13 ignored,      4 excluded,      0 off,      1 on,      64 auto
//      Output ports:   74 total,     1 ignored,      9 excluded,      0 off,      0 on,      64 auto
//
// Wrapper analysis summary:
//
//      0 output ports required a dedicated wrapper cell.
//      1 input port required a dedicated wrapper cell.
//      64 flip-flops were converted into output shared wrapper cells.
//      64 flip-flops were converted into input shared wrapper cells.
//      Use report_wrapper_cells for more details.
//
// command: add_scan_mode int_mode -edt_instances coreb_rtl2_tessent_edt_c1_inst
// Reading core description file ../tsdb_outdir/instruments/coreb_rtl2_edt.instrument/coreb_rtl2_tessent_edt_c1.tcd
// Setting the chain count to the number of specified scan connections (15).
// Automatically inferring '-enable_dft_signal int_mode' from the specified scan mode name.
// Automatically inferring '-type internal' from the scan mode type (internal) associated with the enable DFT signal 'int_mode'.
// command: ## Stitching OCC bits in wrapper chains.
// command: set wrapper_cells_occ_bits [get_scan_elements -class wrapper]
// command: append_to_collection wrapper_cells_occ_bits [get_scan_elements coreb.*occ*]
// command: add_scan_mode ext_mode -chain_length 32 -include_elements $wrapper_cells_occ_bits
// Automatically inferring '-enable_dft_signal ext_mode' from the specified scan mode name.
// Automatically inferring '-type external' from the scan mode type (external) associated with the enable DFT signal 'ext_mode'.
```

```

// command: analyze_scan_chains
// Warning: Scan element '/coreb_rtl2_tessent_occ_clkc_inst/scan_out' of class 'core' was specified in the population of external mode 'ext_mode'.
Distribution - analyzing elements: 0.0% completed (estimated time remaining 0 secs)// Warning: Scan element '/coreb_rtl2_tessent_occ_clkb_inst/scan_out' of class 'core' was specified in the population of external mode 'ext_mode'.
// Warning: Scan element '/coreb_rtl2_tessent_occ_clka_inst/scan_out' of class 'core' was specified in the population of external mode 'ext_mode'.
// Chain allocation of 'int_mode' mode completed:
Distribution - populating 'int_mode' chains: 94.0% completed (estimated time remaining 0 secs) 15 distributed chains of sizes ranging from 67 to 68
// Chain allocation of 'ext_mode' mode completed:
Distribution - populating 'ext_mode' chains: 100.0% completed (estimated time remaining 0 secs) 5 distributed chains of sizes ranging from 28 to 29
// command: insert_test_logic
Validation - checking node equations: 8.0% completed (estimated time remaining 0 secs)Validation - checking node equations: 8.0% completed (estimated time remaining 0 secs)Validation - checking node equations: 0.0% completed
=====
Test Logic Insertion Summary:
=====

Structural Data:
-----
      Added top-level port count: 2
      Added instance count: 209

Logical Data:
-----
      Added input wrapper logic count: 65
      Added output wrapper logic count: 64
      Added pipelining logic count: 4
      Added retiming logic count: 25
      Added scan chain count (int_mode): 15
      Added scan chain count (ext_mode): 5

// Warning: Flattened model deleted.
//
// Writing out netlist and related files in ../tsdb_outdir/dft_inserted_designs/coreb_gate.dft_inserted_design

// command: stop
// Error: Command 'stop' is unknown
// 'DOFile coreb dft gate.tcl' aborted at line 37

```

```

INSERTION> set_system_mode analysis
// Error: Changing system mode from insertion mode to analysis mode is prohibited.
// You have to switch to setup mode first.
INSERTION> set_attribute_value [get_module -of_type design] -name synthesize_before_analysis
{SYNC_1R1W_16x8 corea corea_rtl1_tessent_sib_1 corea_rtl2_tessent_edt_c1 corea_rtl2_tessent_edt_c1_bypass_logic
corea_rtl2_tessent_edt_c1_compactor corea_rtl2_tessent_edt_c1_controller corea_rtl2_tessent_edt_c1_decompressor
corea_rtl2_tessent_edt_c1_onehot_decoder_3_to_7 corea_rtl2_tessent_edt_c1_onehot_decoder_4_to_8 corea_rtl2_tesse
nt_edt_c1_spatial_compactor_7_w_output_lockup corea_rtl2_tessent_edt_c1_spatial_compactor_8_w_output_lockup core
a_rtl2_tessent_edt_c1_tdr corea_rtl2_tessent_edt_c1_xor_decoder corea_rtl2_tessent_occ_0 corea_rtl2_tessent_occ_
1 corea_rtl2_tessent_occ_2 corea_rtl2_tessent_occ_control_0 corea_rtl2_tessent_occ_control_1 corea_rtl2_tessent_
occ_control_2 corea_rtl2_tessent_occ_shift_reg_0 corea_rtl2_tessent_occ_shift_reg_1 corea_rtl2_tessent_occ_shift_
reg_2 corea_rtl2_tessent_occ_sib_0 corea_rtl2_tessent_occ_sib_1 corea_rtl2_tessent_occ_sib_2 corea_rtl2_tessent_
posedge_synchronizer_reset_0 corea_rtl2_tessent_posedge_synchronizer_reset_1 corea_rtl2_tessent_posedge_synchron
izer_reset_2 corea_rtl2_tessent_sib_1 corea_rtl2_tessent_sib_2_0 corea_rtl2_tessent_sib_2_1 corea_rtl2_tessent_
tdr_sri_ctrl corea_ts_graybox corea_DW01_dec_0_1 corea_ts_graybox_corea_DW01_inc_0_1 corea_ts_graybox_corea_DW01_
inc_1_1 corea_ts_graybox_corea_gate_tessent_input_wrapper_hold_scan_cell_p_1 corea_ts_graybox_corea_gate_tessen
t_input_wrapper_hold_scan_cell_p_1_1 corea_ts_graybox_corea_gate_tessent_input_wrapper_hold_scan_cell_p_2_1 core
a_ts_graybox_corea_gate_tessent_output_wrapper_hold_scan_cell_p_1 corea_ts_graybox_corea_rtl1_tessent_mbist_bap_
1 corea_ts_graybox_corea_rtl1_tessent_mbist_bap_tdr_1 coreb coreb_DW01_add_10 coreb_DW01_add_11 coreb_DW01_add_1
2 coreb_DW01_add_13 coreb_DW01_add_7 coreb_DW01_add_8 coreb_DW01_add_9 ...}
INSERTION> set_attribute_value qcsram* -name preserve_boundary -silent
INSERTION> set_attribute_value qcrf* -name preserve_boundary -silent
INSERTION> set_system_mode analysis
// Error: Changing system mode from insertion mode to analysis mode is prohibited.
// You have to switch to setup mode first.
INSERTION> set sys m setup
SETUP> source
RUNME           coreb_dft_gate.tcl log          schematic.tcl
SETUP> source schematic.tcl

```



```
// Warning: Flattened model deleted.  
//  
// Writing out netlist and related files in ../tsdb_outdir/dft_inserted_designs/coreb_gate.dft_inserted_design  
  
// command: set_context patterns -scan  
// command: set_tck_port [get_single_name [get_icl_port -filter ijtag_function==tck]]  
// command: foreach_in_collection mode_wrapper [get_config_elements Core(coreb)/Scan/Mode -part tcd -silent] {  
set mode_name [get_config_value $mode_wrapper -id <0>]  
set mode_type [get_config_value type -in $mode_wrapper]  
import_scan_mode $mode_name  
check_design_rules  
if {$mode_type eq "external"} {  
    report_scan_cells  
    analyze_graybox  
    write_design -tsdb -graybox  
}  
set_system_mode setup  
}  
// sub-command: import_scan_mode int_mode  
// Resetting design.  
// Warning: The current mode name was not specified and will be set to 'int_mode'.  
// Different ATPG configurations should use different mode names, otherwise  
// they will overwrite each other in the TSDB when 'write_tsdb_data -replace' is called.  
// If you will have multiple ATPG configurations for this scan mode of this design,  
// use the 'set_current_mode' command to change the current mode name.  
// Reading core description file ../tsdb_outdir/instruments/coreb_rtl2_occ.instrument/coreb_rtl2_tessent_occ.tcd  
  
// sub-command: check_design_rules  
// Warning: Rule FN1 violation occurs 285 times  
// Warning: Rule FN4 violation occurs 2007 times  
// Warning: Rule FP13 violation occurs 103 times  
// Flattening process completed, cell instances=11311, gates=21816, PIs=87+4(pseudo ports), P0s=79, CPU time=0.10 sec.  
// -----  
// Begin circuit learning analyses.  
// -----  
// Learning completed, CPU time=0.07 sec.  
// -----  
// Begin scan chain identification process, memory elements = 2007.  
// -----  
// Begin simulation of test_setup procedure with 189 cycles.  
// Simulation of test_setup procedure completed, CPU time=0.0 sec.  
// Begin simulation of load_unload procedure.  
// Simulation of load_unload procedure completed, CPU time=0.2 sec.  
// -----  
// Begin EDT Finder analyses.  
// -----  
// Finding EDT logic.  
// Finding internal scan chains.  
// EDT Finder completed, EDT blocks=1, scan chains=15, CPU time=0.02 sec.  
// -----
```

```

// Chain = coreb_rtl2_tessent_edt_c1_inst_chain_1 successfully traced with scan_cells = 68.
// Chain = coreb_rtl2_tessent_edt_c1_inst_chain_2 successfully traced with scan_cells = 68.
// Chain = coreb_rtl2_tessent_edt_c1_inst_chain_3 successfully traced with scan_cells = 68.
// Chain = coreb_rtl2_tessent_edt_c1_inst_chain_4 successfully traced with scan_cells = 68.
// Chain = coreb_rtl2_tessent_edt_c1_inst_chain_5 successfully traced with scan_cells = 68.
// Chain = coreb_rtl2_tessent_edt_c1_inst_chain_6 successfully traced with scan_cells = 68.
// Chain = coreb_rtl2_tessent_edt_c1_inst_chain_7 successfully traced with scan_cells = 68.
// Chain = coreb_rtl2_tessent_edt_c1_inst_chain_8 successfully traced with scan_cells = 67.
// Chain = coreb_rtl2_tessent_edt_c1_inst_chain_9 successfully traced with scan_cells = 67.
// Chain = coreb_rtl2_tessent_edt_c1_inst_chain_10 successfully traced with scan_cells = 67.
// Chain = coreb_rtl2_tessent_edt_c1_inst_chain_11 successfully traced with scan_cells = 67.
// Chain = coreb_rtl2_tessent_edt_c1_inst_chain_12 successfully traced with scan_cells = 67.
// Chain = coreb_rtl2_tessent_edt_c1_inst_chain_13 successfully traced with scan_cells = 67.
// Chain = coreb_rtl2_tessent_edt_c1_inst_chain_14 successfully traced with scan_cells = 67.
// Chain = coreb_rtl2_tessent_edt_c1_inst_chain_15 successfully traced with scan_cells = 67.
// 8 external shadows that use shift clocking have been identified.
// 1012 scan cells have been identified in 15 scan chains.
// Longest scan chain has 68 scan cells.
// Warning: 36 edge-triggered clock ports set to stable high. (D7)
// -----
// Begin EDT setup and rules checking.
// -----
// Running EDT Pattern Generation Phase.
// Warning: The longest chain (68 cells) is longer than the specified range (10 - 50) for longest chain. This
may decrease coverage (if EDT aborts exist) and/or effective compression.
// EDT setup and rules checking completed, CPU time=0.05 sec.
// -----
// Begin transparent latch checking for 91 latches.
// -----
// Warning: 6 latches not transparent due to uncontrollable. (D6)
// Warning: 20 latches not transparent due to unobservable. (D6)
// Number transparent latches = 65.

// Begin scan clock rules checking.
// -----
// 6 scan clock/set/reset lines have been identified.
// Note: 685 scan cells whose clock ports are not off when all clocks are off will be handled through additional
ATPG effort.
// These scan cells have been excluded from default C1 violation list. Use "report_drc_rules C1 -excluded"
to report such C1 violations.
// 416 sequential cells passed clock stability checking.
// There were 25 clock rule C3 fails (clock may capture data affected by its captured data).
// Warning: There were 3 clock rule C4 fails (clock may be affected by its captured data).
// Warning: There were 4 clock rule C7 fails (scan cell capture ability check).
// Warning: There were 278 clock rule C7 fails (nonscan cell capture ability check).
// Note: Trailing edge triggered device can capture data affected by leading edge.
// -----
// 982 non-scan memory elements are identified.
// -----
// 370 non-scan memory elements are identified as TIE-0. (D5)
// 87 non-scan memory elements are identified as TIE-1. (D5)
// 32 non-scan memory elements are identified as TIE-X. (D5)
// 3 non-scan memory elements are identified as INIT-0. (D5)
// 425 non-scan memory elements are identified as INIT-X. (D5)
// 65 non-scan memory elements are identified as TLA. (D5)
// -----
// Analysis recommends using "set_split_capture on". It is currently turned off (default value).
// sub-command: set_system_mode setup
// sub-command: import_scan_mode ext_mode
// Resetting design.
// Warning: The current mode name was not specified and will be set to 'ext_mode'.
// Different ATPG configurations should use different mode names, otherwise
// they will overwrite each other in the TSDB when 'write_tsdb_data -replace' is called.
// If you will have multiple ATPG configurations for this scan mode of this design,

```

```

//      use the 'set_current_mode' command to change the current mode name.
// sub-command: check_design_rules
// Warning: Rule FN1 violation occurs 285 times
// Warning: Rule FN4 violation occurs 2007 times
// Warning: Rule FP13 violation occurs 103 times
// Flattening process completed, cell instances=11311, gates=21747, PIs=87+3(pseudo ports), P0s=79, CPU time=0.
12 sec.
// -----
// Begin circuit learning analyses.
// -----
// Learning completed, CPU time=0.06 sec.
// -----
// Begin scan chain identification process, memory elements = 2007.
// -----
// Begin simulation of test_setup procedure with 188 cycles.
// Simulation of test_setup procedure completed, CPU time=0.0 sec.
// Begin simulation of load_unload procedure.
// Simulation of load_unload procedure completed, CPU time=0.1 sec.
// Note: Skipping EDT Finder, since no EDT decompressors defined
// Chain = ext_mode_chain1 successfully traced with scan_cells = 28.
// Chain = ext_mode_chain2 successfully traced with scan_cells = 28.
// Chain = ext_mode_chain3 successfully traced with scan_cells = 29.
// Chain = ext_mode_chain4 successfully traced with scan_cells = 28.
// Chain = ext_mode_chain5 successfully traced with scan_cells = 29.
// 2 external shadows that use shift clocking have been identified.
// 142 scan cells have been identified in 5 scan chains.
// Longest scan chain has 29 scan cells.
// Warning: 3 edge-triggered clock ports set to stable high. (D7)
// -----
// Begin transparent latch checking for 94 latches.
// -----
// Warning: 4 latches not transparent due to all clocks off. (D6)

// Warning: 20 latches not transparent due to unobservable. (D6)
// Number transparent latches = 70.
// -----
// Begin scan clock rules checking.
// -----
// 5 scan clock/set/reset lines have been identified.
// All scan clocks successfully passed off-state check.
// 611 sequential cells passed clock stability checking.
// There were 22 clock rule C3 fails (clock may capture data affected by its captured data).
// Warning: There were 3 clock rule C4 fails (clock may be affected by its captured data).
// Warning: There were 334 clock rule C7 fails (nonscan cell capture ability check).
// Note: Trailing edge triggered device can capture data affected by leading edge.
// -----
// 1860 non-scan memory elements are identified.
// -----
// 371 non-scan memory elements are identified as TIE-0. (D5)
// 85 non-scan memory elements are identified as TIE-1. (D5)
// 26 non-scan memory elements are identified as TIE-X. (D5)
// 3 non-scan memory elements are identified as INIT-0. (D5)
// 1305 non-scan memory elements are identified as INIT-X. (D5)
// 70 non-scan memory elements are identified as TLA. (D5)
// -----
// Analysis recommends using "set_split_capture on". It is currently turned off (default value).
// sub-command: report_scan_cells
cell#      chain      memory_type      inv      gate#          shift_clock
                inv      cell_name                      instance_name
(ext. pin names)
----- ----- ----- ----- ----- ----- ----- ----- ----- ----- ----- -----
```

```

0      ext_mode_chain1 MASTER  (FF-LE)  FFFF    19686 /coreb_rtl2_tessent_occ_clkb_inst_tessent_persistent_ce
ll_clock_out_mux_Y F     sff      /\ffb4_reg[13]          ""
(SI,Q)
                               TLA   (LA-AL)  ----  21646 /coreb_rtl2_tessent_occ_clkb_inst_tessent_persistent_ce
ll_clock_out_mux_Y T     nlatch   /\ts_1_lockup_latchn_clkc21_intno108_i          ""
(-,-)
1      ext_mode_chain1 MASTER  (FF-LE)  FFFF    19685 /coreb_rtl2_tessent_occ_clkb_inst_tessent_persistent_ce
ll_clock_out_mux_Y F     sff      /\ffb4_reg[14]          ""
(SI,Q)
2      ext_mode_chain1 MASTER  (FF-LE)  FFFF    19684 /coreb_rtl2_tessent_occ_clkb_inst_tessent_persistent_ce
ll_clock_out_mux_Y F     sff      /\ffb4_reg[15]          ""
(SI,Q)
3      ext_mode_chain1 MASTER  (FF-LE)  FFFF    19683 /coreb_rtl2_tessent_occ_clkb_inst_tessent_persistent_ce
ll_clock_out_mux_Y F     sff      /\ffb4_reg[16]          ""
(SI,Q)
4      ext_mode_chain1 MASTER  (FF-LE)  FFFF    19682 /coreb_rtl2_tessent_occ_clkb_inst_tessent_persistent_ce
ll_clock_out_mux_Y F     sff      /\ffb4_reg[17]          ""
(SI,Q)
5      ext_mode_chain1 MASTER  (FF-LE)  FFFF    19681 /coreb_rtl2_tessent_occ_clkb_inst_tessent_persistent_ce
ll_clock_out_mux_Y F     sff      /\ffb4_reg[18]          ""
(SI,Q)
6      ext_mode_chain1 MASTER  (FF-LE)  FFFF    19680 /coreb_rtl2_tessent_occ_clkb_inst_tessent_persistent_ce
ll_clock_out_mux_Y F     sff      /\ffb4_reg[19]          ""
(SI,Q)
7      ext_mode_chain1 MASTER  (FF-LE)  FFFF    19679 /coreb_rtl2_tessent_occ_clkb_inst_tessent_persistent_ce
ll_clock_out_mux_Y F     sff      /\ffb4_reg[20]          ""
(SI,Q)
8      ext_mode_chain1 MASTER  (FF-LE)  FFFF    19678 /coreb_rtl2_tessent_occ_clkb_inst_tessent_persistent_ce
ll_clock_out_mux_Y F     sff      /\ffb4_reg[21]          ""
(SI,Q)
9      ext_mode_chain1 MASTER  (FF-LE)  FFFF    19677 /coreb_rtl2_tessent_occ_clkb_inst_tessent_persistent_ce
ll_clock_out_mux_Y F     sff      /\ffb4_reg[22]          ""
(SI,Q)
10     ext_mode_chain1 MASTER  (FF-LE)  FFFF    19676 /coreb_rtl2_tessent_occ_clkb_inst_tessent_persistent_ce
ll_clock_out_mux_Y F     sff      /\ffb4_reg[23]          ""
(SI,Q)
26     ext_mode_chain5 MASTER  (FF-LE)  FFFF    19885 /coreb_rtl2_tessent_occ_clka_inst_tessent_persistent_ce
ll_clock_out_mux_Y F     sff      /\ffa1_reg[3]          ""
(SI,Q)
27     ext_mode_chain5 MASTER  (FF-LE)  FFFF    21644 /coreb_rtl2_tessent_occ_clkc_inst_tessent_persistent_ce
ll_clock_out_mux_Y F     sff      /\ts_1_dihw_1927smodp1_i/\ts_1_logic_2000fsffp1_i          ""
(SI,Q)
                               TLA   (LA-AL)  ----  21664 /coreb_rtl2_tessent_occ_clkc_inst_tessent_persistent_ce
ll_clock_out_mux_Y T     nlatch   /\ts_1_lockup_latchn_clkc1_intno1928_i          ""
(-,-)
28     ext_mode_chain5 MASTER  (FF-LE)  FFFF    21668 /coreb_rtl2_tessent_occ_clkc_inst_tessent_persistent_ce
ll_clock_out_mux_Y F     sff      /\ts_1_pipeline_fsffp_clkc1_lo0l4_extsi1948_sea0_i          ""
(SI,Q)

// sub-command: analyze_graybox
// The 'in_graybox' attribute has been set for 4266 design instances (37.13% of 11489 total design instances).
// 3686 (32.08%) instances were identified in ICL scan resource instruments.

// 18 (0.16%) instances were identified in the logic from the preserved instances to other preserved instances, wrapper chains, and design boundary.
// 562 (4.89%) instances were identified in the wrapper chains and the logic from the wrapper chains to the design boundary.
// sub-command: write_design -tsdb -graybox
// Writing out graybox netlist and related files in ../tsdb_outdir/dft_inserted_designs/coreb_gate.dft_inserted_design
// sub-command: set_system_mode setup

```

Step 5. ATPG

Intest:

```
1 set_context patterns -scan
2 set_tsdb_output_directory ../../tsdb_outdir
3
4 read_cell_library ../../library/adk.tcelllib
5 read_verilog ../../library/mems/SYNC_1R1W_16x8.v -interface_only
6
7 open_tsdb ../../Lab3/corea/tsdb_outdir
8 read_design corea -design_id gate -view graybox -verbose
9 read_design coreb -design_id gate
10 set_current_design coreb
11 set_current_mode edt_stuck_intest -type internal
12 import_scan_mode int_mode -fast_capture_mode off
13
14 set_static_dft_signal_values ext_mode 1 -instance corea_i1
15 set_static_dft_signal_values ext_mode 1 -instance corea_i2
16 set_static_dft_signal_values ext_mode 1 -instance corea_i3
17 set_static_dft_signal_values ext_mode 1 -instance corea_i4
18
19 check_design_rules
20 set_fault_type stuck
21
22 add_faults -all
23
24
25 create_patterns
26 write_tsdb_data -replace
27
28 system mkdir -p -v simulations
29
30
31 write_patterns /hdd2/home/vidishar/aug23/level3/Lab4/coreb/5.atpg/sa/intest/simulations/coreb_int_mode_parallel.v -verilog -parallel -replace -parameter_list {SIM_TOP_NAME parallel_TB SIM_KEEP_PATH 1 SIM_STATUS_MSG 1}
32 exit
```

Statistics Report
Stuck-at Faults

Fault Classes	#faults (total)	#faults (total relevant)
FU (full)	81114	61475
UO (unobserved)	17 (0.02%)	same (0.03%)
DS (det_simulation)	37435 (46.15%)	same (60.89%)
DI (det_implication)	13523 (16.67%)	same (22.00%)
PU (posdet_untestable)	3 (0.00%)	same (0.00%)
PT (posdet_testable)	60 (0.07%)	same (0.10%)
UU (unused)	5678 (7.00%)	same (9.24%)
TI (tied)	240 (0.30%)	same (0.39%)
BL (blocked)	140 (0.17%)	same (0.23%)
RE (redundant)	369 (0.45%)	same (0.60%)
AU (atpg_untestable)	23649 (29.16%)	4010 (6.52%)

Fault Sub-classes
AU (atpg_untestable)
UDN (undriven)
EDT (edt_blocks)
PC* (pin_constraints)
TC* (tied_cells)
MPO (mask_po)
SEQ (sequential_depth)
OCC (on_chip_clock_control)
IJTAG (ijtag)
Unclassified
UC+UO
AAB (atpg_abort)
UNS (unsuccess)

*Use "report_statistics -detailed_analysis" for details.

Coverage

test_coverage	68.27%	92.63%
fault_coverage	62.86%	82.94%
atpg_effectiveness	99.94%	99.94%

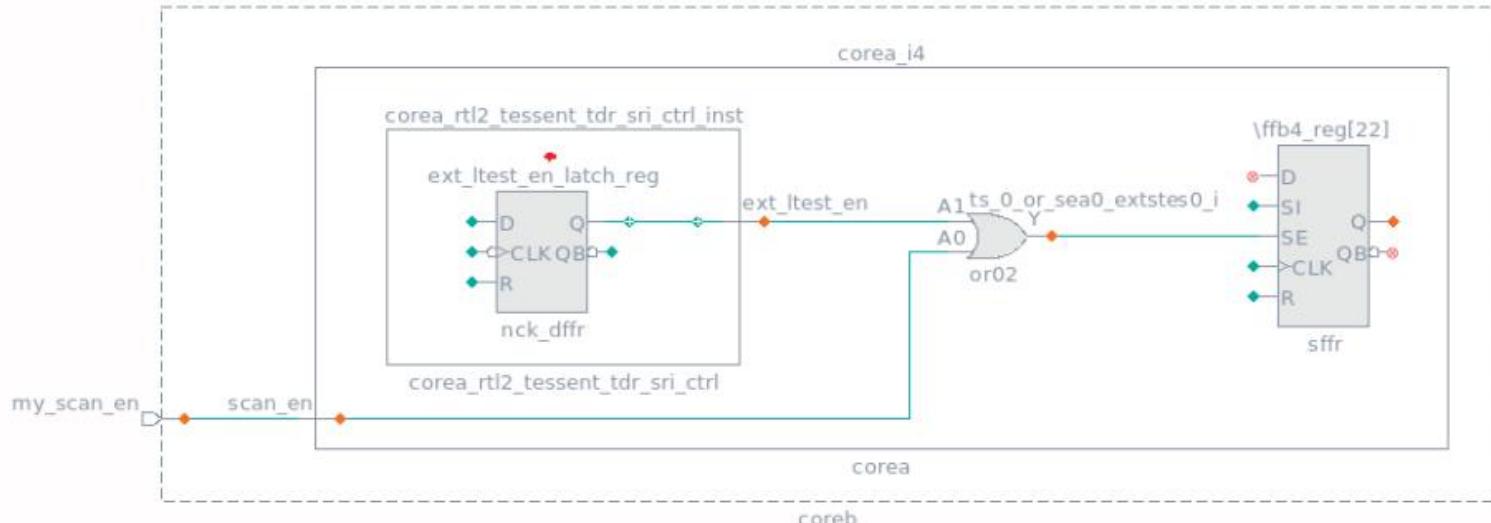
#test_patterns	287
#simulated_patterns	307
CPU_time (secs)	13.5

Major drop is because of undriven nets

```

ANALYSIS> system_gvim AU_UDN
Gtk-Message: 23:25:52.630: Failed to load module "canberra-gtk-module"
0
ANALYSIS> a_s_o /corea_i4/\ffb4_reg[22]/D -disp hier
// Error: Specified object 'fb4_reg[22]/D' not found in the hierarchical design.
ANALYSIS> a_s_o /corea_i4/\ffb4_reg[22]/D -disp hier
ANALYSIS>

```



This is a shared output wrapper,
 D input will be a part of CoreA level
 While doing the coreb level insertion - graybox of corea - only the periphery information

Simulation:-

verilog_files.list (~/aug23/level3/Lab4/coreb/5.atpg/sa/intest/simulations) - GVIM7

File Edit Tools Syntax Buffers Window Help

File menu icons: New, Open, Save, Print, Cut, Copy, Paste, Find, Replace, Select All, Exit.

Path: /home/vidishar/aug23/level3/Lab4/coreb/tsdb_outdir/dft_inserted_designs/coreb_gate.dft_inserted_design/coreb.vg

```

../../../../library/adk.v
../../../../library/mems/SYNC_1R1W_16x8.v
../../../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted_design/corea.vg_graybox

```

```

# Simulated      280 patterns
#
# Simulated      281 patterns
#
# Simulated      282 patterns
#
# Simulated      283 patterns
#
# Simulated      284 patterns
#
# Simulated      285 patterns
#
# Simulated      286 patterns
#
# Simulated      287 patterns
#
# No error between simulated and expected patterns
#
# ** Note: $finish : coreb_int_mode_parallel.v(6219)
#   Time: 55922 ns  Iteration: 0  Instance: /parallel_TB
# End time: 12:10:28 on Feb 12,2024, Elapsed time: 0:00:05
# Errors: 0, Warnings: 17

```

Extest:-

```

1 set_context patterns -scan
2 set_tsdb_output_directory ../../../../tsdb_outdir
3
4 read_cell_library ../../../../../../library/adk.tcelllib
5 read_verilog ../../../../../../library/mems/SYNC_1R1W_16x8.v -interface_only
6
7 open_tsdb ../../../../../../Lab3/corea/tsdb_outdir
8 read_design corea -design_id gate -view graybox -verbose
9 read_design coreb -design_id gate
10 set_current_design coreb
11 set_current_mode edt_stuck extest -type external
12 import_scan_mode ext_mode -fast_capture_mode off
13 |
14 add_output_masks -all
15
16 check_design_rules
17
18 set_fault_type stuck
19
20 create_patterns
21
22 read_faults /hdd2/home/vidishar/aug23/level3/Lab4/coreb/tsdb_outdir/logic_test_cores/coreb_gate.logic_test_core/coreb.atp
g_mode_edt_stuck_intest/coreb_edt_stuck_intest_stuck.faults.gz -merge
23
24 report_statis -det
25 system mkdir -p -v simulations
26
27 write_patterns /hdd2/home/vidishar/aug23/level3/Lab4/coreb/5.atpg/sa/extest/simulations/coreb_ext_mode_parallel.v -verilo
g -serial -replace -parameter_list {SIM_TOP_NAME parallel_TB SIM_KEEP_PATH 1 SIM_STATUS_MSG 1}
28
29 report_statis -det
30
~
```

Statistics Report

Stuck-at Faults

Fault Classes	#faults	#fau
	(total)	(total r)
lts		
elevant)		
FU (full)	81446	617
95		
UO (unobserved) (0.03%)	17 (0.02%)	same
DS (det_simulation) (62.27%)	38477 (47.24%)	same
DI (det_implication) (22.08%)	13647 (16.76%)	same
PU (posdet_untestable) (0.00%)	3 (0.00%)	same
PT (posdet_testable) (0.10%)	64 (0.08%)	same
UU (unused) (9.19%)	5678 (6.97%)	same
TI (tied) (0.39%)	240 (0.29%)	same
BL (blocked) (0.23%)	140 (0.17%)	same
RE (redundant) (0.60%)	369 (0.45%)	same
AU (atpg_untestable) (5.11%)	22811 (28.01%)	3160

Fault Sub-classes

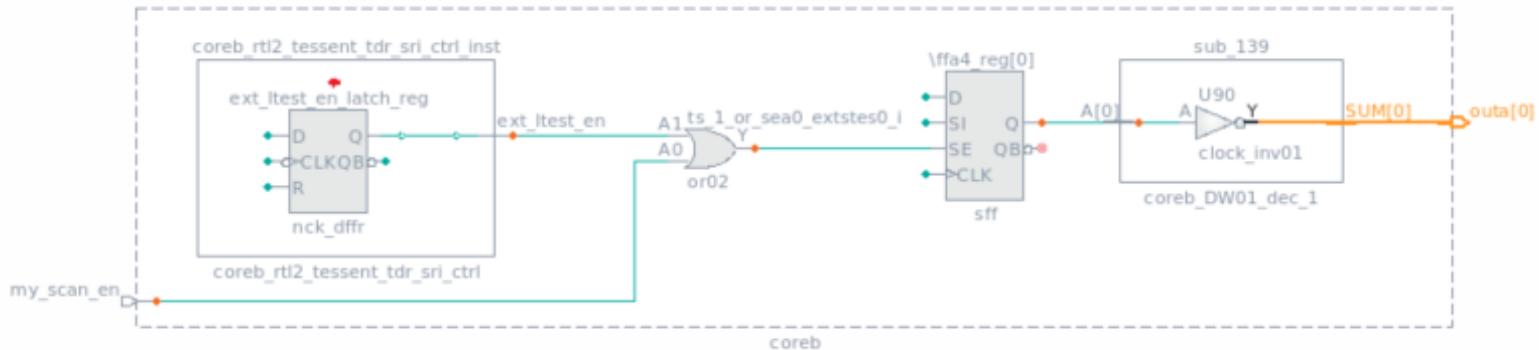
DI (det_implementation)			
EDT (edt_logic)	1351 (1.66%)	same	
(2.19%)			
SCAN (scan_path)	7715 (9.47%)	same	
(12.48%)			
SEN (scan_enable)	1748 (2.15%)	same	
(2.83%)			
CLK (clock)	2807 (3.45%)	same	
(4.54%)			
SR (set_reset)	10 (0.01%)	same	
(0.02%)			
DIN (data_input)	16 (0.02%)	same	
(0.03%)			
AU (atpg_untestable)			
UDN (undriven)	990 (1.22%)	same	
(1.60%)			
PC (pin_constraints)	35 (0.04%)	same	
(0.06%)			
(Individual pin constraints below threshold)	33 (0.04%)		
(Combined pin constraints)	2 (0.00%)		
TC (tied_cells)	924 (1.13%)	same	
(1.50%)			
/corea_i1/corea_rtl2_tessent_tdr_sri_ctrl_inst/int_ltest_en_latch_reg (19969) T0	196 (0.24%)		
/corea_i4/corea_rtl2_tessent_tdr_sri_ctrl_inst/int_ltest_en_latch_reg (20974) T0	196 (0.24%)		
/corea_i3/corea_rtl2_tessent_tdr_sri_ctrl_inst/int_ltest_en_latch_reg (20639) T0	196 (0.24%)		
/corea_i2/corea_rtl2_tessent_tdr_sri_ctrl_inst/int_ltest_en_latch_reg (20304) T0	196 (0.24%)		
(Individual tied cells below threshold)	126 (0.15%)		
(Combined tied cells)	14 (0.02%)		
MPO (mask_po)	1208 (1.48%)	same	
(1.95%)			
SEQ (sequential_depth)	1 (0.00%)	same	
(0.00%)			
OCC (on_chip_clock_control)	1506 (1.85%)	de	
leted			
IJTAG (ijtag)	18145 (22.28%)	de	
leted			
Unclassified	2 (0.00%)	same	
(0.00%)			
UC+UO			
AAB (atpg_abort)	8 (0.01%)	same	
(0.01%)			
UNS (unsuccess)	9 (0.01%)	same	
(0.01%)			

Coverage

```
test_coverage 69.53%
94.20% 64.04%
fault_coverage 84.40%
atpg_effectiveness 99.94%
-----
#test_patterns 0
#simulated_patterns 0
CPU_time (secs) 9.0
```

ATPG_UD - it has a coverage loss of 1.6%

Share output wrapper of CoreB level



CoreB levels AU.MPO will be covered during TOP level.

Step 6: Pattern Retargetting

PATTERN RE-TARGETTING

Re-applying already generated coreA intest patterns from top level instead of generating it again.

Why pattern retargeting?

Finally at the tester level, everything has to be applied from top level.

Why only coreA intest?

CoreA extest (interconnections) are already tested at the coreB level and patterns are generated from coreB level.

Line 23 has written in a Note

NOTE :

In the scan pattern retargeting, currently only the retargeting of scan data is supported by our tool.

Hence the tool ignores the capture info in the pattern file.

The user is expected to define the no. of ATPG cycles required for capture.

The no. specified with the should be large enough to accommodate the actual capture pulses needed for capture at coreA level.

- pat db (pattern data base) used during pattern retargetting

```

1 set_context patterns -scan_retargeting
2
3 set_tsdb_output_directory ../../../../tsdb_outdir
4
5 open_tsdb ../../../../../../Lab3/corea/tsdb_outdir
6
7
8 read_design corea -design_id gate -view graybox -verbose
9 read_design coreb -design_id gate
10
11 read_cell_library ../../../../../../library/adk.tcelllib
12 read_verilog ../../../../../../library/mems/SYNC_1RIW_16x8.v -interface_only
13
14 set_current_design coreb
15 add_core_instances -module corea -mode edt_stuck_intest
16
17 import_clocks
18 check_design_rules
19 write_tsdb_data -replace
20
21 read_patterns ../../../../../../Lab3/corea/tsdb_outdir/logic_test_cores/corea_gate.logic_test_core/corea.atpg_mode_edt_stuck
    _intest/corea_edt_stuck_intest_stuck.patdb
22
23 set_external_capture_options -pll_cycles 5 [lindex [get_timeplate_list] 0]
24
25 system mkdir -p -v simulations
26
27
28 write_pattern /hdd2/home/vidishar/aug23/level3/Lab4/coreb/6.pattern_retargetting(sa/intest/simulations/coreb_level_corea_
parallel.v -parallel -v -replace -param_list {SIM_TOP_NAME Parallel_TB}
29

```

Retargetting:-

```

/home/vinayakp/aug23/level3/Lab4/coreb/6.pattern_retargetting(sa/intest>>tessent -shell -dofile corea_pattern_re
target.tcl
// Warning: Tessent user documentation not found
// Tessent Shell 2021.1 Fri Feb 26 20:45:56 GMT 2021
// Copyright 2011-2021 Mentor Graphics Corporation
//
// All Rights Reserved.
//
// THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION WHICH
// IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS AND IS
// SUBJECT TO LICENSE TERMS.
//
// Mentor Graphics software executing under x86-64 Linux on Mon Feb 19 00:10:06 IST 2024.
// 64 bit version
// Host: vlsiguru (64168 MB RAM, 32191 MB Swap)
//
// command: set_context patterns -scan_retargeting
// command: set_tsdb_output_directory ../../../../tsdb_outdir
// command: open_tsdb ../../../../../../Lab3/corea/tsdb_outdir
// command: read_design corea -design_id gate -view graybox -verbose
// sub-command: set_read_design_tag corea
// sub-command: read_verilog ../../../../../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted
    _design/corea.vg_graybox -no_duplicate_modules_warnings
// sub-command: set_read_design_tag ""
// sub-command: read_icl ../../../../../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted_des
    ign/corea.icl -no_notes
// sub-command: source ../../../../../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted_des
    ign/corea.pdl
// sub-command: read_core_descriptions ../../../../../../Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.df
    t_inserted_design/corea.tcd
// command: read_design coreb -design_id gate
// command: read_cell_library ../../../../../../library/adk.tcelllib

```

```

// Reading DFT Library file ../../../../../../library/adk.tcelllib
// Finished reading file ../../../../../../library/adk.tcelllib
// command: read_verilog ../../../../../../library/mems/SYNC_1R1W_16x8.v -interface_only
// command: set_current_design coreb
// Warning: 73 cases: Undriven net in netlist module
// Warning: 103 cases: Floating input on instance in netlist
// Warning: 63 cases: Net in netlist not connected
// Note: Issue set_current_design with the -show_elaboration_warnings option to see more details about previous
warnings
// -----
// Begin ICL elaboration and checking.
// -----
// ICL elaboration completed, CPU time=0.25 sec.
// -----
// command: add_core_instances -module corea -mode edt_stuck_intest
// Reading core description file ../../../../../../Lab3/corea/tsdb_outdir/logic_test_cores/corea_gate.logic_test_c
ore/corea.atpg_mode_edt_stuck_intest/corea_edt_stuck_intest.tcd.gz
// Warning: The core description of 'corea_rtl1_tessent_sib_1' (instrument type 'occ') has been overwritten.
// Added core instance 'corea_i1'.
// Added core instance 'corea_i2'.
// Added core instance 'corea_i3'.
// Added core instance 'corea_i4'.
// command: import_clocks
// command: check_design_rules
// Warning: Rule FN1 violation occurs 157 times
// Warning: Rule FN3 violation occurs 4 times
// Warning: Rule FN4 violation occurs 2007 times
// Warning: Rule FP13 violation occurs 103 times
// Flattening process completed, cell instances=11311, gates=22648, PIs=87, Pos=79, CPU time=0.11 sec.
// -----
// Begin circuit learning analyses.

// Begin simulation of test_setup procedure with 591 cycles.
// Simulation of test_setup procedure completed, CPU time=0.0 sec.
// Begin simulation of load_unload procedure.
// Simulation of load_unload procedure completed, CPU time=0.1 sec.
// -----
// Begin transparent latch checking for 122 latches.
// -----
// Warning: 37 latches not transparent due to uncontrollable. (D6)
// Warning: 4 latches not transparent due to all clocks off. (D6)
// Warning: 12 latches not transparent due to unobservable. (D6)
// Number transparent latches = 69.
// -----
// Begin scan clock rules checking.
// -----
// 2 scan clock/set/reset lines have been identified.
// All scan clocks successfully passed off-state check.
// 455 sequential cells passed clock stability checking.
// There were 5 clock rule C3 fails (clock may capture data affected by its captured data).
// Warning: There were 48 clock rule C4 fails (clock may be affected by its captured data).
// Warning: There were 310 clock rule C7 fails (nonscan cell capture ability check).
// Note: Trailing edge triggered device can capture data affected by leading edge.
// Core instances=4, Shift cycles=58, Scan channels=8, Scan chains=60, Scan cells=2660
// command: write_tsdb_data -replace
// Writing ../../../../../../tsdb_outdir/logic_test_cores/coreb_gate.logic_test_core/coreb.atpg_retargeting_mode_retargeting/coreb_retargeting.tcd.gz
// command: read_patterns ../../../../../../Lab3/corea/tsdb_outdir/logic_test_cores/corea_gate.logic_test_core/cor
ea.atpg_mode_edt_stuck_intest/corea_edt_stuck_intest_stuck.patdb
// command: set_external_capture_options -pll_cycles 5 [lindex [get_timeplate_list] 0]
// command: system mkdir -p -v simulations
// command: write_patterns /hdd2/home/vidishar/aug23/level3/Lab4/coreb/6.pattern_retargetting/sa/intest/simulat
ions/coreb_level_corea_parallel.v -parallel -v -replace -param_list {SIM_TOP_NAME Parallel_TB}
// Error: File /hdd2/home/vidishar/aug23/level3/Lab4/coreb/6.pattern_retargetting/sa/intest/simulations/coreb_l
evel_corea_parallel.v cannot be created
// 'DOfile_corea_pattern_retarget.tcl' aborted at line 28

```

Simulations:-

- 1 /hdd2/home/vidishar/aug23/level3/Lab4/coreb/tsdb_outdir/dft_inserted_designs/coreb_gate.dft_inserted_design/coreb.vg
- 2 ../../../../../../library/adk.v
- 3 ../../../../../../library/mems/SYNC_1R1W_16x8.v
- 4 /hdd2/home/vidishar/aug23/level3/Lab3/corea/tsdb_outdir/dft_inserted_designs/corea_gate.dft_inserted_design/corea.vg
- 5

```
# Begin chain test
#
# 23720ns: Start clock monitoring on: clkc
# 23720ns: Start clock monitoring on: clkb
# 23720ns: Start clock monitoring on: clka
# 23841.200ns: Clock monitoring passed: clka. Period = 10.000000ns as expected (within 1.00% margin of 10.000000ns)
# 23879.984ns: Clock monitoring passed: clkb. Period = 13.200000ns as expected (within 1.00% margin of 13.200000ns)
# 23889.680ns: Clock monitoring passed: clkc. Period = 14.000000ns as expected (within 1.00% margin of 14.000000ns)
# End chain test
#
# No error between simulated and expected patterns
#
# ** Note: $finish : coreb_level_corea_parallel.v(18916)
#   Time: 112122 ns Iteration: 0 Instance: /Parallel_TB
# End time: 00:13:49 on Feb 19,2024, Elapsed time: 0:00:07
# Errors: 0, Warnings: 1
```

Step 7: MBIST Patterns on Netlist

```
1 set_context patterns
2 set_tsdb_output_directory ../tsdb_outdir
3
4 read_cell_library ../../library/adk.tcelllib
5
6 open_tsdb /hdd2/home/vidishar/aug23/level3/Lab3/corea/tsdb_outdir/
7
8 read_design coreb -design_id gate -view interface -verbose
9 read_design corea -design_id gate -view interface -verbose
10
11
12 set_current_design coreb
13
14 set_defaults_value /PatternsSpecification/SignoffOptions/simulate_instruments_in_lower_physical_instances on
15
16 set spec [create_patterns_spec]
17 report_config_data $spec
18 process_patterns_specification
19
20 set_simulation_library_sources -v ../../library/adk.v -y ../../library/mems/ -extension v
21 run_testbench_simulations
22
23
```

previously we have validated the mbist patterns on rtl level netlist

Here we are doing on gate level netlist

```
// Done processing of /PatternsSpecification(coreb,gate,signoff)
//
// Writing configuration data file '../tsdb_outdir/patterns/coreb_gate.patterns_spec_signoff'.
// command: set_simulation_library_sources -v ../../library/adk.v -y ../../library/mems/ -extension v
// command: run_testbench_simulations
Starting 15 simulations for ./simulation_outdir/coreb_gate.simulation_signoff
// Waiting for the simulation(s) to complete

unscheduled 0 queued 0 running 0 pass 15 fail 0
```