Lab 2 - Implementation

- It consists of MBIST, Synthesis, Scan (with wrappers), ATPG, Simulations.

Step 1: MBIST Insertion

```
#//
#//      ---  |   |     /\       ----   ----             /|
#//     |   | |   |    /  \    |     |                  / |
#//     |_ _| |- -|   /    \    ----  |----   ========     |
#//     |     |   |  /------\       | |      ========     |
#//     |     |   | /        \  ----   ----               __|__
###//

### context "dft rtl" tell the tool to enter into RTL insertion mode, design_id tells to create a seperate directory in t
  sdb for this particular below insertion steps. -design_id <your custom name for this insertion , for example first_insert
  ion>
set_context dft -rtl -design_id mbist_insertion

## specify the output directory where you want to dump the outputs of mbist insertion
set_tsdb_output_directory ../tsdb_outdir

## provide the design files and library files

read_cell_library ../../library/adk.tcelllib
read_verilog ../../library/mems/SYNC_1R1W_16x8.v -exclude_from_file_dictionary
read_verilog ../design/coreb.v

set_current_design coreb

add_black_boxes -auto
set_design_level physical_block

add_clocks clka -period 10ns
add_clocks clkb -period 13.2ns
add_clocks clkc -period 14ns
report_clocks

set_dft_specification_requirements -memory_test on
coreb mbist.tcl
#//
#//      ---  |   |     /\       ----   ----             ----
#//     |   | |   |    /  \    |     |                      |
#//     |_ _| |- -|   /    \    ----  |----   ========   __/
#//     |     |   |  /------\       | |      ========  |
#//     |     |   | /        \  ----   ----               ------

## DFT Signals
add_dft_signal ltest_en int_mode ext_mode tck_occ_en int_ltest_en ext_ltest_en
add_dft_signal scan_en   -source_node scan_en
add_dft_signal shift_capture_clock -source_nodes test_clock
check_design_rules

#//
#//      ---  |   |     /\       ----   ----             ----
#//     |   | |   |    /  \    | |    |                      |
#//     |_ _| |- -|   /    \    ----  |----   ========   __/
#//     |     |   |  /------\       | |      ========     \
#//     |     |   | /        \  ----   ----               ____|

set spec [create_dft_specification]

report_config_dat $spec

process_dft_specification

extract_icl
```

```
#//
#//      ---  |   |     /\   |   ----   ----            /
#//     |   | |   |    /  \     |      |               / |
#//     |_ _| |- -|   /    \    ----   |----   ========  |__|__
#//     |     |   |  /------\       | |       ========     |
#//     |     |   | /        \   ----   ----               |
#//
#//      ---  |   |     /\       ----   ----             ----
#//     |   | |   |    /  \     |      |                 |
#//     |_ _| |- -|   /    \    ----   |----   ========  |___
#//     |     |   |  /------\       | |       ========      |
#//     |     |   | /        \   ----   ----               ____|

#create_patterns_spec
set spec1 [create_patterns_spec]

report_config_data $spec1

process_patterns_specification
write_design_import_script -use_relative_path_to . -replace

set_simulation_library_sources -v ../design/corea_interface.v -v ../../library/adk.v -y ../../library/mems -extension v

report_simulation_library_sources

run testbench simulations
```

Here the open tsdb command and graybox netlist it wont be read because it is just a warm up test case.

- Here the graybox netlist hasn't read so the coverage will be less why? Because the interconnections will not be tested.

```
//      Writing pattern file '../tsdb_outdir/patterns/coreb_mbist_insertion.patterns_signoff/MemoryBist_Parallel
RetentionTest_P1.v'
//      Writing simulation data dictionary file '../tsdb_outdir/patterns/coreb_mbist_insertion.patterns_signoff/
simulation.data_dictionary'
//
//  Done  processing of /PatternsSpecification(coreb,mbist_insertion,signoff)
//
//  Writing configuration data file '../tsdb_outdir/patterns/coreb_mbist_insertion.patterns_spec_signoff'.
//  command: write_design_import_script -use_relative_path_to . -replace
//  Writing file 'coreb.dc_shell_import_script'.
//  command: #//
//  command: #//         ---  |   |     /\       ----   ----             ----
//  command: #//        |   | |   |    /  \     |      |                |
//  command: #//        |_ _| |- -|   /    \    ----   |----   ========  |___
//  command: #//        |     |   |  /------\       | |       ========      |
//  command: #//        |     |   | /        \   ----   ----               ____|
//  command: set_simulation_library_sources -v ../design/corea_interface.v -v ../../library/adk.v -y ../../libra
ry/mems -extension v
//  command: report_simulation_library_sources
//
//  List of -v/-y files and directories
//  type  path                                                                  file extensions
//  ----  ------------------------------------------------------------------  ---------------
//  file  ../design/corea_interface.v
//  file  ../../library/adk.v
//  dir   ../../library/mems                                                   v v.gz
//  file  /home/tools/mentor/MENTOR_SOURCE/lnx-x86/lib64/hdleng/lib/dft_sim.v
//  command: run_testbench_simulations
Starting 3 simulations for ./simulation_outdir/coreb_mbist_insertion.simulation_signoff
//  Waiting for the simulation(s) to complete

unscheduled 0 queued 0 running 0 pass 3 fail 0
SETUP>
```

So 3 simulations which are passed (MBIST, MBIST Parallel Retention, IJTAG)

Step 2: Synthesis

```
1
2 sh mkdir -p -v outputs
3
4 set design_name corea
5
6
7 ## Defind the library files
8 set target_library "../../library/adk.db"
9 set link_library "../../library/adk.db $target_library"
10 read_db $target_library
11
12 # Bus naming style for Verilog
13 set bus_naming_style {%s[%d]}
14
15 # Read input design files
16 source ../mbist_insertion/${design_name}.dc_shell_import_script
17
18 # Synthesize the top module
19 elaborate ${design_name}
20 set_size_only [get_cells tessent_persistent_cell_* -hier -filter {is_hierarchical==false}] -all_instances
21 link
22
23 # Check design for inconsistencies
24 check_design
25
26 # Timing specification
27 create_clock -period 10 -waveform {0 5} clka
28 create_clock -period 10 -waveform {0 5} clkb
29
30
31 # Avoid assign statements in the synthesized netlist.
32 set_fix_multiple_port_nets -feedthroughs -outputs -buffer_constants
33
34 # Compile design
35 uniquify
36 compile -map_effort medium
37
38 # Report design results for TOP design
39 report_area > outputs/${design_name}_dc_script_report.out
40 report_constraint -all_violators -verbose >> outputs/${design_name}_dc_script_report.out
41 report_timing -path full -delay max >> outputs/${design_name}_dc_script_report.out
42 report_reference >> outputs/${design_name}_dc_script_report.out
43
44 write -f verilog -hierarchy -o outputs/${design_name}_top_gate.v
45
46 sh rm *.syn *.pvl *.mr
47
48 exit
```

```
  Optimization Complete
  ---------------------
1
# Report design results for TOP design
report_area > outputs/${design_name}_dc_script_report.out
report_constraint -all_violators -verbose >> outputs/${design_name}_dc_script_report.out
report_timing -path full -delay max >> outputs/${design_name}_dc_script_report.out
report_reference >> outputs/${design_name}_dc_script_report.out
write -f verilog -hierarchy -o outputs/${design_name}_top_gate.v
Warning: Design 'corea' has '1' unresolved references. For more detailed information, use the "link" command. (U
ID-341)
Writing verilog file '/home/vinayakp/aug23/level3/Lab1/synthesis/outputs/corea_top_gate.v'.
Warning: Verilog 'assign' or 'tran' statements are written out. (VO-4)
Warning: Verilog writer has added 5 nets to module corea_first_insertion_tessent_mbist_c1_controller using SYNOP
SYS_UNCONNECTED_ as prefix.  Please use the change_names command to make the correct changes before invoking the
 verilog writer.  (VO-11)
Warning: Verilog writer has added 5 nets to module corea_first_insertion_tessent_mbist_c2_controller using SYNOP
SYS_UNCONNECTED_ as prefix.  Please use the change_names command to make the correct changes before invoking the
 verilog writer.  (VO-11)
1
sh rm *.syn *.pvl *.mr
exit

Memory usage for this session 166 Mbytes.
Memory usage for this session including child processes 166 Mbytes.
CPU usage for this session 24 seconds ( 0.01 hours ).
Elapsed time for this session 25 seconds ( 0.01 hours ).

Thank you...
```

Step 3: Scan Insertion

```
set_context dft -scan -design_id corea_scan -hierarchical

set_tsdb_output_directory ../tsdb_outdir

read_cell_library ../../library/adk.tcelllib

read_verilog ../../library/mems/SYNC_1R1W_16x8.v -interface_only

read_verilog ../synthesis/outputs/corea_top_gate.v

read_design corea -design_id first_insertion -icl_only

set_current_design corea

set_design_level physical_block

delete_clocks -all

add_clocks 0 clka
add_clocks 0 clkb
add_clocks 0 clkc

## change following in other atpg scripts too
add_clocks 1 rst

add_primary_inputs /rsta_reg/QB -cut
add_primary_inputs /rstb_reg/QB -cut
add_primary_inputs /rstc_reg/QB -cut

add_pin_constraints C0 /rsta_reg/QB
add_pin_constraints C0 /rstb_reg/QB
add_pin_constraints C0 /rstc_reg/QB


check_design_rules

set_wrapper_analysis_options -exclude_ports {*ijtag* *clk*}

set_dedicated_wrapper_cell_options on -ports rst

analyze_wrapper_cells

add_scan_mode int_mode -chain_length 50

add_scan_mode ext_mode -chain_length 32

analyze_scan_chains

insert_test_logic -write_in_tsdb on

```

```
/home/vinayakp/aug23/level3/Lab1/scan_insertion>>tessent -shell -dofile corea_scan.tcl
//  Warning: Tessent user documentation not found
//  Tessent Shell  2021.1    Fri Feb 26 20:45:56 GMT 2021
//               Copyright 2011-2021 Mentor Graphics Corporation
//
//                          All Rights Reserved.
//
//    THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION WHICH
//  IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS AND IS
//                       SUBJECT TO LICENSE TERMS.
//
//  Mentor Graphics software executing under x86-64 Linux on Mon Feb 19 10:46:05 IST 2024.
//  64 bit version
//  Host: vlsiguru (64168 MB RAM, 32191 MB Swap)
//
//  command: set_context dft -scan -design_id corea_scan -hierarchical
//  command: set_tsdb_output_directory ../tsdb_outdir
//  command: read_cell_library ../../library/adk.tcelllib
//  Reading DFT Library file ../../library/adk.tcelllib
//  Finished reading file ../../library/adk.tcelllib
//  command: read_verilog ../../library/mems/SYNC_1R1W_16x8.v -interface_only
//  command: read_verilog ../synthesis/outputs/corea_top_gate.v
//  command: read_design corea -design_id first_insertion -icl_only
//  command: set_current_design corea
//  Warning: 9 cases: Undriven net in netlist module
//  Warning: 61 cases: Net in netlist not connected
//  Note: Issue set_current_design with the -show_elaboration_warnings option to see more details about previous
 warnings
//  ---------------------------------------------------------------------------
//  Begin ICL elaboration and checking.
//  ----------------------------------
//  ICL elaboration completed, CPU time=0.10 sec.
//  ---------------------------------------------------------------------------
//  command: set_design_level physical_block
//  command: delete_clocks -all
//  command: add_clocks 0 clka
//  command: add_clocks 0 clkb
//  command: add_clocks 0 clkc
//  command: ## change following in other atpg scripts too
//  command: add_clocks 1 rst
//  command: add_primary_inputs /rsta_reg/QB -cut
//  Warning: Primary input 'rsta_reg/QB_pport' is added at pin '/rsta_reg/QB'
//  command: add_primary_inputs /rstb_reg/QB -cut
//  Warning: Primary input 'rstb_reg/QB_pport' is added at pin '/rstb_reg/QB'
//  command: add_primary_inputs /rstc_reg/QB -cut
//  Warning: Primary input 'rstc_reg/QB_pport' is added at pin '/rstc_reg/QB'
//  command: add_pin_constraints C0 /rsta_reg/QB
//  command: add_pin_constraints C0 /rstb_reg/QB
//  command: add_pin_constraints C0 /rstc_reg/QB
//  command: check_design_rules
//  Warning: Rule FN1 violation occurs 86 times
//  Warning: Rule FN4 violation occurs 682 times
//  Flattening process completed, cell instances=5999, gates=9522, PIs=77+4(pseudo ports), POs=65, CPU time=0.05
 sec.
//  ---------------------------------------------------------------------------
//  Begin circuit learning analyses.
//  --------------------------------
//  Learning completed, CPU time=0.04 sec.
//  ---------------------------------------------------------------------------
//  Begin scan chain identification process, memory elements = 682,
//  sequential library cells = 682.
//  ---------------------------------------------------------------------------
//  Begin simulation of test_setup procedure with 23 cycles.
//  Simulation of test_setup procedure completed, CPU time=0.0 sec.
//  Begin simulation of auto-generated load_unload procedure.
//  Simulation of load_unload procedure completed, CPU time=0.0 sec.
//  Scan segment = /corea_first_insertion_tessent_sib_sti_inst/ltest_so successfully traced with scan_cells = 7.
```

```
//  7 scan cells have been identified in 1 scan segment.
//  Warning: 1 edge-triggered clock ports set to stable high. (D7)
//  Warning: Model 'nlatch' has no muxscan scan equivalent and is treated as nonscan model
//  ---------------------------------------------------------------------------
//  30 sequential library cells are treated as non-scan.
//  ---------------------------------------------------------------------------
//     8 sequential library cells missing mux-scan equivalent.
//     5 sequential library cells below hard module.
//    17 sequential library cells defined non-scan.
//  ---------------------------------------------------------------------------
//  Begin scannability rules checking for 642 sequential library cells
//  and 1 scan segment. The scan segment contains 10 additional cells.
//  ---------------------------------------------------------------------------
//  Note: There were 3 S7 violations (Potentially scannable cell that is not in the clock path is driven by a co
nstant value).
//  642 sequential library cells and 1 scan segment identified as scannable.
//  ---------------------------------------------------------------------------
//  Begin transparent latch checking for 11 latches.
//  ---------------------------------------------------------------------------
//  Warning: 1 latches not transparent due to unobservable. (D6)
//  Number transparent latches = 10.
//  ---------------------------------------------------------------------------
//  Begin scan clock rules checking.
//  ---------------------------------------------------------------------------
//  7 scan clock/set/reset lines have been identified.
//  All scan clocks successfully passed off-state check.
//  317 sequential cells passed clock stability checking.
//  There were 23 clock rule C3 fails (clock may capture data affected by its captured data).
//  Note: Trailing edge triggered device can capture data affected by leading edge.
//  ---------------------------------------------------------------------------
//  32 non-scan memory elements are identified.
//  ---------------------------------------------------------------------------
//  18 non-scan memory elements are identified as TIE-0. (D5)
//   3 non-scan memory elements are identified as TIE-1. (D5)
//   1 non-scan memory element is   identified as TIE-X. (D5)
//  10 non-scan memory elements are identified as TLA.   (D5)
//  ---------------------------------------------------------------------------
//  ---------------------------------------------------------------------------
//  Begin shift register identification for 642 sequential library cells.
//  ---------------------------------------------------------------------------
//  Number of shift register flops recorded for scan insertion: 36 (5.28%)
//  Number of shift registers recorded for scan insertion: 17
//  Longest shift register has 3 flops.
//  Shortest shift register has 2 flops.
//  Potential number of nonscan flops to be converted to scan cells: 17
//  Potential number of scan cells to be converted to nonscan flops: 0
//  Number of targeted sequential library cells = 642
//  command: set_wrapper_analysis_options -exclude_ports {*ijtag* *clk*}
//  command: set_dedicated_wrapper_cell_options on -ports rst
//  command: analyze_wrapper_cells
//
//     Port information and user constraints:
//     --------------------------------------
//         Input ports:    77 total,     3 ignored,    10 excluded,     0 off,     0 on,    64 auto
//        Output ports:    65 total,     0 ignored,     1 excluded,     0 off,     0 on,    64 auto
//
//
//     Wrapper analysis summary:
//     -------------------------
//        64 flip-flops were converted into output shared wrapper cells.
//        64 flip-flops were converted into input shared wrapper cells.
//        Use report_wrapper_cells for more details.
//
//  command: add_scan_mode int_mode -chain_length 50
//  Automatically inferring '-enable_dft_signal int_mode' from the specified scan mode name.
//  Automatically inferring '-type internal' from the scan mode type (internal) associated with the enable DFT s
ignal 'int_mode'.
//  command: add_scan_mode ext_mode -chain_length 32
//  Automatically inferring '-enable_dft_signal ext_mode' from the specified scan mode name.
//  Automatically inferring '-type external' from the scan mode type (external) associated with the enable DFT s
ignal 'ext_mode'.
//  command: analyze_scan_chains
//  Chain allocation of 'int_mode' mode completed:
Distribution - populating 'int_mode' chains: 91.8% completed (estimated time remaining 0 secs)//        14 distr
ibuted chains of sizes ranging from 46 to 47
//  Chain allocation of 'ext_mode' mode completed:
Distribution - populating 'ext_mode' chains: 100.0% completed (estimated time remaining 0 secs)//         5 dist
ributed chains of sizes ranging from 26 to 27
//  command: insert_test_logic -write_in_tsdb on
```

```
============================
Test Logic Insertion Summary:
============================

  Structural Data:
  ----------------
                          Added top-level port count:           4
                                Added instance count:         191

  Logical Data:
  -------------
                Added clock gater control logic count:           2
                      Added input wrapper logic count:          64
                     Added output wrapper logic count:          64
                         Added pipelining logic count:           7
                           Added retiming logic count:          22
                    Added scan chain count (int_mode):          14
                    Added scan chain count (ext_mode):           5

//  Warning: Flattened model deleted.
//
//  Writing out netlist and related files in ../tsdb_outdir/dft_inserted_designs/corea_corea_scan.dft_inserted_d
esign
```

Step 4: ATPG

Intest:-

```
1  set_context patterns -scan
2
3  set_tsdb_output_directory ../../../tsdb_outdir
4
5  read_cell_library ../../../../library/adk.tcelllib
6
7  read_verilog ../../../../library/mems/SYNC_1R1W_16x8.v -interface_only
8
9  read_design corea -design_id  corea_scan
10
11 set_current_design corea
12
13 ## it will save the patterns with the current_mode set SA inside tsdb with an option of internal
14 set_current_mode SA_intest -type internal
15
16 ## This will get the constraints/constant values related to intest mode from tsdb post scan insertion
17 #fast_capture_mode off -> will enable SA constraints , making it on -> will automatically program the TDR's to TDF mode.
18 import_scan_mode int_mode -fast_capture_mode off
19
20 add_clocks 1 rst
21
22 add_primary_inputs /rsta_reg/QB -cut
23 add_primary_inputs /rstb_reg/QB -cut
24 add_primary_inputs /rstc_reg/QB -cut
25
26 add_pin_constraints C0 /rsta_reg/QB
27 add_pin_constraints C0 /rstb_reg/QB
28 add_pin_constraints C0 /rstc_reg/QB
29
30 add_black_boxes -mod SYNC_1R1W_16x8
31
32 ## hacking commands since EDT, OCC are not inserted in the design and also in this lab session clocks are not declared as
    -pulse_in_capture mode like how done in Lab0. So please enable the following switches to process the next steps of ATPG.
33         ## General Note: these clocks should not be declared as pulse_in_capture since there is no occ and wrappers are e
   nabled.
34
35 set_attribute_value {clka clkb clkc test_clock rst} -name is_excluded_from_isolation_constraints
36 set_drc_hand R7 warning
37
38 check_design_rules
39
40 set_fault_type stuck
41
42 create_patterns
43
44 write_tsdb_data -replace
45
46 system mkdir -p -v simulations
47
48 write_patterns /hdd2/home/vidishar/aug23/level3/Lab1/atpg/sa/intest/simulations/corea_int_mode_parallel.v -verilog -paral
   lel -replace -parameter_list {SIM_TOP_NAME parallel_TB SIM_KEEP_PATH 1}
49
50
```

```
                          Statistics Report
                           Stuck-at Faults
-------------------------------------------------------------------------
Fault Classes                        #faults           #faults
                                     (total)       (total relevant)
-----------------------------  ---------------- --------------------
  FU (full)                          44610             44027
  -------------------------  ---------------- --------------------
  DS (det_simulation)              33140  (74.29%)       same  (75.27%)
  DI (det_implication)              5672  (12.71%)       same  (12.88%)
  PU (posdet_untestable)               1  ( 0.00%)       same  ( 0.00%)
  UU (unused)                       1150  ( 2.58%)       same  ( 2.61%)
  TI (tied)                          294  ( 0.66%)       same  ( 0.67%)
  BL (blocked)                       205  ( 0.46%)       same  ( 0.47%)
  RE (redundant)                     343  ( 0.77%)       same  ( 0.78%)
  AU (atpg_untestable)              3805  ( 8.53%)       3222  ( 7.32%)
-------------------------------------------------------------------------
Fault Sub-classes
  -------------------------
  DI (det_implication)
    SCAN  (scan_path)               3369  ( 7.55%)       same  ( 7.65%)
    SEN   (scan_enable)              788  ( 1.77%)       same  ( 1.79%)
    CLK   (clock)                   1462  ( 3.28%)       same  ( 3.32%)
    SR    (set_reset)                  3  ( 0.01%)       same  ( 0.01%)
    DIN   (data_input)                 2  ( 0.00%)       same  ( 0.00%)
    MBIST                             48  ( 0.11%)       same  ( 0.11%)
  AU (atpg_untestable)
    BB    (black_boxes)               56  ( 0.13%)       same  ( 0.13%)
    PC*   (pin_constraints)         1114  ( 2.50%)       same  ( 2.53%)
    TC*   (tied_cells)               803  ( 1.80%)       same  ( 1.82%)
    MPO   (mask_po)                  564  ( 1.26%)       same  ( 1.28%)
    SEQ   (sequential_depth)         529  ( 1.19%)       same  ( 1.20%)
    IJTAG (ijtag)                    583  ( 1.31%)         deleted
    Unclassified                     156  ( 0.35%)       same  ( 0.35%)
  *Use "report_statistics -detailed_analysis" for details.
-------------------------------------------------------------------------
Coverage
  -------------------------
  test_coverage                      91.07%              92.33%
  fault_coverage                     87.00%              88.16%
  atpg_effectiveness                100.00%             100.00%
-------------------------------------------------------------------------
#test_patterns                                             266
  #basic_patterns                                           62
  #clock_sequential_patterns                               204
#simulated_patterns                                        276
CPU_time (secs)                                            6.0
-------------------------------------------------------------------------
```

Extest:-

```
1  set_context patterns -scan
2
3  set_tsdb_output_directory ../../../tsdb_outdir
4
5  read_cell_library ../../../../library/adk.tcelllib
6
7  read_verilog ../../../../library/mems/SYNC_1R1W_16x8.v -interface_only
8
9  read_design corea -design_id  corea_scan
10
11 set_current_design corea
12
13 ## it will save the patterns/faults with the current_mode set SA inside tsdb with an option of internal
14 set_current_mode SA_extest -type external
15
16 ## This will get the constraints/constant values related to intest mode from tsdb post scan insertion
17 #fast_capture_mode off -> will enable SA constraints , making it on -> will automatically program the TDR's to TDF mode.
18 import_scan_mode ext_mode -fast_capture_mode off
19
20 add_clocks 1 rst
21
22 add_primary_inputs /rsta_reg/QB -cut
23 add_primary_inputs /rstb_reg/QB -cut
24 add_primary_inputs /rstc_reg/QB -cut
25
26 add_pin_constraints C0 /rsta_reg/QB
27 add_pin_constraints C0 /rstb_reg/QB
28 add_pin_constraints C0 /rstc_reg/QB
29
30 add_black_boxes -mod SYNC_1R1W_16x8
31
```

```
31
32 ## hacking commands since EDT, OCC are not inserted in the design and also in this lab session clocks are not declared as
    -pulse_in_capture mode like how done in Lab0. So please enable the following switches to process the next steps of ATPG.
33         ## General Note: these clocks should not be declared as pulse_in_capture since there is no occ and wrappers are e
   nabled.
34
35 set_attribute_value {clka clkb clkc test_clock rst} -name is_excluded_from_isolation_constraints
36 set_drc_hand R7 warning
37
38 check_design_rules
39
40 set_fault_type stuck
41
42 create_patterns
43
44 write_tsdb_data -replace
45
46 system mkdir -p -v simulations
47
48 write_patterns /hdd2/home/vidishar/aug23/level3/Lab1/atpg/sa/extest/simulations/corea_int_mode_parallel.v -verilog -paral
   lel -replace -parameter_list {SIM_TOP_NAME parallel_TB SIM_KEEP_PATH 1}
49
50 ## to get the overall coverage combined with both intest and extest , here extest faults already avaialble in this tessen
   t run , so just loading the previous intest faults list which consists of all fault categories. We can use below commands
51 read_faults  ./../../../tsdb_outdir/logic_test_cores/corea_corea_scan.logic_test_core/corea.atpg_mode_SA_intest/corea_SA_
   intest_stuck.faults.gz -merge
52
53 report_statis -det
```

```
                          Statistics Report
                           Stuck-at Faults
-------------------------------------------------------------------------
Fault Classes                        #faults          #faults
                                     (total)      (total relevant)
-----------------------------  ---------------- --------------------
  FU (full)                          44970             44347
  -------------------------  ---------------- --------------------
  UC (uncontrolled)                3604  ( 8.01%)       same  ( 8.13%)
  UO (unobserved)                  6671  (14.83%)       same  (15.04%)
  DS (det_simulation)              2272  ( 5.05%)       same  ( 5.12%)
  DI (det_implication)             1805  ( 4.01%)       same  ( 4.07%)
  PU (posdet_untestable)              1  ( 0.00%)       same  ( 0.00%)
  PT (posdet_testable)               69  ( 0.15%)       same  ( 0.16%)
  UU (unused)                      1150  ( 2.56%)       same  ( 2.59%)
  TI (tied)                         294  ( 0.65%)       same  ( 0.66%)
  BL (blocked)                      205  ( 0.46%)       same  ( 0.46%)
  RE (redundant)                    331  ( 0.74%)       same  ( 0.75%)
  AU (atpg_untestable)            28568  (63.53%)      27945  (63.01%)
-------------------------------------------------------------------------
Fault Sub-classes
  -------------------------
  DI (det_implication)
    SCAN  (scan_path)              1152  ( 2.56%)       same  ( 2.60%)
    SEN   (scan_enable)             276  ( 0.61%)       same  ( 0.62%)
    CLK   (clock)                   319  ( 0.71%)       same  ( 0.72%)
    SR    (set_reset)                 4  ( 0.01%)       same  ( 0.01%)
    DIN   (data_input)                6  ( 0.01%)       same  ( 0.01%)
    MBIST                            48  ( 0.11%)       same  ( 0.11%)
  AU (atpg_untestable)
    UDN   (undriven)                 16  ( 0.04%)       same  ( 0.04%)
    BB    (black_boxes)              56  ( 0.12%)       same  ( 0.13%)
```

```
    PC*   (pin_constraints)       378  ( 0.84%)       same  ( 0.85%)
    TC*   (tied_cells)           5558  (12.36%)       same  (12.53%)
    SEQ   (sequential_depth)    13910  (30.93%)       same  (31.37%)
    IJTAG (ijtag)                 623  ( 1.39%)         deleted
    Unclassified                 8027  (17.85%)       same  (18.10%)
  UC+UO
    AAB   (atpg_abort)          10275  (22.85%)       same  (23.17%)
  *Use "report_statistics -detailed_analysis" for details.
---------------------------------------------------------------------
Coverage
  --------------------------
  test_coverage                          9.57%               9.71%
  fault_coverage                         9.14%               9.27%
  atpg_effectiveness                    77.07%              77.07%
---------------------------------------------------------------------
#test_patterns                                                  60
  #basic_patterns                                               40
  #clock_sequential_patterns                                    20
#simulated_patterns                                            104
CPU_time (secs)                                               141.7
---------------------------------------------------------------------
```