Lab 1 - Implementation

- It consists of MBIST, Synthesis, Scan (with wrappers), ATPG, Simulations.

Step 1: MBIST Insertion

1. Phase 1

```
/home/vinayakp/aug23/level3/Lab1/mbist_insertion>>tessent -shell -dofile corea_mbist.tcl
//  Warning: Tessent user documentation not found
//  Tessent Shell  2021.1    Fri Feb 26 20:45:56 GMT 2021
//               Copyright 2011-2021 Mentor Graphics Corporation
//
//                         All Rights Reserved.
//
//    THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION WHICH
//  IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS AND IS
//                       SUBJECT TO LICENSE TERMS.
//
//  Mentor Graphics software executing under x86-64 Linux on Tue Jan 30 10:43:35 IST 2024.
//  64 bit version
//  Host: vlsiguru (64168 MB RAM, 32191 MB Swap)
//
//  command: #//
//  command: #//         ---  |   |     /\       ----   ----               /|
//  command: #//        |   | |   |    /  \    |      |                   / |
//  command: #//        |_ _| |- -|   /    \    ----  |----   ========      |
//  command: #//        |     |   |  /------\       | |       ========      |
//  command: ##//       |     |   | /        \  ----   ----                 __|__
//  command: ### context "dft rtl" tell the tool to enter into RTL insertion mode, design_id tells to create a s
eperate directory in tsdb for this particular below insertion steps. -design_id <your custom name for this inser
tion , for example first_insertion>
//  command: set_context dft -rtl -design_id first_insertion
//  command: ## specify the output directory where you want to dump the outputs of mbist insertion
//  command: set_tsdb_output_directory ../tsdb_outdir
//  command: ## provide the design files and library files
//  command: read_cell_library ../../library/adk.tcelllib
//  Reading DFT Library file ../../library/adk.tcelllib
//  Finished reading file ../../library/adk.tcelllib
//  command: read_verilog ../../library/mems/SYNC_1R1W_16x8.v -exclude_from_file_dictionary -verbose
//  Reading Verilog file ../../library/mems/SYNC_1R1W_16x8.v
//  Finished reading file ../../library/adk.tcelllib
//  command: read_verilog ../../library/mems/SYNC_1R1W_16x8.v -exclude_from_file_dictionary -verbose
//  Reading Verilog file ../../library/mems/SYNC_1R1W_16x8.v
//  Finished reading file ../../library/mems/SYNC_1R1W_16x8.v
//  command: read_verilog ../design/corea.v -verbose
//  Reading Verilog file ../design/corea.v
//  Finished reading file ../design/corea.v
//  command: ## Elaborate the design
//  command: set_current_design corea
//  command: # set the design level to either chip, physical_block or sub_block
//  command: set_design_level physical_block
//  command: ## declare the clocks and constraints
//  command: add_clocks 0 clka -period 10ns
//  command: add_clocks 0 clkb -period 13.2ns
//  command: add_clocks 0 clkc -period 14ns
//  command: report_clocks
User-defined Clocks (3):
========================

  Sync and Async Source Clocks
  ============================
   ------  ---------  ------------  --------  ---------
   Name    Off State   Constraints  Internal    Period
   ------  ---------  ------------  --------  ---------
   'clka'      -      Asynchronous     No     10.00ns
   'clkb'      -      Asynchronous     No     13.20ns
   'clkc'      -      Asynchronous     No     14.00ns

//  command: set_dft_specification_requirements -memory_test on
//  command: #//
```

2. Phase 2

```
//  command: set_dft_specification_requirements -memory_test on
//  command: #//
//  command: #//         ---  |   |     /\       ----   ----            ----
//  command: #//        |   | |   |    /  \     |      |                    |
//  command: #//        |_ _| |- -|   /    \     ----  |----   ========   __/
//  command: #//        |     |   |  /------\       | |       ========  |
//  command: #//        |     |   | /        \  ----   ----              ------
//  command: ## DFT Signals
//  command: add_dft_signals ltest_en int_mode ext_mode tck_occ_en int_ltest_en ext_ltest_en
//  command: add_dft_signals scan_en   -source_node scan_en
//  command: add_dft_signals shift_capture_clock -source_nodes test_clock
//  command: check_design_rules
//  ------------------------------------------------------------------------
//  Begin RTL synthesis.
//  --------------------
//  Synthesized modules=1, Time=1.54 sec.
//  Note: There was 1 module selectively synthesized. There were also 5 sub-modules created by synthesis.
//        Use 'get_module -filter is_synthesized' to see them.
//        You can also use 'set_quick_synthesis_options -verbose on' to have the synthesis step report the
//        synthesized module name in the transcript as it is being synthesized.
//  ------------------------------------------------------------------------
//  Warning: Rule FN4 violation occurs 2 times
//  Flattening process completed, cell instances=844, gates=4383, PIs=70, POs=64, CPU time=0.01 sec.
//  ------------------------------------------------------------------------
//  Begin circuit learning analyses.
//  --------------------------------
//  Learning completed, CPU time=0.01 sec.
//  command: #//
```

3. Phase 3

```
//  command: #//          ---  |   |     /\       ----   ----             ----
//  command: #//         |   | |   |    /  \     |      |                   |
//  command: #//         |_ _| |- -|   /    \     ----  |----   ========   __/
//  command: #//         |     |   |  /------\       | |       ========    \
//  command: #//         |     |   | /        \  ----   ----              ____|
//  command: set spec [create_dft_specification]
//  sub-command: create_dft_specification
//
//  Begin creation of DftSpecification(corea,first_insertion)
//    Creation of RtlCells wrapper
//    Creation of IjtagNetwork wrapper
//    Creation of MemoryBist wrapper
//    Creation of MemoryBisr wrapper
//
//  Done  creation of DftSpecification(corea,first_insertion)
//
//  command: report_config_data $spec

DftSpecification(corea,first_insertion) {
  IjtagNetwork {
    HostScanInterface(ijtag) {
      Sib(sri) {
        Attributes {
          tessent_dft_function : scan_resource_instrument_host;
        }
        Tdr(sri_ctrl) {
          Attributes {
            tessent_dft_function : scan_resource_instrument_dft_control;
          }
        }
      }
```

```
      Sib(sti) {
        Attributes {
          tessent_dft_function : scan_tested_instrument_host;
        }
        Sib(mbist) {
        }
      }
    }
  }
  MemoryBist {
    ijtag_host_interface : Sib(mbist);
    Controller(c1) {
      clock_domain_label : clka;
      Step {
        MemoryInterface(m1) {
          instance_name : ram1;
        }
      }
    }
    Controller(c2) {
      clock_domain_label : clkb;
      Step {
        MemoryInterface(m1) {
          instance_name : ram2;
        }
      }
    }
  }
}
//  command: process_dft_specification
//
//  Begin processing of /DftSpecification(corea,first_insertion)
//    --- IP generation phase ---
//    Validation of IjtagNetwork
//    Validation of MemoryBist
//    Processing of RtlCells
//      Generating Verilog RTL Cells
//        Verilog RTL : ../tsdb_outdir/instruments/corea_first_insertion_cells.instrument/corea_first_insertion_
tessent_posedge_synchronizer_reset.v
//
//      Loading the generated RTL verilog files (1) to enable instantiating the contained modules
//      into the design.
//    Processing of IjtagNetwork
//      Generating design files for IJTAG SIB module corea_first_insertion_tessent_sib_1
//        Verilog RTL : ../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_
tessent_sib_1.v
//        IJTAG ICL   : ../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_
tessent_sib_1.icl
//        TCD Scan    : ../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_
tessent_sib_1.tcd_scan
//        CTL         : ../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_
tessent_sib_1.ctl
//        TCD         : ../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_
tessent_sib_1.tcd
//        PDL         : ../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_
tessent_sib_1.pdl
//      Generating design files for IJTAG SIB module corea_first_insertion_tessent_sib_2
//        Verilog RTL : ../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_
tessent_sib_2.v
```

```
//      Generating design files for IJTAG SIB module corea_first_insertion_tessent_sib_3
//        Verilog RTL : ../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_
tessent_sib_3.v
//        IJTAG ICL   : ../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_
tessent_sib_3.icl
//      Generating design files for IJTAG Tdr module corea_first_insertion_tessent_tdr_sri_ctrl
//        Verilog RTL : ../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_
tessent_tdr_sri_ctrl.v
//        IJTAG ICL   : ../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_
tessent_tdr_sri_ctrl.icl
//
//      Loading the generated RTL verilog files (4) to enable instantiating the contained modules
//      into the design.
//    Processing of MemoryBist
//      Generating the IJTAG ICL for the memories.
//      Generating design files for MemoryBist Controller(c1)
//      Generating design files for MemoryBist Controller(c2)
//  Warning: There are warnings issued while generating design files for MemoryBist controller(s).
//           Review the messages in the following generation log files:
//           ../tsdb_outdir/instruments/corea_first_insertion_mbist.instrument/corea_first_insertion_tessent_mbi
st_c1.generation_log,
//           ../tsdb_outdir/instruments/corea_first_insertion_mbist.instrument/corea_first_insertion_tessent_mbi
st_c2.generation_log
//      Generating design files for Bist Access Port
//
//      Loading the generated RTL verilog files (5) to enable instantiating the contained modules
//      into the design.
//      Generating design files for MemoryBist controller assemblies
//    --- Instrument insertion phase ---
//   Inserting instruments of type 'ijtag'
//   Inserting instruments of type 'memory_bist'
//    Writing out modified source design in ../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_insert
ed_design
//    Writing out specification in ../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_spec
//
//  Done  processing of DftSpecification(corea,first_insertion)
//
//  command: extract_icl
//  Note: Updating the hierarchical data model to reflect RTL design changes.
//  Writing design source dictionary : ../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_de
sign/corea.design_source_dictionary
//  ------------------------------------------------------------------------------
//  Begin RTL synthesis.
//  --------------------
//  Synthesized modules=1, Time=1.51 sec.
//  Note: There was 1 module selectively synthesized. There were also 5 sub-modules created by synthesis.
//        Use 'get_module -filter is_synthesized' to see them.
//        You can also use 'set_quick_synthesis_options -verbose on' to have the synthesis step report the
//        synthesized module name in the transcript as it is being synthesized.
//  ------------------------------------------------------------------------------
//  Warning: Rule FN1 violation occurs 1586 times
//  Warning: Rule FN4 violation occurs 8 times
//  Warning: Rule FP13 violation occurs 26 times
//  Flattening process completed, cell instances=967, gates=4837, PIs=77, POs=65, CPU time=0.06 sec.
//  ------------------------------------------------------------------------------
//  Begin circuit learning analyses.
//  --------------------------------
//  Learning completed, CPU time=0.00 sec.
//  ------------------------------------------------------------------------------
//  Begin ICL extraction.
//  ---------------------
//  ICL extraction completed, ICL instances=11, CPU time=0.10 sec.
//  ------------------------------------------------------------------------------
//  ------------------------------------------------------------------------------
//  Begin ICL elaboration and checking.
//  ICL extraction completed, ICL instances=11, CPU time=0.10 sec.
//  ------------------------------------------------------------------------------
//  ------------------------------------------------------------------------------
//  Begin ICL elaboration and checking.
//  ----------------------------------
//  ICL elaboration completed, CPU time=0.08 sec.
//  ------------------------------------------------------------------------------
//  Writing ICL file : ../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_design/corea.icl
//  Writing consolidated PDL file: ../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_design
/corea.pdl

//  Writing SDC file: ../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_design/corea.sdc
//  Writing DFT info dictionary: ../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_design/c
orea.dft_info_dictionary
//  command: #//
```

4. Phase 4

```
//  Writing SDC file: ../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_design/corea.sdc
//  Writing DFT info dictionary: ../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_design/c
orea.dft_info_dictionary
//  command: #//
//  command: #//         ---  |   |     /\       ----   ----              /
//  command: #//        |   | |   |    /  \    |      |                  / |
//  command: #//        |_ _| |- -|   /    \    ----  |----   ========  |__|__
//  command: #//        |     |   |  /------\       | |       ========     |
//  command: #//        |     |   | /        \  ----   ----                |
//  command: #create_patterns_spec
//  command: set spec1 [create_patterns_spec]
//  sub-command: create_patterns_specification
//  Creating '/PatternsSpecification(corea,first_insertion,signoff)'
//    Getting patterns specifications for the 'ijtag' instrument type
//    Getting patterns specifications for the 'memory_bist' instrument type
//  command: report_config_data $spec1

PatternsSpecification(corea,first_insertion,signoff) {
  AdvancedOptions {
    ConstantPortSettings {
      scan_en : 0;
    }
  }
  Patterns(ICLNetwork) {
    ICLNetworkVerify(corea) {
    }
  }
  Patterns(MemoryBist_P1) {
    ClockPeriods {
      clkb : 13.2ns;
      clka : 10.0ns;
    }
    TestStep(run_time_prog) {
      MemoryBist {
          run_mode : run_time_prog;
          reduced_address_count : on;
          Controller(corea_first_insertion_tessent_mbist_c1_controller_inst) {
            DiagnosisOptions {
              compare_go : on;
              compare_go_id : on;
            }
          }
          Controller(corea_first_insertion_tessent_mbist_c2_controller_inst) {
            DiagnosisOptions {
              compare_go : on;
              compare_go_id : on;
            }
          }
        }
      }
    }
  }
  Patterns(MemoryBist_ParallelRetentionTest_P1) {
    ClockPeriods {
      clkb : 13.2ns;
      clka : 10.0ns;
    }
    TestStep(ParallelRetentionTest) {
      MemoryBist {
        run_mode : hw_default;
        parallel_retention_time : 0;
        reduced_address_count : on;
        Controller(corea_first_insertion_tessent_mbist_c1_controller_inst) {
          parallel_retention_group : 1;
          DiagnosisOptions {
            compare_go_id : on;
          }
```

```
        Controller(corea_first_insertion_tessent_mbist_c2_controller_inst) {
          parallel_retention_group : 1;
          DiagnosisOptions {
            compare_go_id : on;
          }
        }
      }
    }
  }
}
//  command: process_patterns_specification
//
//  Begin processing of /PatternsSpecification(corea,first_insertion,signoff)
//
//    Processing of /PatternsSpecification(corea,first_insertion,signoff)/Patterns(ICLNetwork)
//
//      Creation of pattern 'ICLNetwork'
//        Solving ICLNetworkVerify(corea)
//
//      Writing pattern file '../tsdb_outdir/patterns/corea_first_insertion.patterns_signoff/ICLNetwork.v'
//
//    Processing of /PatternsSpecification(corea,first_insertion,signoff)/Patterns(MemoryBist_P1)
//      Processing of TestStep(run_time_prog) instrument 'memory_bist'
//
//      Creation of pattern 'MemoryBist_P1'
//        Solving TestStep(run_time_prog)
//
//      Writing pattern file '../tsdb_outdir/patterns/corea_first_insertion.patterns_signoff/MemoryBist_P1.v'
//
//    Processing of /PatternsSpecification(corea,first_insertion,signoff)/Patterns(MemoryBist_ParallelRetentionT
est_P1)
//      Processing of TestStep(ParallelRetentionTest) instrument 'memory_bist'
//
//      Creation of pattern 'MemoryBist_ParallelRetentionTest_P1'
//        Solving TestStep(ParallelRetentionTest)
//      Writing pattern file '../tsdb_outdir/patterns/corea_first_insertion.patterns_signoff/MemoryBist_Parallel
RetentionTest_P1.v'
//      Writing simulation data dictionary file '../tsdb_outdir/patterns/corea_first_insertion.patterns_signoff/
simulation.data_dictionary'
//
//  Done  processing of /PatternsSpecification(corea,first_insertion,signoff)
//
//  Writing configuration data file '../tsdb_outdir/patterns/corea_first_insertion.patterns_spec_signoff'.
//  command: write_design_import_script -use_relative_path_to . -replace
//  Writing file 'corea.dc_shell_import_script'.
```

5. Phase 5

```
//  command: #//
//  command: #//         ---  |   |     /\       ----   ----             ----
//  command: #//        |   | |   |    /  \    |      |                 |
//  command: #//        |_ _| |- -|   /    \    ----  |----   ========  |___
//  command: #//        |     |   |  /------\       | |       ========      |
//  command: #//        |     |   | /        \  ----   ----               ____|
//  command: set_simulation_library_sources -v ../../library/adk.v -y ../../library/mems -extension v
//  command: report_simulation_library_sources
//
//  List of -v/-y files and directories
//  type  path                                                                  file extensions
//  ----  ------------------------------------------------------------------  ---------------
//  file  ../../library/adk.v
//  dir   ../../library/mems                                                   v v.gz
//  file  /home/tools/mentor/MENTOR_SOURCE/lnx-x86/lib64/hdleng/lib/dft_sim.v
//  command: run_testbench_simulations
Starting 3 simulations for ./simulation_outdir/corea_first_insertion.simulation_signoff
//  Waiting for the simulation(s) to complete

unscheduled 0 queued 0 running 0 pass 3 fail 0
```

Step 2: Synthesis

```
/home/vinayakp/aug23/level3/Lab1/synthesis>>dc_shell -f synthesis.tcl

                        Design Compiler Graphical
                              DC Ultra (TM)
                               DFTMAX (TM)
                           Power Compiler (TM)
                              DesignWare (R)
                              DC Expert (TM)
                            Design Vision (TM)
                            HDL Compiler (TM)
                            VHDL Compiler (TM)
                               DFT Compiler
                            Design Compiler(R)

                Version S-2021.06-SP2 for linux64 - Aug 24, 2021

                    Copyright (c) 1988 - 2021 Synopsys, Inc.
   This software and the associated documentation are proprietary to Synopsys,
 Inc. This software may only be used in accordance with the terms and conditions
 of a written license agreement with Synopsys, Inc. All other use, reproduction,
   or distribution of this software is strictly prohibited.  Licensed Products
     communicate with Synopsys servers for the purpose of providing software
    updates, detecting software piracy and verifying that customers are using
    Licensed Products in conformity with the applicable License Key for such
  Licensed Products. Synopsys will use information gathered in connection with
    this process to deliver software updates and pursue software pirates and
                                 infringers.

 Inclusivity & Diversity - Visit SolvNetPlus to read the "Synopsys Statement on
             Inclusivity and Diversity" (Refer to article 000036315 at
                         https://solvnetplus.synopsys.com)
```

```
Initializing...
sh mkdir -p -v outputs
set design_name corea
corea
## Defind the library files
set target_library "../../library/adk.db"
../../library/adk.db
set link_library "../../library/adk.db $target_library"
../../library/adk.db ../../library/adk.db
read_db $target_library
Loading db file '/home/vinayakp/aug23/level3/library/adk.db'
Loading db file '/home/tools/synopsys/oct2021/syn/S-2021.06-SP2/libraries/syn/gtech.db'
Loading db file '/home/tools/synopsys/oct2021/syn/S-2021.06-SP2/libraries/syn/standard.sldb'
  Loading link library 'adk_typ'
  Loading link library 'gtech'
Loading db file '/home/vinayakp/aug23/level3/library/adk.db'
Warning: Overwriting design file '/home/vinayakp/aug23/level3/library/adk.db'. (DDB-24)
Loaded 0 designs.
# Bus naming style for Verilog
set bus_naming_style {%s[%d]}
%s[%d]
# Read input design files
source ../mbist_insertion/${design_name}.dc_shell_import_script
Running PRESTO HDLC
Compiling source file ../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_design/modified_rtl
_files/corea.v
Warning:  ../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_design/modified_rtl_files/corea
.v:77: the undeclared symbol 'clkag1' assumed to have the default net type, which is 'wire'. (VER-936)
Warning:  ../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_design/modified_rtl_files/corea
.v:78: the undeclared symbol 'clkbg1' assumed to have the default net type, which is 'wire'. (VER-936)
Presto compilation completed successfully.
Running PRESTO HDLC
Compiling source file ../tsdb_outdir/instruments/corea_first_insertion_cells.instrument/corea_first_insertion_te
```

```
Compiling source file ../tsdb_outdir/instruments/corea_first_insertion_cells.instrument/corea_first_insertion_te
ssent_posedge_synchronizer_reset.v
Presto compilation completed successfully.
Running PRESTO HDLC
Compiling source file ../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_te
ssent_sib_1.v
Compiling source file ../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_te
ssent_sib_2.v
Compiling source file ../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_te
ssent_sib_3.v
Compiling source file ../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_te
ssent_tdr_sri_ctrl.v
Presto compilation completed successfully.
Running PRESTO HDLC
Compiling source file ../tsdb_outdir/instruments/corea_first_insertion_mbist.instrument/corea_first_insertion_te
ssent_mbist_bap.v
Compiling source file ../tsdb_outdir/instruments/corea_first_insertion_mbist.instrument/corea_first_insertion_te
ssent_mbist_c1_controller.v
Compiling source file ../tsdb_outdir/instruments/corea_first_insertion_mbist.instrument/corea_first_insertion_te
ssent_mbist_c1_interface_m1.v
Compiling source file ../tsdb_outdir/instruments/corea_first_insertion_mbist.instrument/corea_first_insertion_te
ssent_mbist_c2_controller.v
Compiling source file ../tsdb_outdir/instruments/corea_first_insertion_mbist.instrument/corea_first_insertion_te
ssent_mbist_c2_interface_m1.v
Presto compilation completed successfully.
1
```

```
# Synthesize the top module
elaborate ${design_name}
Running PRESTO HDLC

Inferred memory devices in process
        in routine corea line 80 in file
                '../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_design/modified_rtl_file
s/corea.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      rsta_reg       | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine corea line 87 in file
                '../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_design/modified_rtl_file
s/corea.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      rstb_reg       | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine corea line 94 in file
                '../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_design/modified_rtl_file
s/corea.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      rstc_reg       | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
===============================================================================


Inferred memory devices in process
        in routine corea line 102 in file
                '../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_design/modified_rtl_file
s/corea.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      ffa4_reg       | Flip-flop |  16   |  Y  | N  | Y  | N  | N  | N  | N  |
|      ffa4_reg       | Flip-flop |  16   |  Y  | N  | N  | Y  | N  | N  | N  |
|      ffa2_reg       | Flip-flop |  32   |  Y  | N  | N  | Y  | N  | N  | N  |
|      ffa3_reg       | Flip-flop |  16   |  Y  | N  | N  | Y  | N  | N  | N  |
|      ffa3_reg       | Flip-flop |  16   |  Y  | N  | Y  | N  | N  | N  | N  |
|      ffa1_reg       | Flip-flop |  32   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine corea line 132 in file
                '../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_design/modified_rtl_file
s/corea.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      ffb4_reg       | Flip-flop |  16   |  Y  | N  | Y  | N  | N  | N  | N  |
|      ffb4_reg       | Flip-flop |  16   |  Y  | N  | N  | Y  | N  | N  | N  |
|      ffb2_reg       | Flip-flop |  32   |  Y  | N  | N  | Y  | N  | N  | N  |
|      ffb3_reg       | Flip-flop |  16   |  Y  | N  | N  | Y  | N  | N  | N  |
|      ffb3_reg       | Flip-flop |  16   |  Y  | N  | Y  | N  | N  | N  | N  |
|      ffb1_reg       | Flip-flop |  32   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
```

```
Inferred memory devices in process
        in routine corea line 161 in file
                '../tsdb_outdir/dft_inserted_designs/corea_first_insertion.dft_inserted_design/modified_rtl_file
s/corea.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      ffc1_reg       | Flip-flop |  16   |  Y  | N  | N  | Y  | N  | N  | N  |
|      ffc1_reg       | Flip-flop |  16   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully. (corea)
Elaborated 1 design.
Current design is now 'corea'.
Information: Building the design 'SYNC_1R1W_16x8'. (HDL-193)
Warning: Cannot find the design 'SYNC_1R1W_16x8' in the library 'WORK'. (LBR-1)
Information: Building the design 'corea_first_insertion_tessent_sib_1'. (HDL-193)

Inferred memory devices in process
        in routine corea_first_insertion_tessent_sib_1 line 73 in file
                '../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_tessent
_sib_1.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|    sib_latch_reg    | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
===============================================================================
```

```
Inferred memory devices in process
        in routine corea_first_insertion_tessent_sib_1 line 73 in file
                '../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_tessent
_sib_1.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|    sib_latch_reg    | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine corea_first_insertion_tessent_sib_1 line 80 in file
                '../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_tessent
_sib_1.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|  to_enable_int_reg  | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine corea_first_insertion_tessent_sib_1 line 89 in file
                '../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_tessent
_sib_1.v'.
===============================================================================
|    Register Name    | Type  | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|   retiming_so_reg   | Latch |   1   |  N  | N  | N  | N  | -  | -  | -  |
===============================================================================
```

```
Inferred memory devices in process
        in routine corea_first_insertion_tessent_sib_1 line 89 in file
                '../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_tessent
_sib_1.v'.
===============================================================================
|    Register Name    | Type  | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|   retiming_so_reg   | Latch |   1   |  N  | N  | N  | N  | -  | -  | -  |
===============================================================================

Inferred memory devices in process
        in routine corea_first_insertion_tessent_sib_1 line 95 in file
                '../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_tessent
_sib_1.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       sib_reg       | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine corea_first_insertion_tessent_sib_1 line 118 in file
                '../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_tessent
_sib_1.v'.
```

```
Inferred memory devices in process
        in routine corea_first_insertion_tessent_sib_1 line 118 in file
                '../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_tessent
_sib_1.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|   ltest_to_si_reg   | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
| ltest_ce_se_ue_reg  | Flip-flop |   2   |  Y  | N  | N  | N  | N  | N  | N  |
|  ltest_to_sel_reg   | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
| ltest_to_reset_reg  | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine corea_first_insertion_tessent_sib_1 line 168 in file
                '../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_tessent
_sib_1.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|    occ_ctrl_reg     | Flip-flop |   2   |  Y  | N  | N  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine corea_first_insertion_tessent_sib_1 line 179 in file
                '../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_tessent
_sib_1.v'.
===========================================================================================
|      Register Name      |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===========================================================================================
| occ_ctrl_so_retimed_reg | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
===========================================================================================


Inferred memory devices in process
        in routine corea_first_insertion_tessent_sib_1 line 179 in file
                '../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_tessent
_sib_1.v'.
===========================================================================================
|      Register Name      |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===========================================================================================
| occ_ctrl_so_retimed_reg | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
===========================================================================================

Inferred memory devices in process
        in routine corea_first_insertion_tessent_sib_1 line 198 in file
                '../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_tessent
_sib_1.v'.
===============================================================================
|      Register Name       | Type  | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
| retiming_ltest_to_si_reg | Latch |   1   |  N  | N  | N  | N  | -  | -  | -  |
===============================================================================

Inferred memory devices in process
        in routine corea_first_insertion_tessent_sib_1 line 203 in file
                '../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_tessent
_sib_1.v'.


===============================================================================
|     Register Name     | Type  | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
| ltest_so_retiming_reg | Latch |   1   |  N  | N  | N  | N  | -  | -  | -  |
===============================================================================
Presto compilation completed successfully. (corea_first_insertion_tessent_sib_1)
Information: Building the design 'corea_first_insertion_tessent_sib_2'. (HDL-193)

Inferred memory devices in process
        in routine corea_first_insertion_tessent_sib_2 line 35 in file
                '../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_tessent
_sib_2.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|    sib_latch_reg    | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine corea_first_insertion_tessent_sib_2 line 42 in file
                '../tsdb_outdir/instruments/corea_first_insertion_ijtag.instrument/corea_first_insertion_tessent
_sib_2.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|  to_enable_int_reg  | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
===============================================================================
```

```
                 Name                                                    Total
-------------------------------------------------------------------------------
Inputs/Outputs                                                          135
    Multiply driven inputs (LINT-6)                                       2
    Unconnected ports (LINT-28)                                          34
    Feedthrough (LINT-29)                                                35
    Shorted outputs (LINT-31)                                            28
    Constant outputs (LINT-52)                                           36

Cells                                                                    37
    Cells do not drive (LINT-1)                                           3
    Connected to power or ground (LINT-32)                               27
    Nets connected to multiple pins on same cell (LINT-33)                7

Nets                                                                     19
    Unloaded nets (LINT-2)                                               18
    Multiply driven net with constant driver (LINT-54)                    1

Tristate                                                                 53
    A tristate bus has a non tri-state driver (LINT-34)                  53
-------------------------------------------------------------------------------


  Optimization Complete
  ---------------------
1
# Report design results for TOP design
report_area > outputs/${design_name}_dc_script_report.out
report_constraint -all_violators -verbose >> outputs/${design_name}_dc_script_report.out
report_timing -path full -delay max >> outputs/${design_name}_dc_script_report.out
report_reference >> outputs/${design_name}_dc_script_report.out
write -f verilog -hierarchy -o outputs/${design_name}_top_gate.v
Warning: Design 'corea' has '1' unresolved references. For more detailed information, use the "link" command. (U
ID-341)
Writing verilog file '/home/vinayakp/aug23/level3/Lab1/synthesis/outputs/corea_top_gate.v'.
Warning: Verilog 'assign' or 'tran' statements are written out. (VO-4)
Warning: Verilog writer has added 5 nets to module corea_first_insertion_tessent_mbist_c1_controller using SYNOP
SYS_UNCONNECTED_ as prefix.  Please use the change_names command to make the correct changes before invoking the
 verilog writer.  (VO-11)
Warning: Verilog writer has added 5 nets to module corea_first_insertion_tessent_mbist_c2_controller using SYNOP
SYS_UNCONNECTED_ as prefix.  Please use the change_names command to make the correct changes before invoking the
 verilog writer.  (VO-11)
1
sh rm *.syn *.pvl *.mr
exit

Memory usage for this session 166 Mbytes.
Memory usage for this session including child processes 166 Mbytes.
CPU usage for this session 23 seconds ( 0.01 hours ).
Elapsed time for this session 24 seconds ( 0.01 hours ).
```

Step 3: Scan Insertion

```
1  set_context dft -scan -design_id corea_scan -hierarchical
2
3  set_tsdb_output_directory ../tsdb_outdir
4
5  read_cell_library ../../library/adk.tcelllib
6
7  read_verilog ../../library/mems/SYNC_1R1W_16x8.v -interface_only
8
9  read_verilog ../synthesis/outputs/corea_top_gate.v
10
11 read_design corea -design_id first_insertion -icl_only
12
13 set_current_design corea
14
15 set_design_level physical_block
16
17 delete_clocks -all
18
19 add_clocks 0 clka
20 add_clocks 0 clkb
21 add_clocks 0 clkc
22
23 ## change following in other atpg scripts too
24 add_clocks 1 rst
25
26 add_primary_inputs /rsta_reg/QB -cut
27 add_primary_inputs /rstb_reg/QB -cut
28 add_primary_inputs /rstc_reg/QB -cut
29
30 add_pin_constraints C0 /rsta_reg/QB
31 add_pin_constraints C0 /rstb_reg/QB
32 add_pin_constraints C0 /rstc_reg/QB
33
34 check_design_rules
35
36 set_wrapper_analysis_options -exclude_ports {*ijtag* *clk*}
37
38 set_dedicated_wrapper_cell_options on -ports rst
39
40 analyze_wrapper_cells
41
42 add_scan_mode int_mode -chain_length 50
43
44 add_scan_mode ext_mode -chain_length 32
45
46 analyze_scan_chains
47
48 insert_test_logic -write_in_tsdb on
49
```

Line 1: it's a hierarchical scan
Line 3: giving the path of the tsdb directory
Line 5: we are reading the library file and memory file
Line 9: reading the synthesized netlist
Line 11: from mbist insertion outputs directory whatever the output files is required for doing the scan insertion it will be read
Line 13:
Line 26 to 32: Cutpoints are mentioned and to temporarily clear the DRC's
Line 36: We are not adding the wrappers for IJTAG clks and EDT channels automatically the tool will ignore it.
Line 38: It will check if a primary input is driving a set or reset port of a flop then what the tool will do, the tool will add a dedicated wrapper for the primary inputs.
Line 40: If the PI is directly connected to a flop or PI is connected to a combo logic, then the tool will reuse the same flop as the shared wrapper flop, whichever PI which have got the shared wrapper then same thing apply for PI as well and after that tool will check whichever PI and PO have not been assigned with the wrappers and the tool will add a dedicated wrapper cell.

```
/home/vinayakp/aug23/level3/Lab1/scan_insertion>>tessent -shell -dofile corea_scan.tcl
]//  Warning: Tessent user documentation not found
//  Tessent Shell  2021.1    Fri Feb 26 20:45:56 GMT 2021
//                Copyright 2011-2021 Mentor Graphics Corporation
//
//                          All Rights Reserved.
//
//    THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION WHICH
//  IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS AND IS
//                        SUBJECT TO LICENSE TERMS.
//
//  Mentor Graphics software executing under x86-64 Linux on Fri Feb 02 12:05:21 IST 2024.
//  64 bit version
//  Host: vlsiguru (64168 MB RAM, 32191 MB Swap)
//
//  command: set_context dft -scan -design_id corea_scan -hierarchical
//  command: set_tsdb_output_directory ../tsdb_outdir
//  command: read_cell_library ../../library/adk.tcelllib
//  Reading DFT Library file ../../library/adk.tcelllib
//  Finished reading file ../../library/adk.tcelllib
//  command: read_verilog ../../library/mems/SYNC_1R1W_16x8.v -interface_only
//  command: read_verilog ../synthesis/outputs/corea_top_gate.v
//  command: read_design corea -design_id first_insertion -icl_only
//  command: set_current_design corea
//  Warning: 9 cases: Undriven net in netlist module
//  Warning: 61 cases: Net in netlist not connected
//  Note: Issue set_current_design with the -show_elaboration_warnings option to see more details about previous
```

```
//  ------------------------------------------------------------------------------
//  Begin ICL elaboration and checking.
//  ----------------------------------
//  ICL elaboration completed, CPU time=0.10 sec.
//  ------------------------------------------------------------------------------
//  command: set_design_level physical_block
//  command: delete_clocks -all
//  command: add_clocks 0 clka
//  command: add_clocks 0 clkb
//  command: add_clocks 0 clkc
//  command: ## change following in other atpg scripts too
//  command: add_clocks 1 rst
//  command: add_primary_inputs /rsta_reg/QB -cut
//  Warning: Primary input 'rsta_reg/QB_pport' is added at pin '/rsta_reg/QB'
//  command: add_primary_inputs /rstb_reg/QB -cut
//  Warning: Primary input 'rstb_reg/QB_pport' is added at pin '/rstb_reg/QB'
//  command: add_primary_inputs /rstc_reg/QB -cut
//  Warning: Primary input 'rstc_reg/QB_pport' is added at pin '/rstc_reg/QB'
//  command: add_pin_constraints C0 /rsta_reg/QB
//  command: add_pin_constraints C0 /rstb_reg/QB
//  command: add_pin_constraints C0 /rstc_reg/QB
//  command: check_design_rules
//  Warning: Rule FN1 violation occurs 86 times
//  Warning: Rule FN4 violation occurs 682 times
//  Flattening process completed, cell instances=5999, gates=9522, PIs=77+4(pseudo ports), POs=65, CPU time=0.06
 sec.
//  ------------------------------------------------------------------------------
//  Begin circuit learning analyses.
//  --------------------------------
//  Learning completed, CPU time=0.04 sec.
```

```
//  ---------------------------------------------------------------------------
//  Begin scan chain identification process, memory elements = 682,
//  sequential library cells = 682.
//  ---------------------------------------------------------------------------
//  Begin simulation of test_setup procedure with 23 cycles.
//  Simulation of test_setup procedure completed, CPU time=0.0 sec.
//  Begin simulation of auto-generated load_unload procedure.
//  Simulation of load_unload procedure completed, CPU time=0.0 sec.
//  Scan segment = /corea_first_insertion_tessent_sib_sti_inst/ltest_so successfully traced with scan_cells = 7.
//  7 scan cells have been identified in 1 scan segment.
//  Warning: 1 edge-triggered clock ports set to stable high. (D7)
//  Warning: Model 'nlatch' has no muxscan scan equivalent and is treated as nonscan model
//  ---------------------------------------------------------------------------
//  30 sequential library cells are treated as non-scan.
//  ---------------------------------------------------------------------------
//     8 sequential library cells missing mux-scan equivalent.
//     5 sequential library cells below hard module.
//    17 sequential library cells defined non-scan.
//  ---------------------------------------------------------------------------
//  Begin scannability rules checking for 642 sequential library cells
//  and 1 scan segment. The scan segment contains 10 additional cells.
//  ---------------------------------------------------------------------------
//  Note: There were 3 S7 violations (Potentially scannable cell that is not in the clock path is driven by a co
nstant value).
//  642 sequential library cells and 1 scan segment identified as scannable.
//  ---------------------------------------------------------------------------
//  Begin transparent latch checking for 11 latches.
//  ---------------------------------------------------------------------------
//  Warning: 1 latches not transparent due to unobservable. (D6)
//  Number transparent latches = 10.
//  ---------------------------------------------------------------------------
//  Begin scan clock rules checking.

//
//  7 scan clock/set/reset lines have been identified.
//  All scan clocks successfully passed off-state check.
//  317 sequential cells passed clock stability checking.
//  There were 23 clock rule C3 fails (clock may capture data affected by its captured data).
//  Note: Trailing edge triggered device can capture data affected by leading edge.
//  ---------------------------------------------------------------------------
//  32 non-scan memory elements are identified.
//  ---------------------------------------------------------------------------
//  18 non-scan memory elements are identified as TIE-0. (D5)
//   3 non-scan memory elements are identified as TIE-1. (D5)
//   1 non-scan memory element is   identified as TIE-X. (D5)
//  10 non-scan memory elements are identified as TLA.   (D5)
//  ---------------------------------------------------------------------------
//  ---------------------------------------------------------------------------
//  Begin shift register identification for 642 sequential library cells.
//  ---------------------------------------------------------------------------
//  Number of shift register flops recorded for scan insertion: 36 (5.28%)
//  Number of shift registers recorded for scan insertion: 17
//  Longest shift register has 3 flops.
//  Shortest shift register has 2 flops.
//  Potential number of nonscan flops to be converted to scan cells: 17
//  Potential number of scan cells to be converted to nonscan flops: 0
//  Number of targeted sequential library cells = 642
//  command: set_wrapper_analysis_options -exclude_ports {*ijtag* *clk*}
//  command: set_dedicated_wrapper_cell_options on -ports rst
//  command: analyze_wrapper_cells
//
//     Port information and user constraints:
//     --------------------------------------
//         Input ports:    77 total,     3 ignored,    10 excluded,     0 off,     0 on,    64 auto
//        Output ports:    65 total,     0 ignored,     1 excluded,     0 off,     0 on,    64 auto
//
```

```
//     Wrapper analysis summary:
//     -------------------------
//        64 flip-flops were converted into output shared wrapper cells.
//        64 flip-flops were converted into input shared wrapper cells.
//        Use report_wrapper_cells for more details.
//
//  command: add_scan_mode int_mode -chain_length 50
//  Automatically inferring '-enable_dft_signal int_mode' from the specified scan mode name.
//  Automatically inferring '-type internal' from the scan mode type (internal) associated with the enable DFT s
ignal 'int_mode'.
//  command: add_scan_mode ext_mode -chain_length 32
//  Automatically inferring '-enable_dft_signal ext_mode' from the specified scan mode name.
//  Automatically inferring '-type external' from the scan mode type (external) associated with the enable DFT s
ignal 'ext_mode'.
//  command: analyze_scan_chains
//  Chain allocation of 'int_mode' mode completed:
Distribution - populating 'int_mode' chains: 91.8% completed (estimated time remaining 0 secs)//        14 distr
ibuted chains of sizes ranging from 46 to 47
//  Chain allocation of 'ext_mode' mode completed:
Distribution - populating 'ext_mode' chains: 100.0% completed (estimated time remaining 0 secs)//         5 dist
ributed chains of sizes ranging from 26 to 27
//  command: insert_test_logic -write_in_tsdb on
============================
Test Logic Insertion Summary:
============================


  Structural Data:
  ----------------
                          Added top-level port count:           4
                                Added instance count:         191

  Logical Data:
  -------------
                Added clock gater control logic count:           2
                      Added input wrapper logic count:          64
                     Added output wrapper logic count:          64
                         Added pipelining logic count:           7
                           Added retiming logic count:          22
                    Added scan chain count (int_mode):          14
                    Added scan chain count (ext_mode):           5

//  Warning: Flattened model deleted.
//
//  Writing out netlist and related files in ../tsdb_outdir/dft_inserted_designs/corea_corea_scan.dft_inserted_d
esign
```

Step 4: ATPG

Intest:-

```
1  set_context patterns -scan
2
3  set_tsdb_output_directory ../../../tsdb_outdir
4
5  read_cell_library ../../../../library/adk.tcelllib
6
7  read_verilog ../../../../library/mems/SYNC_1R1W_16x8.v -interface_only
8
9  read_design corea -design_id  corea_scan
10
11 set_current_design corea
12
13 ## it will save the patterns with the current_mode set SA inside tsdb with an option of internal
14 set_current_mode SA_intest -type internal
15
16 ## This will get the constraints/constant values related to intest mode from tsdb post scan insertion
17 #fast_capture_mode off -> will enable SA constraints , making it on -> will automatically program the TDR's to TDF mode.
18 import_scan_mode int_mode -fast_capture_mode off
19
20 add_clocks 1 rst
21
22 add_primary_inputs /rsta_reg/QB -cut
23 add_primary_inputs /rstb_reg/QB -cut
24 add_primary_inputs /rstc_reg/QB -cut
25
26 add_pin_constraints C0 /rsta_reg/QB
27 add_pin_constraints C0 /rstb_reg/QB
28 add_pin_constraints C0 /rstc_reg/QB
29
30
31 add_black_boxes -mod SYNC_1R1W_16x8
33 ## hacking commands since EDT, OCC are not inserted in the design and also in this lab session clocks are not declared as
    -pulse_in_capture mode like how done in Lab0. So please enable the following switches to process the next steps of ATPG.
34          ## General Note: these clocks should not be declared as pulse_in_capture since there is no occ and wrappers are e
   nabled.
35
36 set_attribute_value {clka clkb clkc test_clock rst} -name is_excluded_from_isolation_constraints
37 set_drc_hand R7 warning
38
39 check_design_rules
40
41 set_fault_type stuck
42
43 create_patterns
44
45 write_tsdb_data -replace
46
47 system mkdir -p -v simulations
48
49 write_patterns /hdd2/home/vidishar/aug23/level3/Lab1/atpg/sa/intest/simulations/corea_int_mode_parallel.v -verilog -paral
   lel -replace -parameter_list {SIM_TOP_NAME parallel_TB SIM_KEEP_PATH 1}
50
```

Line 36 and 37: We have not inserted OCC, and we have also not declared the clock as -pulse in capture

Line 45: flat model, fault list, pat db patterns, tcd file … everything will write it out into the tsdb output directory.

```
                          Statistics Report
                           Stuck-at Faults
-----------------------------------------------------------------------
Fault Classes                          #faults          #faults
                                       (total)      (total relevant)
-----------------------------  ---------------- --------------------
  FU (full)                          44610             44027
  ---------------------------  ---------------- --------------------
  DS (det_simulation)              33140  (74.29%)       same  (75.27%)
  DI (det_implication)              5672  (12.71%)       same  (12.88%)
  PU (posdet_untestable)               1  ( 0.00%)       same  ( 0.00%)
  UU (unused)                       1150  ( 2.58%)       same  ( 2.61%)
  TI (tied)                          294  ( 0.66%)       same  ( 0.67%)
  BL (blocked)                       205  ( 0.46%)       same  ( 0.47%)
  RE (redundant)                     343  ( 0.77%)       same  ( 0.78%)
  AU (atpg_untestable)              3805  ( 8.53%)       3222  ( 7.32%)
-----------------------------------------------------------------------
Fault Sub-classes
  ---------------------------
  DI (det_implication)
    SCAN  (scan_path)               3369  ( 7.55%)       same  ( 7.65%)
    SEN   (scan_enable)              788  ( 1.77%)       same  ( 1.79%)
    CLK   (clock)                   1462  ( 3.28%)       same  ( 3.32%)
    SR    (set_reset)                  3  ( 0.01%)       same  ( 0.01%)
    DIN   (data_input)                 2  ( 0.00%)       same  ( 0.00%)
    MBIST                             48  ( 0.11%)       same  ( 0.11%)
  AU (atpg_untestable)
    BB    (black_boxes)               56  ( 0.13%)       same  ( 0.13%)
    PC*   (pin_constraints)         1114  ( 2.50%)       same  ( 2.53%)
    TC*   (tied_cells)               803  ( 1.80%)       same  ( 1.82%)
    MPO   (mask_po)                  564  ( 1.26%)       same  ( 1.28%)
    SEQ   (sequential_depth)         529  ( 1.19%)       same  ( 1.20%)
    IJTAG (ijtag)                    583  ( 1.31%)         deleted
   Unclassified                 156  ( 0.35%)      same  ( 0.35%)
  *Use "report_statistics -detailed_analysis" for details.
-----------------------------------------------------------------------
Coverage
  --------------------------
  test_coverage                        91.07%              92.33%
  fault_coverage                       87.00%              88.16%
  atpg_effectiveness                  100.00%             100.00%
-----------------------------------------------------------------------
#test_patterns                                                  266
  #basic_patterns                                                62
  #clock_sequential_patterns                                    204
#simulated_patterns                                             276
CPU_time (secs)                                                 6.1
-----------------------------------------------------------------------

//  command: write_tsdb_data -replace
//  Writing ../../../tsdb_outdir/logic_test_cores/corea_corea_scan.logic_test_core/corea.atpg_mode_SA_intest/cor
ea_SA_intest.tcd.gz
//  Writing ../../../tsdb_outdir/logic_test_cores/corea_corea_scan.logic_test_core/corea.atpg_mode_SA_intest/cor
ea_SA_intest.flat.gz
//  Writing ../../../tsdb_outdir/logic_test_cores/corea_corea_scan.logic_test_core/corea.atpg_mode_SA_intest/cor
ea_SA_intest_stuck.patdb
//  Writing ../../../tsdb_outdir/logic_test_cores/corea_corea_scan.logic_test_core/corea.atpg_mode_SA_intest/cor
ea_SA_intest_stuck.faults.gz
//  command: system mkdir -p -v simulations
//  command: write_patterns /hdd2/home/vidishar/aug23/level3/Lab1/atpg/sa/intest/simulations/corea_int_mode_para
llel.v -verilog -parallel -replace -parameter_list {SIM_TOP_NAME parallel_TB SIM_KEEP_PATH 1}
//  Error: File /hdd2/home/vidishar/aug23/level3/Lab1/atpg/sa/intest/simulations/corea_int_mode_parallel.v canno
t be created
```

Extest:-

```
set_context patterns -scan

set_tsdb_output_directory ../../../tsdb_outdir

read_cell_library ../../../../library/adk.tcelllib

read_verilog ../../../../library/mems/SYNC_1R1W_16x8.v -interface_only

read_design corea -design_id  corea_scan



set_current_design corea

## it will save the patterns/faults with the current_mode set SA inside tsdb with an option of internal
set_current_mode SA_extest -type external

## This will get the constraints/constant values related to intest mode from tsdb post scan insertion
#fast_capture_mode off -> will enable SA constraints , making it on -> will automatically program the TDR's to TDF mode.
import_scan_mode ext_mode -fast_capture_mode off

add_clocks 1 rst

add_primary_inputs /rsta_reg/QB -cut
add_primary_inputs /rstb_reg/QB -cut
add_primary_inputs /rstc_reg/QB -cut

add_pin_constraints C0 /rsta_reg/QB
add_pin_constraints C0 /rstb_reg/QB
add_pin_constraints C0 /rstc_reg/QB


add_black_boxes -mod SYNC_1R1W_16x8
    _     _               _    _                                                                  7,33          Top

## hacking commands since EDT, OCC are not inserted in the design and also in this lab session clocks are not declared as -pulse_in_capture mode like how done in Lab0. So please enable the following switches to process the next steps of ATPG.
        ## General Note: these clocks should not be declared as pulse_in_capture since there is no occ and wrappers are enabled.

set_attribute_value {clka clkb clkc test_clock rst} -name is_excluded_from_isolation_constraints
set_drc_hand R7 warning

check_design_rules

set_fault_type stuck

create_patterns

write_tsdb_data -replace

system mkdir -p -v simulations

write_patterns /hdd2/home/vidishar/aug23/level3/Lab1/atpg/sa/extest/simulations/corea_int_mode_parallel.v -verilog -parallel -replace -parameter_list {SIM_TOP_NAME parallel_TB SIM_KEEP_PATH 1}

## to get the overall coverage combined with both intest and extest , here extest faults already avaialble in this tessent run , so just loading the previous intest faults list which consists of all fault categories. We can use below commands
read_faults  ./../../../tsdb_outdir/logic_test_cores/corea_corea_scan.logic_test_core/corea.atpg_mode_SA_intest/corea_SA_intest_stuck.faults.gz -merge

report_statis -det
```