ASSEMBLY AND PACKAGING TECHNOLOGY

Lecture 1

5/8/25

Table of Contents

- → Introduction
- → Housing Technologies : Packages for 1st, 2nd Level
- → Substrates
- → Assembly Technologies
- → Interconnection Technologies
- → Construction, design and simulation in APT

* The power of microelectronics : in area of $30.00\ mm^2$ 100 million Transistors / mm^2

From the first transistor to super computers.
Built at Bell Laboratories by John Bardeen, William Shockley and Walter Brattain 1948
Supercomputer : IBM Power 9 with 150 petaflops

Feature Size : Actual node size 10 - 14 nm

Gordon Moore <cofounder of INTEL>

MOORE'S LAW

Moore's law describes the empirical regularity that the number of transistors on IC doubles approximately every two years.

→ This advancement is important for other aspects of technological progress in computing - such as processing speed or price of computers.

"No of transistors per chip doubles every two years due in large part to advanced material processing techniques"

AMD64 : Standard for 64 bit

X86 : instruction set for 32 bit processes
X64 : extension of x86 for 64 bit processes.

10nm

Intel 4004 : Employee 40's 4th iteration
Intel 80808 : Double the computing power
Intel 8086 : Iteration 86 of original design
:

Apple A13 : Iphone 11 Pro.

Lithography is the only process defining technology that determines the scale and size.

ASML (Netherlands)

Size Reduction and Close to Chip Assembly

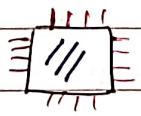
* Surface Mount Technology (still relevant though)
  - → pick and place assembly and direct soldering onto Printed Circuit Boards [PCB's]
  - → Component miniaturization
* Flip-Chip Assembly (Standard new tech.) → most complex design use this
  - → solder balls on the semiconductor (10-30 μm diameter)
  - → flipping of the component
  - → reflow soldering

Packaging Concepts for electronic systems
History and Current Trends

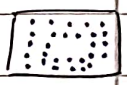
As tech evolved - we were able to reduce the size of the package compared to chip. This is called package form factor. [PFF]

$$\text{Package Form Factor} = \frac{\text{Package Area}}{\text{Chip Area}}$$

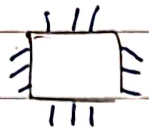
Quad Flat Package

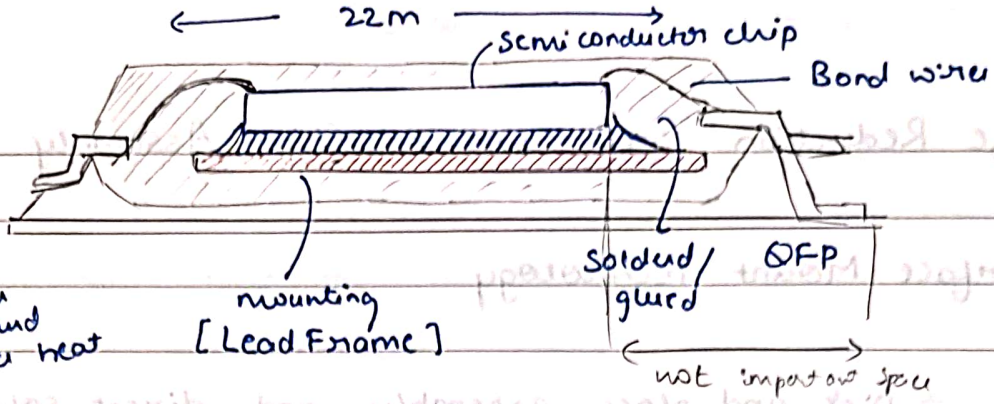


Ball Grid Array

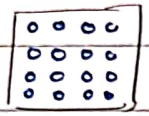


Chips-Scale Package

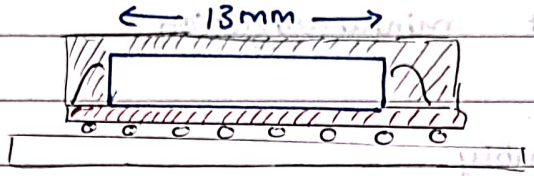




QFP : PFF ~ 5·5



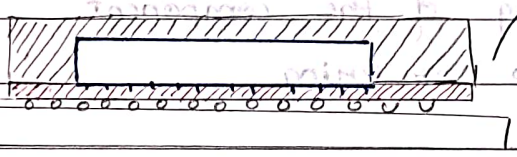
BGA



Ball Grid Array

BGA : PFF ~ 2

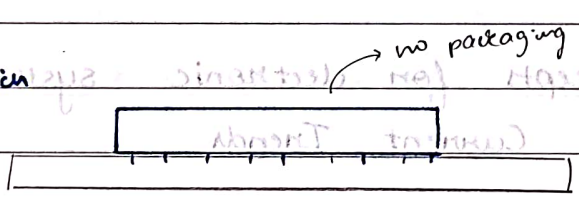
CSP :



Chips Scale Packaging

PFF ~ 1,2

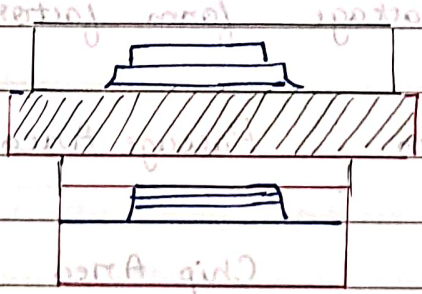
WLP fan in



Wafer level packaging

PFF = 1

Stacking devices : PFF < 1



9.34 mm

Advanced Packaging

(i) Flip Chip

1> CSP
- → CUF (Capillary)
- → NCP (Paste)
- → NCF (Film)

2> BGA
- → CUF (Capillary)
- → Lid Attach (TIM1)

3> POP → WIA (Warpage Improvement Adhesive)

(ii) Wafer Level

1> Fan-In
- → BSP (Backside Prot)
- → FSP (Frontside Prot)

2> UV-WBC

3> Fan-Out
- → DAF (Film, Face Up)
- → LCM (Liquid Molding)

(iii) Panel Level

1> Memory 3D TSV
- → NCF (WAUF)
- → LCM (Liquid Molding)

Integration Concepts

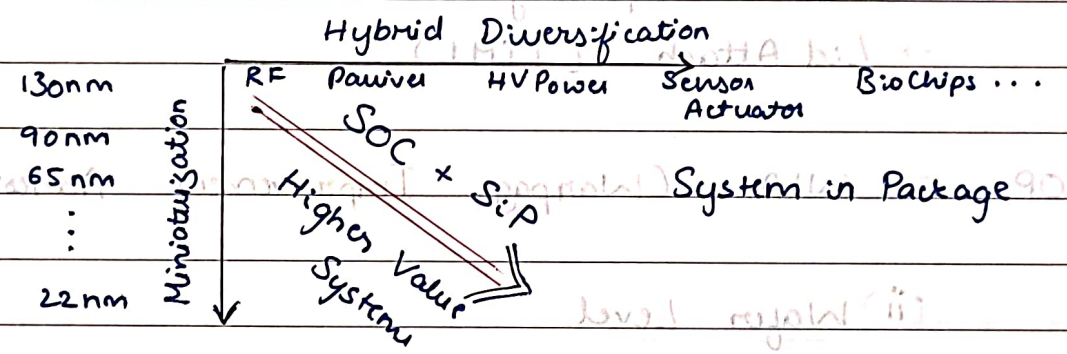
→ technology has advanced from monolithic → hybrid integration

→ Monolithic [More Moore]

The concept uses parallelization and scale-up rather than new concepts

→ Hybrid [More than Moore]

The concept combines new techniques and breaks classical Moore scaling.



Example :

Example of a hybrid packaging concept for hybrid electronic system.

→ ABS [Antilock Braking System] control module with a multifunctional plastic packaging

→ Levels of integration

* Component level – which components interact with other components
* Assembly level – how components interact via packaging
* System level – how do they interact with the environment via the packaging