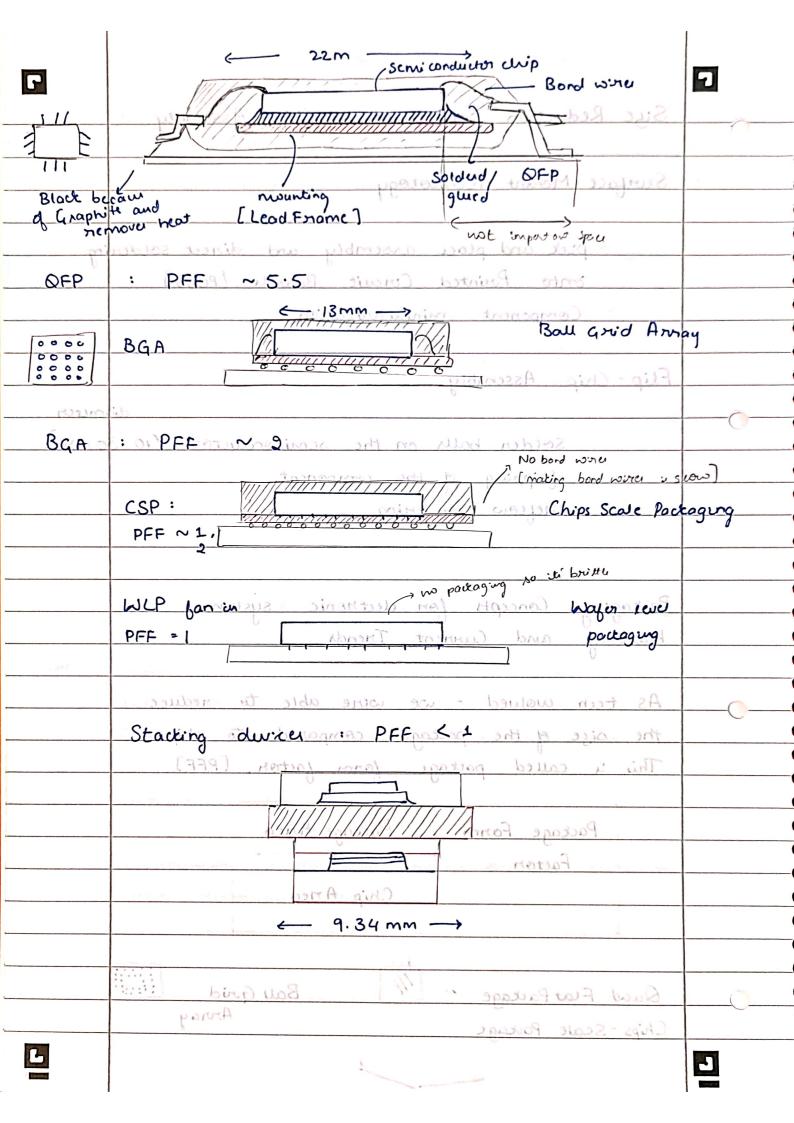
	Granden Hoene copanda & INTEL	Ð
6	THAT WE STORY	
	ASSEMBLY AND PACKAGING	
	TECHNOLOGY	· · · · · · · · · · · · · · · · · · ·
	the time of the back of the back of the time of	
5 8 25	Lecture 1 1	
6	Table of Contents " programme institution	1
	→ Introduction → Housing Technologies: Packages for 1st, 2 rd	Level
	→ Substratu → Assembly Technologies	
•	→ Interconnection Technologies → Construction, design and simulation in APT	
	Total 4004 : Employer 40: 4th : tenotion Total 80808 : Dauby the conquiting payon at all	MROL
*	The power of microelectronics : In area of 30.00	
	From the first transistor to super computers.	
	Built at Bell Labonatories by John Bardeen William Shockley and Walter Brattain 1948	
	Supercomputer: IBM Power 9 with 150 petaglor	2
	Feature Size: Actual node size 10-14 nm	
므		<u> </u>

G	Goordon Hoote (cofourdu & INTEL >	2
	MOORE'S LAW	
	Moone's law describe the emperical	,
	requestry that the number of transitory on IC	
	double approximately every two years.	ADS.
→	This advancement is important for other aspects	Primary of
,	of technological progress in computing - such as	X
	procuing speed or price q computou.	- 1 - -
	Lecture L	
	" No of transitory per chip doubles every two	5/8/25
	years due in large part to advanced material	
	procuing technique " Hostrod to sadd	3.1
	Intrusduction) /*=-
Level	AMD641 Standard for 264 bits possest	40-
	Substratu	10F
	X86: instructionantset ford32bit procuu	
	X64: entension q x86 gor 64 bit procene	
	Construction design and simulation in API	
MHOI	Intel 4004: Employee 40's 4th iteration	
	Intel 80808: Double the computing power	
- mm C	Intel 18086 : 1 Ituration en 860 of original design	X
	100 million Thankiton / mm2	
•	Apple A13: Iphone 11 Pro.	
	Enon the pinct translation to super compilers.	
-	Lithography is the only process defining technology	
	that Platerminer the scale and size of	
2	ASMC (Netherlands) C. P. MOCIOS MAI : MOTIONALINAS	
Ø —i	Forman Size: Artual made size 10-14 pm	

	gials realisate junes.	
	01-c 608	
6	Size Reduction and Close to Chip Assembly	2
	Swiface Mount Technology	11. 34 1 16
	Strate a book to the original	are the
	onto Printed Circuit Boards [PCB's]	•
	Component miniaturization	
L.	4.3.4.4.4.4.4.4.4.4.4.4.4.4.4.4.4.4.4.4	2 8 7 1. 2 7 3 7
*	Flip-Chip Assembly -> most compuse design use this	49 9 9
6		much
	-> solder balls on the semiconductoria (10-3	OHM
	dipping of the component	
Luse.	and start reflow soldwing : 920	
31 ·	PEG ~ 100 months and a second super land of ~ 339	
,	P. A. C.	
	Packaging Concepts for cleetronic systems 9161	
. 9	History and Countert Triends	
	As teen wowed - we were able to reduce	
,	the size of the package compared to chip	
3.5	This is called package form factor. [PFF]	
3.2	Package Form Package Arrea	
	Factor = F	
	Chip Astea	
	6-9.34 MM	
	Quad Flat Package = Bau Grid Annou	
	Chips - Scale Pockage Array	
		0



G		
	Advanced Packaging	
	in Flips Chip basers on presented	~ -
1>	CSP [-month anoth] sufficeed	* .
	→ NCP (Paste) new months and to	
	- NCF (Film) 1 mott mott) birdutt	4.00
ع>	BGA Scott Scotting Scotting Comment of the BGA	
	→ Lid Attach (TTM1) indyH iquisis nouse possell prouse is most	
3>	Since the second of the second	e)
	in Wager Level and marry?	
1>	Fan - In -> BSP (Backside Prot)	
_	FSP (Frontside Prot)	
2>	Example descriptions against UV. My temperature by the temperature of	
3>	Fan - Out - DAF (Film, Face Up)	<u> </u>
*	Early Panel Level distribution of the	<u>@-</u>
	Memory 3D TSV TO NCF (WAUF)	
1.7	MYMORU SD 100	

Integration Concepts technology has advanced from monolithic -> hybrid integration Monolithic [Mone Moone] The concept usu paraudization and scale-up nather than new conceptions 9011 Hybrid [More than Moore] The concept combine new technique and break clarsical Moone Scaling. Hybrid Diversification

RF Pawie HVPower Senson

Actuator BioChips ... 130nm System in Package System on Chip (Frantside Pret) Example q a hybrid packaging concept for hybrid electronic system. Fan - Out - DAF (Film Face up) ABS [Antilock Broking System] control module with a multifunctional plastic packaging Levels of integration has been in * Component level - which component interest with other component * Assembly level - how component interoca via packaging System birlevel - M how do they interact with the environment via the pockaging