DESIGN AND ANALYSIS OF CMOS LOGIC GATES IN CADENCE VIRTUOSO TOOL

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INTRODUCTION

Overview of CMOS Technology:

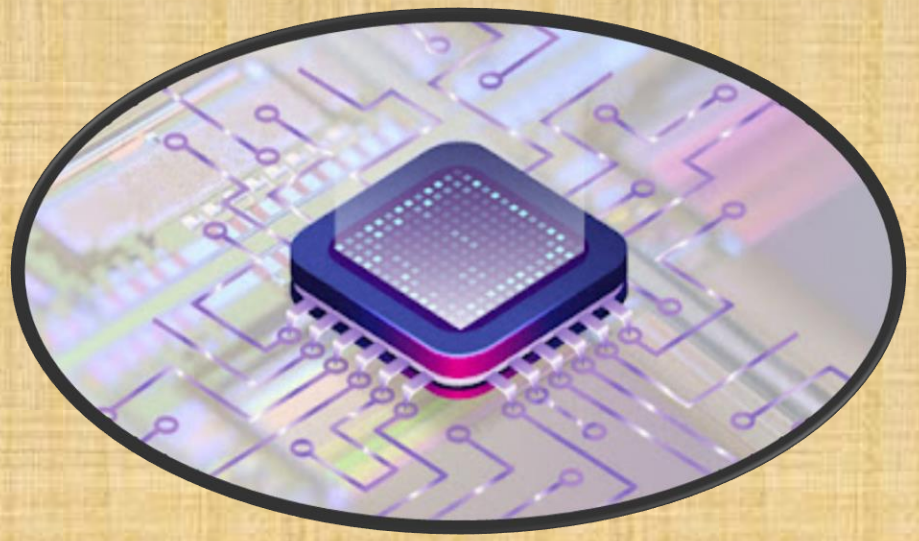
- CMOS (Complementary Metal-Oxide-Semiconductor) combines NMOS and PMOS transistors to create efficient digital logic circuits.
- Widely used in VLSI design due to its low power consumption and high noise immunity.

Objectives of the Presentation:

- Focuses on the design and transient analysis of basic logic gates (Inverter, OR, NOR, AND, NAND) using CMOS technology.
- Showcasing the use of Cadence Virtuoso for CMOS circuit design and simulation.

LITERATURE WORK

- **CMOS Fundamentals:**
  - CMOS technology is preferred due to its low power consumption and high noise immunity.
  - NMOS transistors are used to pull the output down (0), while PMOS transistors are used to pull the output up (1).
- **Recent Trends in CMOS VLSI:**
  - **Scaling challenges**: As transistors shrink, problems like short-channel effects and leakage currents increase.
  - **Advancements**: Innovations like FinFET, SOI (Silicon-On-Insulator) have helped overcome some scaling limitations.



Name	Graphical Symbol	Algebraic Function	Truth Table
AND		$F = A \cdot B$ or $F = AB$	A B | F 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1
OR		$F = A + B$	A B | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1
NOT		$F = \overline{A}$ or $F = A'$	A | F 0 | 1 1 | 0
NAND		$F = \overline{AB}$	A B | F 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0
NOR		$F = \overline{A + B}$	A B | F 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0

METHODOLOGY

- **Designing CMOS Logic Gates in Cadence Virtuoso:**

  Step-by-step design of Inverter, OR, NOR, AND, NAND gates using NMOS and PMOS transistors.

- **Simulation and Transient Analysis:**

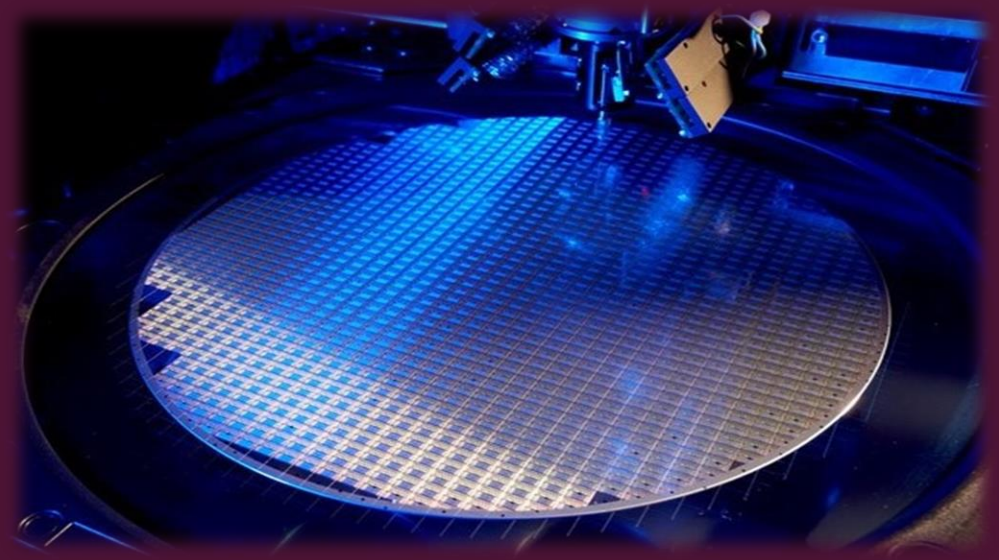
  Transient analysis is performed to observe the switching behavior of the gates, showing how the output transitions over time with varying inputs.

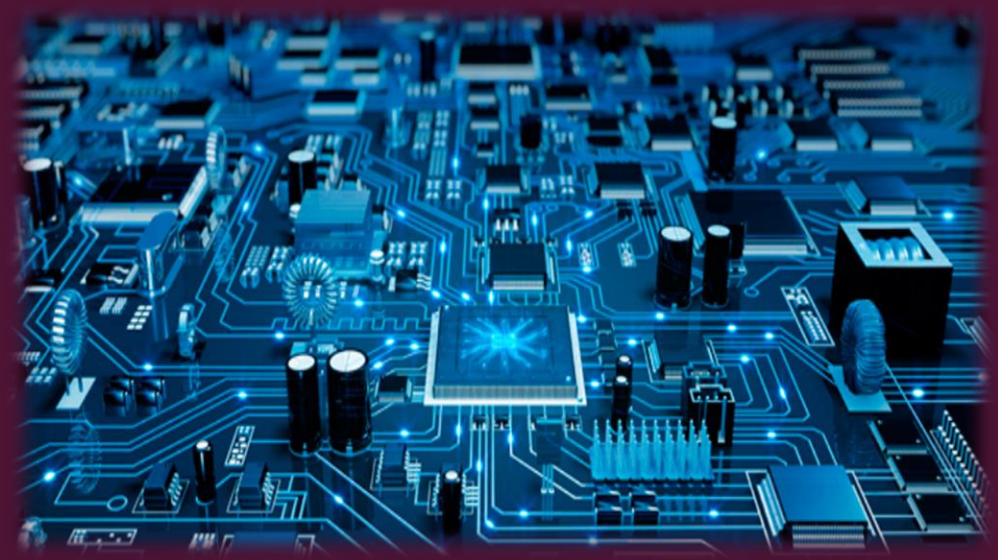
- **Tools used:**

  Cadence Virtuoso for schematic capture and simulation.

DESIGN & RESULTS

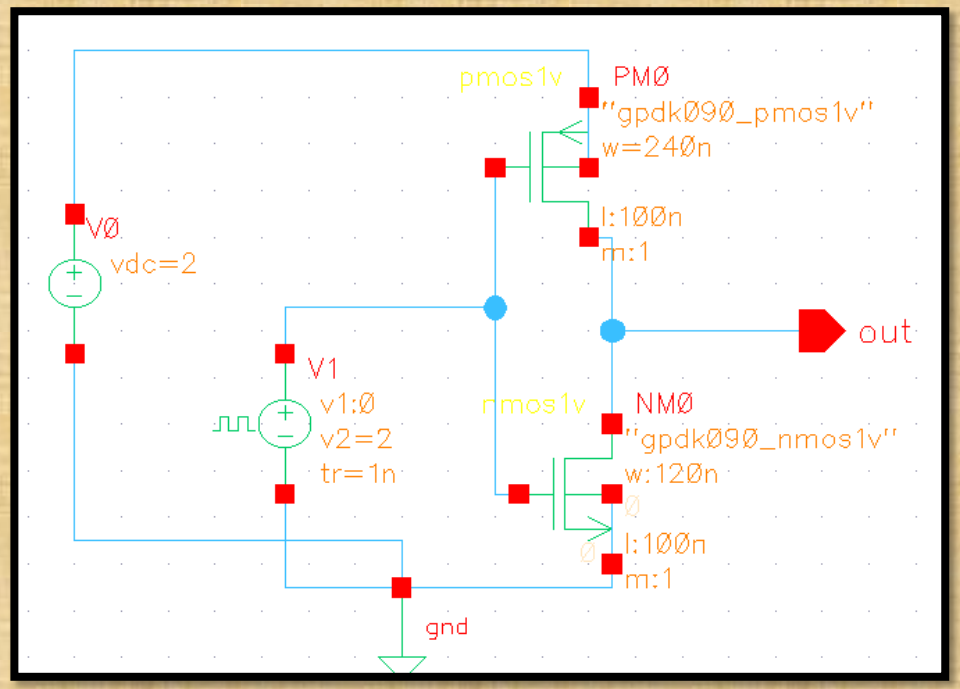
BASIC LOGIC GATES (INVERTER, OR, NOR, AND, NAND)



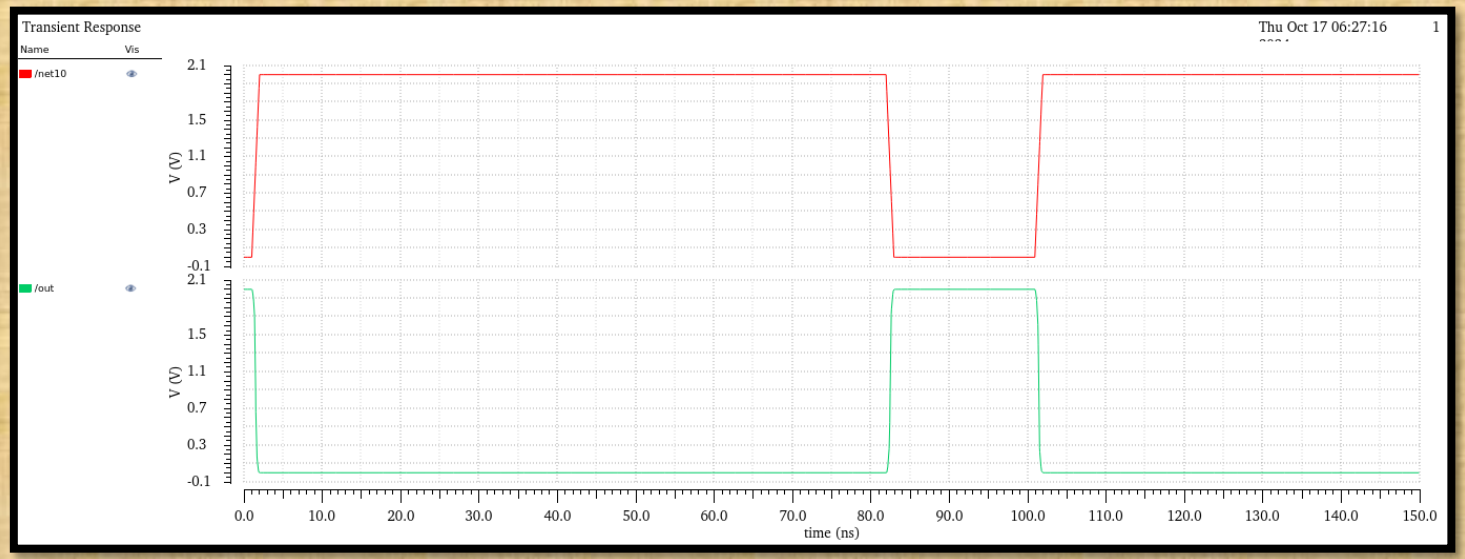


INVERTER

1PMOS &1 NMOS connected in series



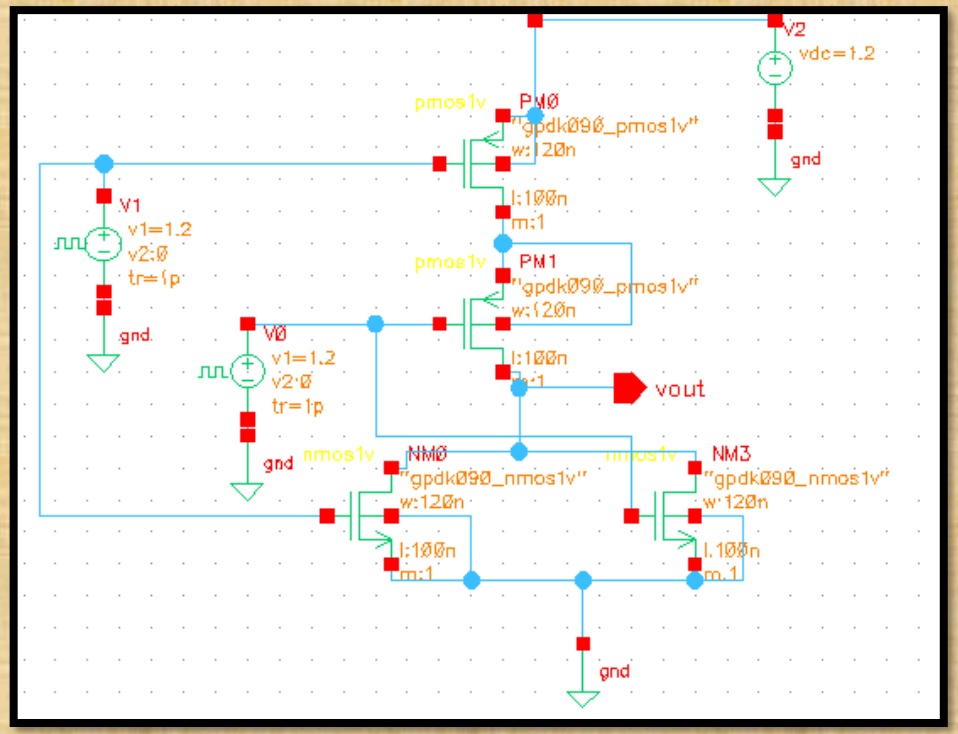
- Graph showing the input switching between 0 and 1, with corresponding output switching inversely.
- Inverter shows perfect switching behavior with minimal delay.

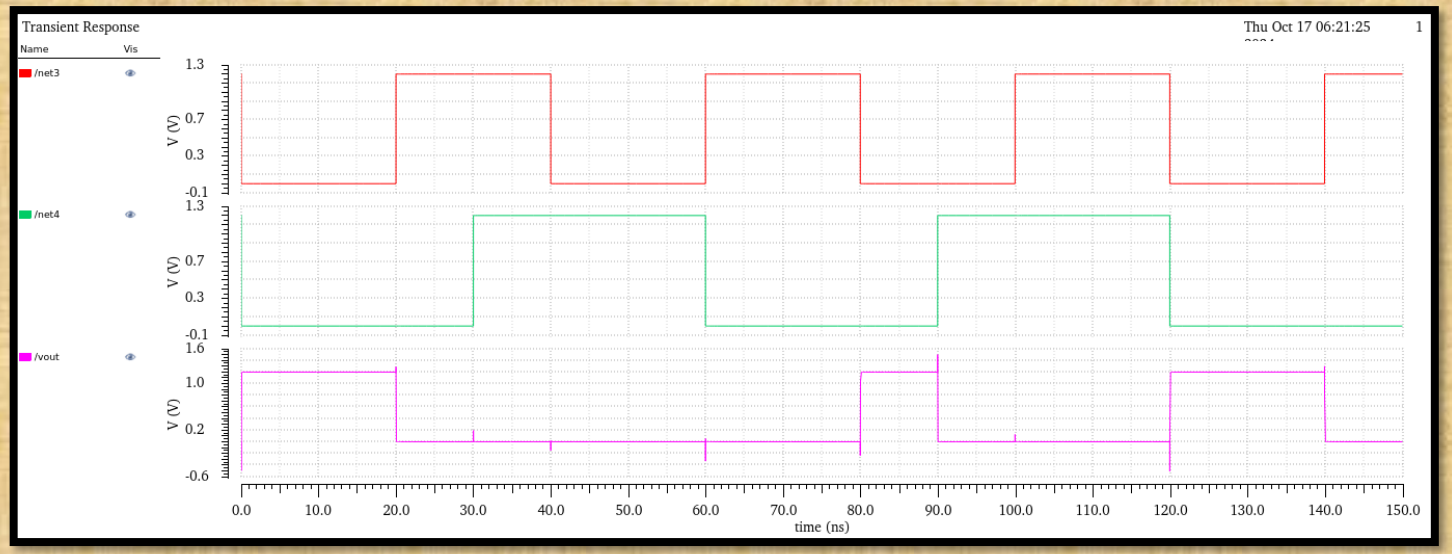


NOR GATE

2 PMOS in series & 2 NMOS in parallel connected together in series

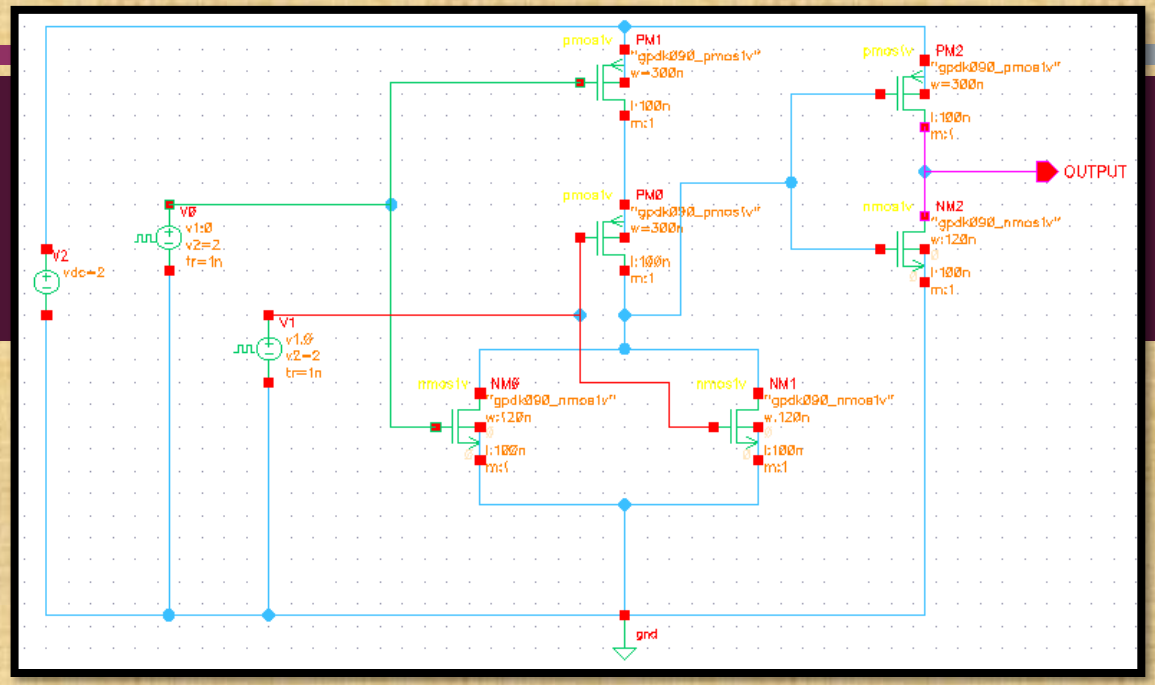
- NOR gate outputs low when either input is high.



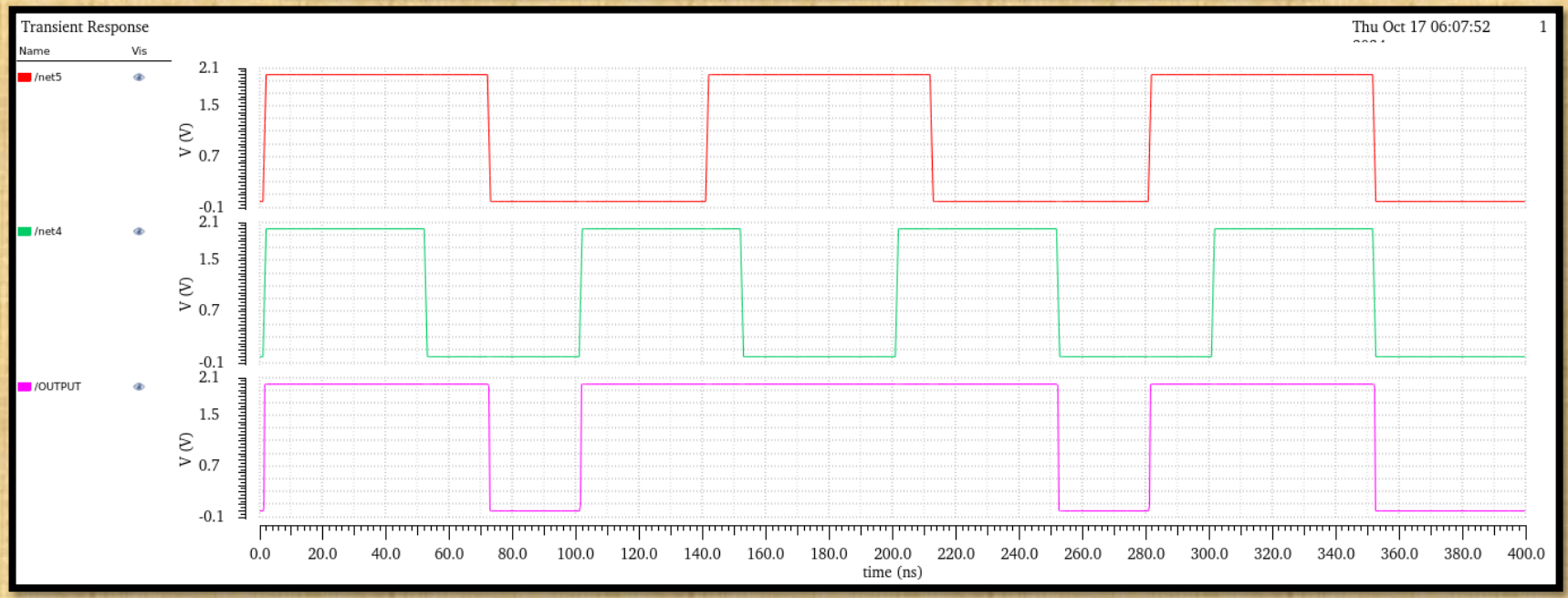


OR GATE

2 PMOS in series & 2 NMOS in parallel connected together in series & inverter connected before output.



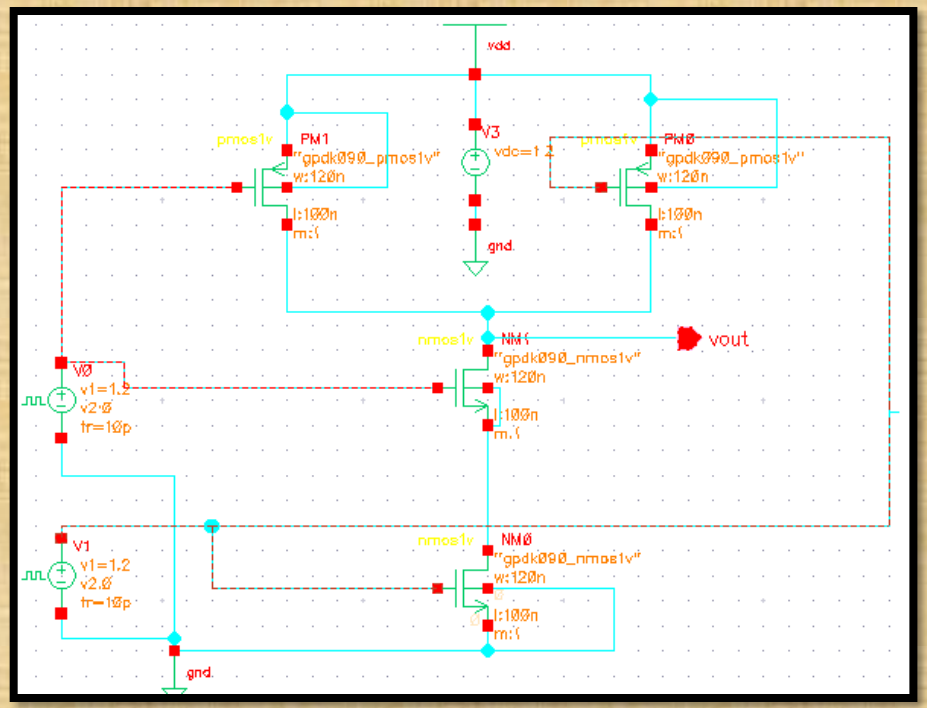
- OR gate output follows the logical OR behavior, outputting 1 when any input is 1.

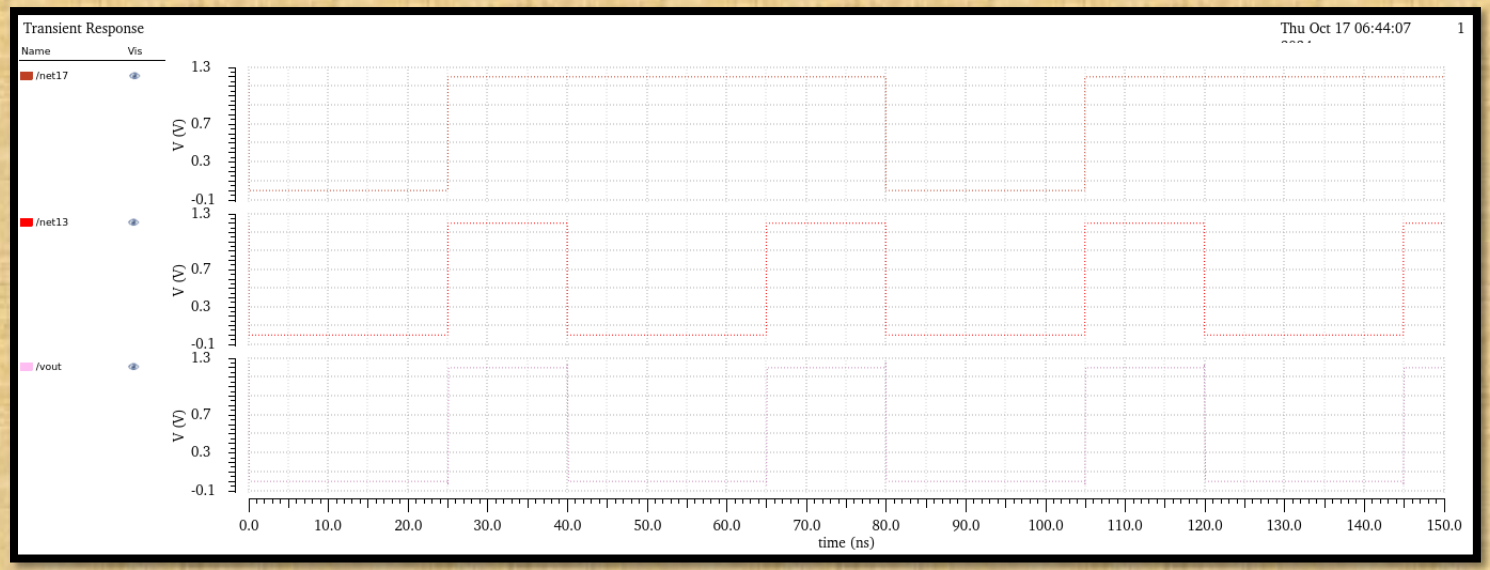


NAND GATE

2 PMOS in parallel & 2 NMOS in series connected together in series.

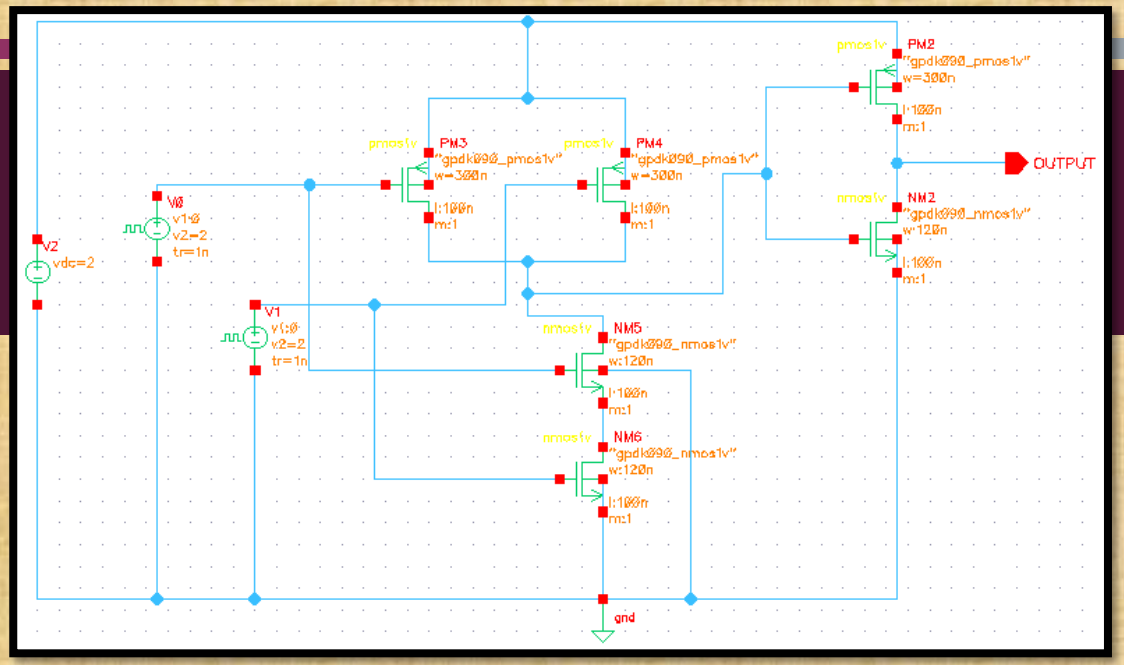
- NAND gate output is high except when both inputs are high.



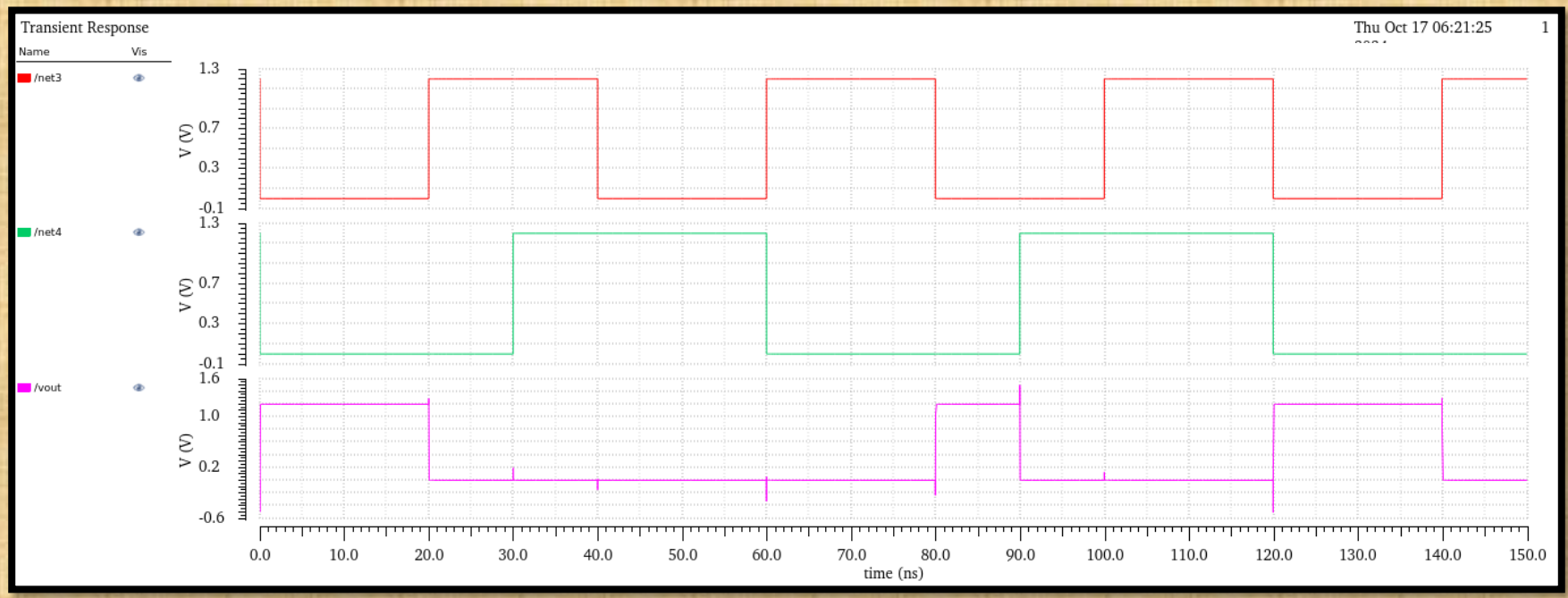


AND GATE

2 PMOS in parallel & 2 NMOS in series connected together in series & inverter connected before output



- AND gate outputs high only when both inputs are high.



CONCLUSION

- **Key Points:**
  - Successfully designed and simulated basic CMOS logic gates (Inverter, OR, NOR, AND, NAND) in Cadence Virtuoso.
  - The transient analysis graphs confirm the correct logical behavior of each gate.

- **Why CMOS is Efficient:**
  - CMOS consumes power only during switching, making it more power-efficient compared to other technologies.

- **Future Prospects:**
  - As technology scales down, challenges such as leakage current need to be addressed.
  - CMOS will continue to evolve with new designs like FinFETs for more power-efficient and faster circuits.

REFERENCES

- **CMOS VLSI Design: A Circuits and Systems Perspective** – Neil H. E. Weste and David Harris.
- **Digital Integrated Circuits: A Design Perspective** – Jan M. Rabaey.
- **Cadence Virtuoso Documentation** for design and simulation methodology.
- CMOS VLSI Design faculty guidance.

THANK YOU!!!