TOWER 0.18 micron, 1.8 Volt
Super Compact Core I/O Pad Library
TSL18CIO150

Version 1.0

October 2003

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Preface

This guide is intended for use with Production Release of IO Library (TSL18CIO150), for the Tower 0.18 micron CMOS process (for DR2 0018SL) technology and characterized with Tower 0.18 micron Spice Models revision "Tower’s spec DRS2 0018B Rev 2.4", "Tower’s spec DRS2 0018BA Rev 3.1" and "Tower’s spec DRS2 0018B5 Rev 3.1".

About This Guide

Overview of Contents

This manual contains the following chapters:

Chapter 1, Introduction

Gives a general description of the functions and characteristics of the Super Compact Core I/O Pad Library.

Chapter 2, Characteristics

Includes the detailed characteristics tables of all the Super Compact Core I/O Pad Library pads.

Chapter 3, Derating Information

Describes the derating factors you should use to estimate delays under different operating conditions.

Chapter 4, Pull-up and pull-down resistors

Describes the pull-up and pull-down resistors applied in the I/O Pads.

Associated Guides and Documentation

Other publications you can consult for related information are:

TSL18CIO150, 0.18 micron, 1.8 volt, Super Compact Core I/O Pad Library (this datasheet)

TSL18FS120, 0.18 micron, 1.8 volt, Fast Silicon SC Library

Conventions

The following syntax conventions are used in this guide:

bold text	Is used for emphasis.
italic text	Indicates new terms and references to other sources of information.
italic text in blue	Indicates cross references that are also hypertext links.
`courier text`	Indicates commands that you enter directly, system responses, and file examples.
`bold courier text`	Indicates user input in examples of terminal sessions.
Helvetica italic text	Is used in syntax descriptions to indicate arguments where you should substitute a real value

Chapter 1
Introduction

Introduction to the TSL18CIO150 Pad Library

This manual is addressed to the design engineer who is doing a preliminary feasibility evaluation and wishes to make comparisons among the design technologies available in the pad libraries. Additionally, you can use this library manual while designing a chip to see which cells are available and to check the power consumption, critical timing values, propagation delay equations, and functions of a cell.

Contents of This Manual

This introduction contains the following sections:

•The *General Information* section of this manual gives basic information about library performances, voltage levels, IO pitch, using power and ground pads.

•The *I/O Cell Library - Product Specification* section contain the recommended operating conditions and DC characteristics.

•The *Library Design Review* section contain specification review, i.e. it describes the resulting DC and AC parameters under different conditions.

•The *Cells* section describes the contents of the datasheets and how to interpret them, and explains how to decode the cells names.

•The *System Design Considerations* section looks at the types of power connections and addresses commonly asked user design questions.

Following this introduction are the data sheets for the TSL18CIO150 pads.

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1.0 General Information

1.1 Library Performances

The TSL18CIO150 library has been designed to be used at a frequency up to 130MHz, on a maximum external load capacitance of 40pF and for a pin package inductance up to 20nH.

1.2 Voltage Levels

The TSL18CIO150 library is made up exclusively of low voltage chip interface circuits powered by a voltage in the range of 1.65V to 1.95V. However, all cells are not 3.3 Volt tolerant, i.e. the corresponding pins can be connected to the buses which can only swing between 0V and 1.95V. The library is designed to be used with the TSL18OS120 1.8-volt Optimum Silicon SC and the TSL18FS120 1.8-volt Fast Silicon SC libraries.

1.3 IO pitch

These library uses a 3.15 mils pitch. The size of the IO is 65µm width and 162µm height without bonding pad. With bonding pad the height is 250µm. Using the bonding cell provided with this library the I/Os can be abutted. Customer bonding cell can be used for the I/O. The usable filler cells are provided in this library.

1.4 Power and Ground Pads

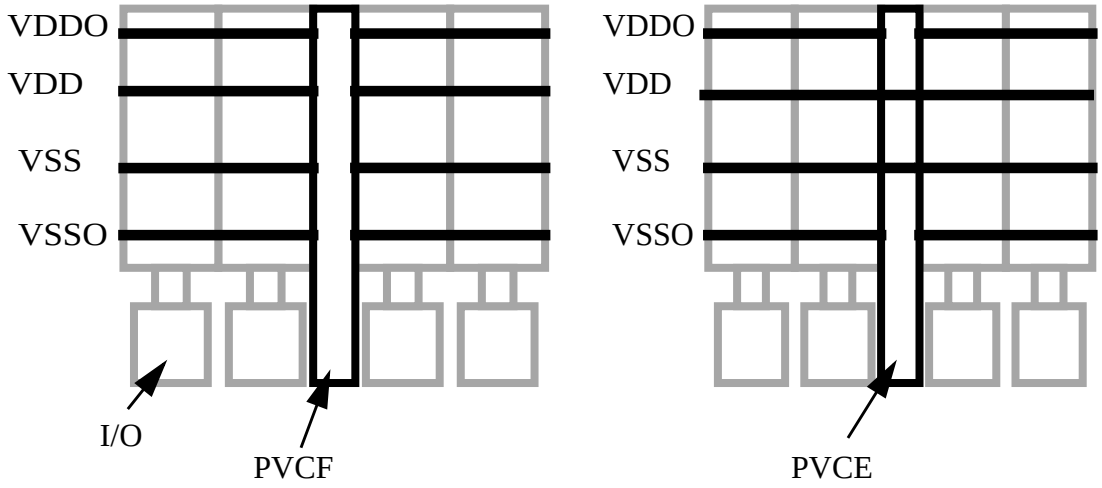
There are two kinds of power pairs for the TSL18CIO150 library. These are “I/O” and “Core” power pairs. I/O power is used by the I/O to switch its external output from one state to the other. And This switching generates noise in the I/O power buses on the chip. Core power is used by the core. Refer to the “*SSO Guidelines*” and “*I/O Usage Application note*” for more information on the types of power pairs and the numbers of each required.

1.5 New Features

This library introduces new power pads named PVDC/PV0C that supply only the core of the chip with separated VDD and VSS. These power pads can be used to supply a chip with multiple power voltage (*see* “*Multiple Power Flow*” *application note*). Furthermore to be able to have multipower supplies for the IO power ring, two pads are also provided to cut properly the ring. These pads are named PVCF and PVCE. The first one PVCF cuts all power rings. The second one PVCE cuts all power rings, except VDD and VSS rings.

These pads can be used in the same way as the corner pad. They do not have icons. They do not appear in the netlist. Their placement with Apollo can be defined with a tdf file.

The following schematic gives an example of the PVCF and PVCE cells usage:

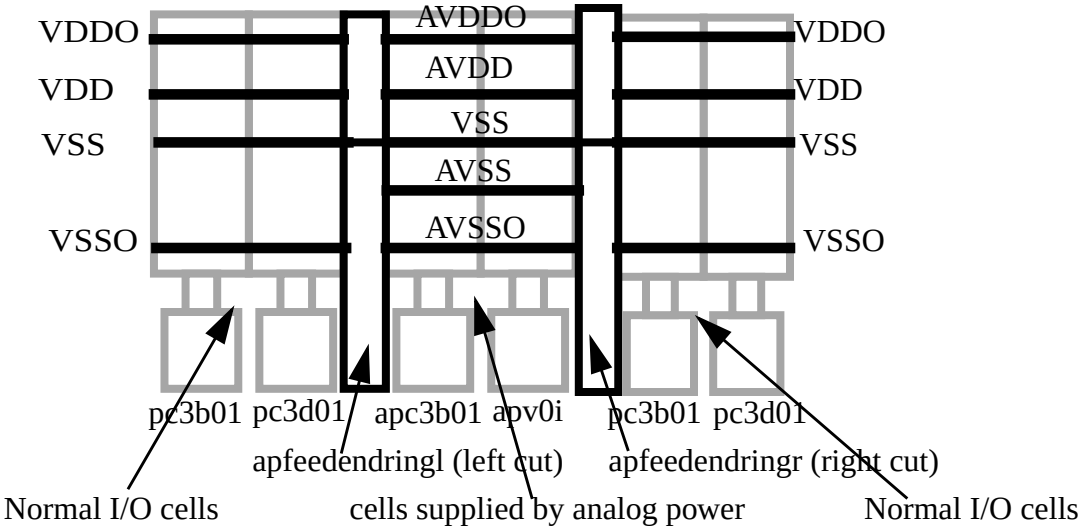


And because cells supplied by analog power are also provided in TSL18CIO150 library, two cut cells, apfeedendringl and apfeedendringr, are used to cut proper ring and seperate the cells supplied by analog power and other normal function cells. The first one apfeedendringl must be put at the left of the cells supplied by analog power.The second one apfeedendringr must be put at the right of the cells supplied by analog power. Both of these two cells cut all power rings except VSS ring.

Non-abutting the cut-cell at either side might introduce unwanted noise coupling between the normal I/O cells and cells supplied by analog power.

These two pads can be used in the same way as the corner pad. They do not have icons. They do not appear in the netlist. Their placement with Apollo can be defined with a tdf file.

The following schematic gives an example of the apfeedendringl and apfeeden-dringr cells usage :



2.0 I/O Cell Library - Product Specification

2.1 1.8V I/O Operation

TABLE 2.1. Recommended Operating Conditions

Parameter	Range
Storage Temperature	-40˚C to +125˚C
Core Supply Voltage (VDD)	-0.5V to +1.98V
I/O Supply Voltage (VDDO)	-0.5V to +1.95V

The following table is the DC characteristics for 1.8V operation:

TABLE 2.2. DC characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VDDO	Ring Power Supply	1.65	1.8	1.95	Volts	1.8V power supply
VIL	Input Low Voltage	-0.3		0.35*VDDO	Volts	
VIH	Input High Voltage	0.65*VDDO		VDDO+0.3V	Volts	
VOL	Output Low Voltage			0.45	Volts	VDDO = min, IOL =-2mA
VOH	Output High Voltage	VDDO-0.45			Volts	VDDO = min, IOH =+2mA
VT+	Schmitt Input High Voltage	0.65*VDDO		VDDO+0.3V	Volts	
VT-	Schmitt Input Low Voltage	-0.3		0.35*VDDO	Volts	
VTH	Input Hysteresis Voltage		0.25		Volts	
IILPU	Input Low Current For Pull-up Pins			+200	µA	VIL=VSS
IIHPU	Input High Current For Pull-up Pins	-1	0	+1	µA	VIH=VDDO
IILPD	Input Low Current For Pull-down Pins	-1	0	+1	µA	VIL=VSS
IIHPD	Input High Current For Pull-down Pins	-200			µA	VIH=VDDO
IIL	Input Low Current	-1	0	+1	µA	VIL=VSS
IIH	Input High Current	-1	0	+1	µA	VIH=VDDO
CIN	Input Pin Capacitance		5		pF	
COUT	Output Pin Capacitance		5		pF	
CIO	Bidirectional Pin Capacitances		5		pF	

2.2 I/O Performance Requirements

Highest drive variant of each I/O is able to drive 40pF at 130MHz.

3.0 Library Design Review

3.1 Specification Review

3.1.1 DC parameters:

3.1.1.1 Voh Parameter:

Voh parameter is simulated using Hspice by tieding up the input I of the I/O cell and connecting a current source between VSS and PAD, sourcing the specified current from the PAD pin.

Results under different conditions are reported in the following table:

TABLE 3.1. Voh for 1.8V Process Option

Cell Name	Specification		Worst Case	Typical Case	Best Case	Conditions
	Min	Typ	SS/1.65V/125degC	TT/1.8V/25degC	FF/1.95V/-40degC	
pc3b01	VDDO-0.45		1.2613	1.5929	1.8156	@Ioh = -2mA
pc3b02	VDDO-0.45		1.2613	1.5929	1.8156	@Ioh = -4mA
pc3b03	VDDO-0.45		1.2613	1.5929	1.8156	@Ioh = -6mA
pc3b04	VDDO-0.45		1.2613	1.5929	1.8156	@Ioh = -8mA
pc3b05	VDDO-0.45		1.2613	1.5929	1.8156	@Ioh = -10mA

3.1.1.2 Vol Parameter:

Vol parameter is simulated using Hspice by tieding down the input I of the I/O cell and connecting a current source between VDDO and PAD, sinking the specified current into the PAD pin.

Results under different conditions are reported in the following table:

TABLE 3.2. Vol for 1.8V Process Option

Cell Name	Specification		Worst Case	Typical Case	Best Case	Conditions
	Typ	Max	SS/1.65V/125degC	TT/1.8V/25degC	FF/1.95V/-40degC	
pc3b01		0.45	0.2566	0.1226	0.0773	@Iol = 2mA
pc3b02		0.45	0.2566	0.1226	0.0773	@Iol = 4mA
pc3b03		0.45	0.2566	0.1226	0.0773	@Iol = 6mA
pc3b04		0.45	0.2566	0.1226	0.0773	@Iol = 8mA
pc3b05		0.45	0.2566	0.1226	0.0773	@Iol = 10mA

3.1.1.3 Vil Parameter:

Vil parameter is characterized with Hspice by doing a quasi-static transient simulation. The input pin PAD is varying very slowly from VSS to VDDO and back to VSS in 2µS. Vil is obtained by measuring

the PAD voltage value which results in a CIN output level of 0.1xVDD. This is done for both rising and falling edge. As the circuit is the same for all bi-directional pads, what ever is the output drive capability, results are provided only for PC3B01 I/O.

Results under different conditions are reported in the following table which also includes the PAD voltage when CIN voltage is equal to VDD/2 (trip-point):

TABLE 3.3. Vil for 1.8V Process Option

Conditions (process/vdd/vddo/temp)	Specification		Input Rising		Input Falling	
	Min	Max	@CIN=0.1xVDD	@CIN=0.5xVDD	@CIN=0.1xVDD	@CIN=0.5xVDD
TT/1.8V/1.8V/25degC	-0.3	0.35*VDDO	0.8472	0.8523	0.8081	0.8116
TT/1.62V/1.65V/25degC	-0.3	0.35*VDDO	0.7966	0.8019	0.7462	0.7498
TT/1.98V/1.95V/25degC	-0.3	0.35*VDDO	0.8977	0.9031	0.8640	0.8675
SS/1.62V/1.65V/125degC	-0.3	0.35*VDDO	0.8307	0.8373	0.7510	0.7558
SS/1.8V/1.8V/125degC	-0.3	0.35*VDDO	0.8824	0.8887	0.8219	0.8266
SS/1.98V/1.95V/125degC	-0.3	0.35*VDDO	0.9362	0.9424	0.8848	0.8893
FF/1.98V/1.95V/-40degC	-0.3	0.35*VDDO	0.8596	0.8647	0.8370	0.8399
FF/1.8V/1.8V/-40degC	-0.3	0.35*VDDO	0.8117	0.8161	0.7864	0.7893
FF/1.62V/1.65V/-40degC	-0.3	0.35*VDDO	0.7636	0.7679	0.7336	0.7364
SF/1.62V/1.65V/25degC	-0.3	0.35*VDDO	0.8583	0.8637	0.8058	0.8094
SF/1.8V/1.8V/25degC	-0.3	0.35*VDDO	0.9108	.9157	0.8696	0.8730
SF/1.98V/1.95V/25degC	-0.3	0.35*VDDO	**0.9631**	**0.9682**	**0.9276**	**0.9310**
FS/1.98V/1.95V/25deg	-0.3	0.35*VDDO	0.8327	0.8379	0.7999	0.8034
FS/1.8V/1.8V/25degC	-0.3	0.35*VDDO	0.7838	0.7890	0.7459	0.7496
FS/1.62V/1.65V/25degC	-0.3	0.35*VDDO	**0.7345**	**0.7398**	**0.6864**	**0.6899**

Minimum values are obtained for FS/1.62V/1.65V/25degC.

Maximum values are obtained for SF/1.98V/1.95V/25degC.

3.1.1.4 Vih Parameter:

Vih parameter is characterized with Hspice by doing a quasi-static transient simulation. The input pin PAD is varying very slowly from VSS to VDDO and back to VSS in 2µS. Vih is obtained by measuring the PAD voltage value which results in a CIN output level of 0.9xVDD. This is done for both rising and falling edge. As the circuit is the same for all bi-directional pads, what ever is the output drive capability, results are provided only for PC3B01 I/O.

Results under different conditions are reported in the following table which also includes the PAD voltage when CIN voltage is equal to VDD/2 (trip-point):

TABLE 3.4. Vih for 1.8V Process Option

Conditions (process/vdd/vddo/temp)	Specification		Input Rising		Input Falling	
	Min	Max	@CIN=0.9xVDD	@CIN=0.5xVDD	@CIN=0.9xVDD	@CIN=0.5xVDD
TT/1.8V/1.8V/25degC	0.65*VDDO	VDDO+0.3	0.8559	0.8523	0.8167	0.8116
TT/1.62V/1.65V/25degC	0.65*VDDO	VDDO+0.3	0.8056	0.8019	0.7551	0.7498
TT/1.98V/1.95V/25degC	0.65*VDDO	VDDO+0.3	0.9065	0.9031	0.8732	0.8675
SS/1.62V/1.65V/125degC	0.65*VDDO	VDDO+0.3	0.8418	0.8373	0.7629	0.7558
SS/1.8V/1.8V/125degC	0.65*VDDO	VDDO+0.3	0.8934	0.8887	0.8334	0.8266
SS/1.98V/1.95V/125degC	0.65*VDDO	VDDO+0.3	0.9469	0.9424	0.8959	0.8893
FF/1.98V/1.95V/-40degC	0.65*VDDO	VDDO+0.3	0.8681	0.8647	0.8450	0.8399
FF/1.8V/1.8V/-40degC	0.65*VDDO	VDDO+0.3	0.8194	0.8161	0.7938	0.7893
FF/1.62V/1.65V/-40degC	0.65*VDDO	VDDO+0.3	0.7712	0.7679	0.7409	0.7364
SF/1.62V/1.65V/25degC	0.65*VDDO	VDDO+0.3	0.8674	0.8637	0.8147	0.8094
SF/1.8V/1.8V/25degC	0.65*VDDO	VDDO+0.3	0.9194	0.9157	0.8781	0.8730
SF/1.98V/1.95V/25degC	0.65*VDDO	VDDO+0.3	**0.9719**	**0.9682**	**0.9361**	**0.9310**
FS/1.98V/1.95V/25degC	0.65*VDDO	VDDO+0.3	0.8417	0.8379	0.8091	0.8034
FS/1.8V/1.8V/25degC	0.65*VDDO	VDDO+0.3	0.7925	0.7890	0.7553	0.7496
FS/1.62V/1.65V/25degC	0.65*VDDO	VDDO+0.3	**0.7438**	**0.7398**	**0.6957**	**0.6899**

Minimum values are obtained for FS/1.62V/1.65V/25degC.

Maximum values are obtained for SF/1.98V/1.95V/25degC.

3.1.1.5 Iil Parameter:

Iil parameter is characterized with Hspice by doing a DC simulation. The input pin PAD is set at VSS and the current through this voltage source is measured. Characterizations are done for the same operating conditions as Vil, however, only the minimum value and the maximum value over the various operating conditions are reported in the table below:

TABLE 3.5. Iil for 1.8V Process Option

Cell Name	Specification		DC Characterization	
	Min	Max	Min	Max
pc3b01	-1e-06	+1e-06	4.987e-11	4.510e-08
pc3b01d	-1e-06	+1e-06	4.981e-11	4.509e-08
pc3b01u		+200e-06	9.899e-06	2.868e-05
pc3b02	-1e-06	+1e-06	4.987e-11	4.510e-08
pc3b03	-1e-06	+1e-06	4.987e-11	4.510e-08
pc3b04	-1e-06	+1e-06	4.987e-11	4.510e-08
pc3b05	-1e-06	+1e-06	4.987e-11	4.510e-08
pc3d21	-1e-06	+1e-06	4.987e-11	4.510e-08
pc3d21u		+200e-06	9.899e-06	2.868e-05
pc3d21d	-1e-06	+1e-06	4.981e-11	4.509e-08
pc3d31	-1e-06	+1e-06	4.987e-11	4.510e-08
pc3d31u		+200e-06	9.899e-06	2.868e-05
pc3d31d	-1e-06	+1e-06	4.981e-11	4.509e-08

3.1.1.6 Iih Parameter:

Iih parameter is characterized with Hspice by doing a DC simulation. The input pin PAD is set at VDDO and the current through this voltage source is measured. Characterizations are done for the same operating conditions as Vih, however, only the minimum value and the maximum value over the various operating conditions are reported in the table below:

TABLE 3.6. Iih for 1.8V Process Option

Cell Name	Specification		DC Characterization	
	Min	Max	Min	Max
pc3b01	-1e-06	+1e-06	-5.204e-11	-3.762e-08
pc3b01d	-200e-06		-7.205e-06	-1.747e-05
pc3b01u	-1e-06	+1e-06	-5.189e-11	-3.761e-08

TABLE 3.6. Iih for 1.8V Process Option

Cell Name	Specification		DC Characterization	
	Min	Max	Min	Max
pc3b02	-1e-06	+1e-06	-5.204e-11	-3.762e-08
pc3b03	-1e-06	+1e-06	-5.204e-11	-3.762e-08
pc3b04	-1e-06	+1e-06	-5.204e-11	-3.762e-08
pc3b05	-1e-06	+1e-06	-5.204e-11	-3.762e-08
pc3d21	-1e-06	+1e-06	-5.204e-11	-3.762e-08
pc3d21u	-1e-06	+1e-06	-5.189e-11	-3.761e-08
pc3d21d	-200e-06		-7.205e-06	-1.747e-05
pc3d31	-1e-06	+1e-06	-5.204e-11	-3.762e-08
pc3d31u	-1e-06	+1e-06	-5.189e-11	-3.761e-08
pc3d31d	-200e-06		-7.205e-06	-1.747e-05

3.1.1.7 Iol Parameter:

Iol parameter is characterized with Hspice by doing a DC simulation. The output pin PAD is forced to Vol (0.45V) via a voltage source and the current through this voltage source is measured. Due to the hierarchical building block strategy, this parameter is only dependent on the I/O output drive strength and is the same across output families (bidir, tristate, simple output).

Results under different conditions are reported in the following table:

TABLE 3.7. Iol for 1.8V Process Option

Cell Name	Specification		Worst Case	Typical Case	Best Case	Conditions
	Min	Typ	SS/1.65V/125degC	TT/1.8V/25degC	FF/1.95V/-40degC	
pc3b01	2mA		2.970	5.782	9.254	@Vol = 0.45V
pc3b02	4mA		5.940	11.56	18.51	@Vol = 0.45V
pc3b03	6mA		8.910	17.34	27.76	@Vol = 0.45V
pc3b04	8mA		11.88	23.13	37.02	@Vol = 0.45V
pc3b05	10mA		14.85	28.91	46.27	@Vol = 0.45V

3.1.1.8 Ioh Parameter:

Ioh parameter is characterized with Hspice by doing a DC simulation. The output pin PAD is forced to Voh (VDDO-0.45) via a voltage source and the current through this voltage source is measured. Due to the hierarchical building block strategy, this parameter is only dependent on the I/O output drive strength and is the same across output families (bidir, tristate, simple output).

Results under different conditions are reported in the following table:

TABLE 3.8. Ioh for 1.8V Process Option

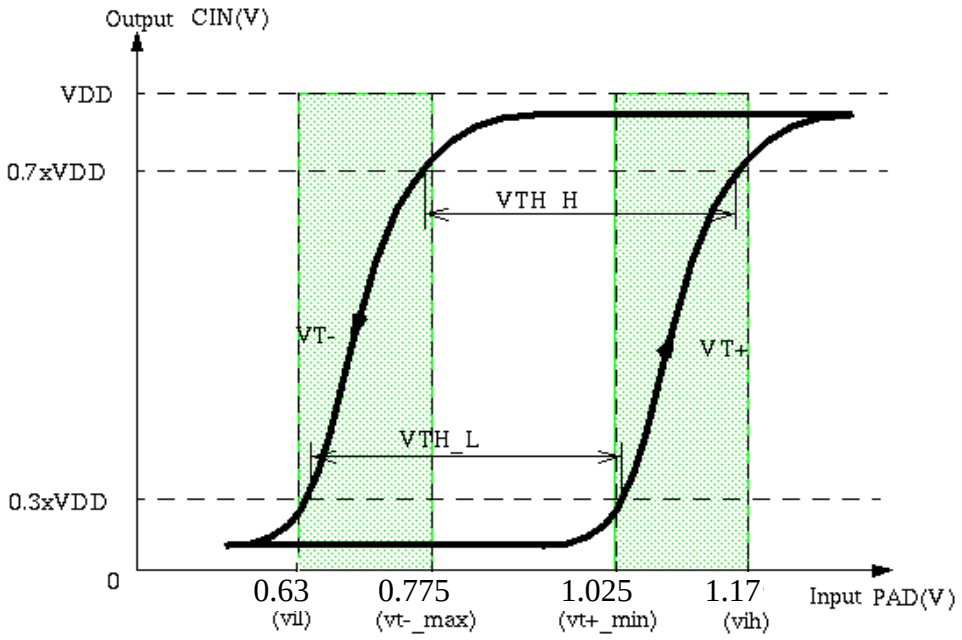
	Specification		Worst Case	Typical Case	Best Case	
Cell Name	Min)	Typ	SS/1.65V/125degC	TT/1.8V/25degC	FF/1.95V/-40degC	Conditions
pc3b01	2mA		-2.188	-3.647	-5.560	@Voh = VDDO-0.45V
pc3b02	4mA		-4.376	-7.294	-11.12	@Voh = VDDO-0.45V
pc3b03	6mA		-6.565	-10.94	-16.68	@Voh = VDDO-0.45V
pc3b04	8mA		-8.754	-14.59	-22.24	@Voh = VDDO-0.45V
pc3b05	10mA		-10.94	-18.24	-27.80	@Voh = VDDO-0.45V

3.1.1.9 Schmitt Trigger DC Parameters:

VT- and VT+ parameters are characterized with Hspice by doing a quasi-static transient simulation, like the Vil and Vih parameters. VT- and VT+ are obtained by measuring the PAD voltage value which results in a CIN output level of 0.3xVDD, 0.5xVDD and 0.7xVDD. This is done for both rising and falling edge. VTH is obtained by calculating the hysteresis value.This value is calculated by using the following equations:

$$VTH\_L = (VT+) - (VT-), \text{ for CIN} = 0.3xVDD$$

$$VTH\_H = (VT+) - (VT-), \text{ for CIN} = 0.7xVDD$$



The Schmitt Trigger Hysteresis

Results under different conditions are reported in the following tables (3.9 - 3.14):

TABLE 3.9. PC3D21 VT- for 1.8V Process Option

Conditions (process/vdd/vddo/temp)	Specification		Input Falling		
	Min	Max	@CIN=0.3xVDD	@CIN=0.5xVDD	@CIN=0.7xVDD
TT/1.8V/1.8V/25degC	0.63	0.775	0.5886	0.5888	0.5891
TT/1.62V/1.65V/25degC	0.63	0.775	0.5208	0.5211	0.5214
TT/1.98V/1.95V/25degC	0.63	0.775	0.6567	0.6569	0.6572
SS/1.62V/1.65V/125degC	0.63	0.775	0.5176	0.5181	0.5186
SS/1.8V/1.8V/125degC	0.63	0.775	0.5918	0.5922	0.5927
SS/1.98V/1.95V/125degC	0.63	0.775	0.6581	0.6585	0.6589
FF/1.98V/1.95V/-40degC	0.63	0.775	0.6612	0.6613	0.6615
FF/1.8V/1.8V/-40degC	0.63	0.775	0.6013	0.6014	0.6016
FF/1.62V/1.65V/-40degC	0.63	0.775	0.5318	0.5320	0.5322

TABLE 3.9. PC3D21 VT- for 1.8V Process Option

Conditions (process/vdd/vddo/temp)	Specification		Input Falling		
	Min	Max	@CIN=0.3xVDD	@CIN=0.5xVDD	@CIN=0.7xVDD
SF/1.62V/1.65V/25degC	0.63	0.775	0.5489	0.5492	0.5495
SF/1.8V/1.8V/25degC	0.63	0.775	0.6222	0.6225	0.6227
SF/1.98V/1.95V/25degC	0.63	0.775	**0.6933**	**0.6936**	**0.6938**
FS/1.98V/1.95V/25degC	0.63	0.775	0.6202	0.6204	0.6207
FS/1.8V/1.8V/25degC	0.63	0.775	0.5567	0.5570	0.5573
FS/1.62V/1.65V/25degC	0.63	0.775	**0.4866**	**0.4870**	**0.4873**

TABLE 3.10. PC3D21 VT+ for 1.8V Process Option

Conditions (process/vdd/vddo/temp)	Specification		Input Rising		
	Min	Max	@CIN=0.3xVDD	@CIN=0.5xVDD	@CIN=0.7xVDD
TT/1.8V/1.8V/25degC	1.025	1.17	1.0425	1.0427	1.0428
TT/1.62V/1.65V/25degC	1.025	1.17	0.9881	0.9883	0.9885
TT/1.98V/1.95V/25degC	1.025	1.17	1.0972	1.0974	1.0976
SS/1.62V/1.65V/125degC	1.025	1.17	1.0174	1.0178	1.0181
SS/1.8V/1.8V/125degC	1.025	1.17	1.0739	1.0742	1.0745
SS/1.98V/1.95V/125degC	1.025	1.17	1.1322	1.1324	1.1327
FF/1.98V/1.95V/-40degC	1.025	1.17	1.0475	1.0476	1.0477
FF/1.8V/1.8V/-40degC	1.025	1.17	0.9984	0.9985	0.9986
FF/1.62V/1.65V/-40degC	1.025	1.17	0.9463	0.9465	0.9466
SF/1.62V/1.65V/25degC	1.025	1.17	1.0337	1.0339	1.0341
SF/1.8V/1.8V/25degC	1.025	1.17	1.0898	1.0900	1.0901
SF/1.98V/1.95V/25degC	1.025	1.17	**1.1460**	**1.1462**	**1.1463**
FS/1.98V/1.95V/25degC	1.025	1.17	1.0463	1.0465	1.0466
FS/1.8V/1.8V/25degC	1.025	1.17	0.9937	0.9939	0.9940

TABLE 3.10. PC3D21 VT+ for 1.8V Process Option

Conditions (process/vdd/vddo/temp)	Specification		Input Rising		
	Min	Max	@CIN=0.3xVDD	@CIN=0.5xVDD	@CIN=0.7xVDD
FS/1.62V/1.65V/25degC	1.025	1.17	**0.9401**	**0.9403**	**0.9404**

Minimum values the VT+ and VT- are obtained for FS/1.62V/1.65V/25degC.

Maximum values the VT+ and VT- are obtained for SF/1.98V/1.95V/25degC.

TABLE 3.11. PC3D21 VTH for 1.8V Process Option

Conditions (process/vdd/vddo/temp)	Specification			VTH_L	VTH_H
	Min	Typ	Max		
TT/1.8V/1.8V/25degC		0.25		0.4539	0.4537
TT/1.62V/1.65V/25degC		0.25		0.4673	0.4671
TT/1.98V/1.95V/25degC		0.25		0.4405	0.4403
SS/1.62V/1.65V/125degC		0.25		**0.4997**	**0.4995**
SS/1.8V/1.8V/125degC		0.25		0.4821	0.4819
SS/1.98V/1.95V/125degC		0.25		0.4740	0.4738
FF/1.98V/1.95V/-40degC		0.25		**0.3863**	**0.3862**
FF/1.8V/1.8V/-40degC		0.25		0.3972	0.3970
FF/1.62V/1.65V/-40degC		0.25		0.4146	0.4144
SF/1.62V/1.65V/25degC		0.25		0.4848	0.4847
SF/1.8V/1.8V/25degC		0.25		0.4675	0.4674
SF/1.98V/1.95V/25degC		0.25		0.4526	0.4525
FS/1.98V/1.95V/25degC		0.25		0.4261	0.4259
FS/1.8V/1.8V/25degC		0.25		0.4370	0.4368
FS/1.62V/1.65V/25degC		0.25		0.4534	0.4531

Minimum values the VTH are obtained for FF/1.98V/1.95V/-40degC.

Maximum values the VTH are obtained for SS/1.62V/1.65V/125degC.

TABLE 3.12. PC3D31 VT- for 1.8V Process Option

Conditions (process/vdd/vddo/temp)	Specification		Input Falling		
	Min	Max	@CIN=0.3xVDD	@CIN=0.5xVDD	@CIN=0.7xVDD
TT/1.8V/1.8V/25degC	0.63	0.775	0.5877	0.5877	0.5876
TT/1.62V/1.65V/25degC	0.63	0.775	0.5168	0.5167	0.5167
TT/1.98V/1.95V/25degC	0.63	0.775	0.6554	0.6554	0.6553
SS/1.62V/1.65V/125degC	0.63	0.775	0.5173	0.5171	0.5170
SS/1.8V/1.8V/125degC	0.63	0.775	0.5872	0.5871	0.5870
SS/1.98V/1.95V/125degC	0.63	0.775	0.6551	0.6550	0.6549
FF/1.98V/1.95V/-40degC	0.63	0.775	0.6631	0.6630	0.6630
FF/1.8V/1.8V/-40degC	0.63	0.775	0.5990	0.5990	0.5989
FF/1.62V/1.65V/-40degC	0.63	0.775	0.5316	0.5315	0.5315
SF/1.62V/1.65V/25degC	0.63	0.775	0.5446	0.5445	0.5445
SF/1.8V/1.8V/25degC	0.63	0.775	0.6196	0.6196	0.6195
SF/1.98V/1.95V/25degC	0.63	0.775	**0.6916**	**0.6915**	**0.6915**
FS/1.98V/1.95V/25degC	0.63	0.775	0.6196	0.6196	0.6195
FS/1.8V/1.8V/25degC	0.63	0.775	0.5560	0.5559	0.5559
FS/1.62V/1.65V/25degC	0.63	0.775	**0.4877**	**0.4876**	**0.4875**

TABLE 3.13. PC3D31 VT+ for 1.8V Process Option

Conditions (process/vdd/vddo/temp)	Specification		Input Rising		
	Min	Max	@CIN=0.3xVDD	@CIN=0.5xVDD	@CIN=0.7xVDD
TT/1.8V/1.8V/25degC	1.025	1.17	1.0440	1.0440	1.0439
TT/1.62V/1.65V/25degC	1.025	1.17	0.9911	0.9910	0.9909
TT/1.98V/1.95V/25degC	1.025	1.17	1.0997	1.0996	1.0995
SS/1.62V/1.65V/125degC	1.025	1.17	1.0242	1.0240	1.0239

TABLE 3.13. PC3D31 VT+ for 1.8V Process Option

Conditions (process/vdd/vddo/temp)	Specification		Input Rising		
	Min	Max	@CIN=0.3xVDD	@CIN=0.5xVDD	@CIN=0.7xVDD
SS/1.8V/1.8V/125degC	1.025	1.17	1.0792	1.0790	1.0789
SS/1.98V/1.95V/125degC	1.025	1.17	1.1359	1.1358	1.1356
FF/1.98V/1.95V/-40degC	1.025	1.17	1.0496	1.0496	1.0495
FF/1.8V/1.8V/-40degC	1.025	1.17	0.9996	0.9996	0.9995
FF/1.62V/1.65V/-40degC	1.025	1.17	0.9496	0.9496	0.9495
SF/1.62V/1.65V/25degC	1.025	1.17	1.0367	1.0366	1.0365
SF/1.8V/1.8V/25degC	1.025	1.17	1.0931	1.0930	1.0929
SF/1.98V/1.95V/25degC	1.025	1.17	**1.1493**	**1.1493**	**1.1492**
FS/1.98V/1.95V/25degC	1.025	1.17	1.0499	1.0499	1.0498
FS/1.8V/1.8V/25degC	1.025	1.17	0.9958	0.9957	0.9957
FS/1.62V/1.65V/25degC	1.025	1.17	**0.9431**	**0.9430**	**0.9429**

Minimum values the VT+ and VT- are obtained for FS/1.62V/1.65V/25degC.

Maximum values the VT+ and VT- are obtained for SF/1.98V/1.95V/25degC.

TABLE 3.14. PC3D31 VTH for 1.8V Process Option

Conditions (process/vdd/vddo/temp)	Specification			VTH_L	VTH_H
	Min	Typ	Max		
TT/1.8V/1.8V/25degC		0.25		0.4563	0.4563
TT/1.62V/1.65V/25degC		0.25		0.4743	0.4743
TT/1.98V/1.95V/25degC		0.25		0.4443	0.4442
SS/1.62V/1.65V/125degC		0.25		**0.5069**	**0.5069**
SS/1.8V/1.8V/125degC		0.25		0.4920	0.4919
SS/1.98V/1.95V/125degC		0.25		0.4808	0.4808
FF/1.98V/1.95V/-40degC		0.25		**0.3866**	**0.3865**

TABLE 3.14. PC3D31 VTH for 1.8V Process Option

Conditions (process/vdd/vddo/temp)	Specification			VTH_L	VTH_H
	Min	Typ	Max		
FF/1.8V/1.8V/-40degC		0.25		0.4006	0.4006
FF/1.62V/1.65V/-40degC		0.25		0.4181	0.4180
SF/1.62V/1.65V/25degC		0.25		0.4921	0.4920
SF/1.8V/1.8V/25degC		0.25		0.4735	0.4734
SF/1.98V/1.95V/25degC		0.25		0.4577	0.4577
FS/1.98V/1.95V/25degC		0.25		0.4303	0.4303
FS/1.8V/1.8V/25degC		0.25		0.4398	0.4398
FS/1.62V/1.65V/25degC		0.25		0.4554	0.4554

Minimum values the VTH are obtained for FF/1.98V/1.95V/-40degC.

Maximum values the VTH are obtained for SS/1.62V/1.65V/125degC.

3.1.2 AC parameters:

3.1.2.1 Worst Case/Best Case Conditions for I->PAD Delay:

After proper sizing of level shifter, worst/best case timings are in-line with standard worst/best case conditions. The following table shows the I->PAD delay for PC3B01 under different input ramp and output load conditions for regular worst case conditions (Process = SS, temperature = 125degC, VDD=1.62V) with VDDO=1.65V and VDDO=1.95V

The following table shows the delay obtained for PC3B01 for various characterization conditions:

TABLE 3.15. Worst Case Characterization Delay for 1.8V Process Option

IR (S)	CLOAD (F)	I->PAD rising @VDDO=1.65V (S)	I->PAD rising @VDDO=1.95V (S)
2.000e-11	4.000e-13	3.801e-09	2.809e-09
2.400e-10	4.000e-13	3.855e-09	2.869e-09
6.000e-10	4.000e-13	3.935e-09	2.963e-09
1.200e-09	4.000e-13	4.055e-09	3.105e-09
3.000e-09	4.000e-13	4.372e-09	3.482e-09
2.000e-11	1.600e-12	4.165e-09	3.083e-09

TABLE 3.15. Worst Case Characterization Delay for 1.8V Process Option

IR (S)	CLOAD (F)	I->PAD rising @VDDO=1.65V (S)	I->PAD rising @VDDO=1.95V (S)
2.400e-10	1.600e-12	4.220e-09	3.143e-09
6.000e-10	1.600e-12	4.300e-09	3.237e-09
1.200e-09	1.600e-12	4.419e-09	3.379e-09
3.000e-09	1.600e-12	4.736e-09	3.756e-09
2.000e-11	8.000e-12	6.065e-09	4.515e-09
2.400e-10	8.000e-12	6.119e-09	4.575e-09
6.000e-10	8.000e-12	6.200e-09	4.669e-09
1.200e-09	8.000e-12	6.321e-09	4.811e-09
3.000e-09	8.000e-12	6.641e-09	5.188e-09

3.1.2.2 Duty Cycle Simulation Results for I->PAD delay:

The following table shows the rising and falling delays and output transition as well as the duty cycle obtained for PC3B05 for various characterization conditions:

TABLE 3.16. Worst Case Characterization Delay and Duty Cycle for 1.8V Process Option

IR	CLOAD	Delay Rising	Transition Rising	Delay Falling	Transition Falling	Duty Cycle Distortion (%)
2.000e-11	4.000e-13	3.913e-09	3.996e-10	2.772e-09	5.842e-10	-5.71
2.400e-10	4.000e-13	3.968e-09	3.994e-10	2.816e-09	5.840e-10	5.76
6.000e-10	4.000e-13	4.049e-09	3.996e-10	2.869e-09	5.837e-10	-5.90
1.200e-09	4.000e-13	4.166e-09	3.999e-10	2.919e-09	5.839e-10	-6.23
3.000e-09	4.000e-13	4.481e-09	3.991e-10	3.028e-09	5.842e-10	-7.26
2.000e-11	1.600e-12	4.040e-09	4.623e-10	2.969e-09	6.955e-10	-5.36
2.400e-10	1.600e-12	4.096e-09	4.622e-10	3.013e-09	6.951e-10	-5.42
6.000e-10	1.600e-12	4.176e-09	4.623e-10	3.066e-09	6.950e-10	-5.55
1.200e-09	1.600e-12	4.294e-09	4.623e-10	3.117e-09	6.951e-10	-5.89
3.000e-09	1.600e-12	4.609e-09	4.615e-10	3.225e-09	6.955e-10	-6.92
2.000e-11	8.000e-12	4.578e-09	7.645e-10	3.784e-09	1.034e-09	-3.97
2.400e-10	8.000e-12	4.633e-09	7.646e-10	3.827e-09	1.033e-09	-4.03

TABLE 3.16. Worst Case Characterization Delay and Duty Cycle for 1.8V Process Option

IR	CLOAD	Delay Rising	Transition Rising	Delay Falling	Transition Falling	Duty Cycle Distortion (%)
6.000e-10	8.000e-12	4.713e-09	7.645e-10	3.879e-09	1.031e-09	-4.17
1.200e-09	8.000e-12	4.831e-09	7.644e-10	3.930e-09	1.031e-09	-4.51
3.000e-09	8.000e-12	5.146e-09	7.639e-10	4.039e-09	1.031e-09	-5.54
2.000e-11	3.000e-11	6.011e-09	1.796e-09	5.340e-09	1.904e-09	-3.36
2.400e-10	3.000e-11	6.067e-09	1.796e-09	5.381e-09	1.903e-09	-3.43
6.000e-10	3.000e-11	6.148e-09	1.796e-09	5.429e-09	1.903e-09	-3.59
1.200e-09	3.000e-11	6.267e-09	1.796e-09	5.477e-09	1.904e-09	-3.95
3.000e-09	3.000e-11	6.584e-09	1.796e-09	5.573e-09	1.905e-09	-5.06
2.000e-11	5.000e-11	7.095e-09	2.779e-09	5.958e-09	2.853e-09	-5.68
2.400e-10	5.000e-11	7.153e-09	2.779e-09	5.994e-09	2.854e-09	-5.79
6.000e-10	5.000e-11	7.238e-09	2.779e-09	6.033e-09	2.855e-09	-6.03
1.200e-09	5.000e-11	7.368e-09	2.779e-09	6.056e-09	2.861e-09	-6.56
3.000e-09	5.000e-11	7.709e-09	2.778e-09	6.072e-09	2.882e-09	-8.18

3.2 Timing Measurement Conditions

Unless otherwise specified the values used in this data sheet are:

VDDO = 1.8V
VDD = 1.8V
Junction Temperature = 25 degreesC
Process = Typical

Low voltage input signal rising and falling edge switching time up to 3ns (core side) and up to 10ns (pad side).

3.3 Characterization Informations

The TSL18CIO150 library has been characterized using the following corner conditions:

	Core voltage (volts)	I/O voltage (Volts)	Temp (^{o}C)	Process
Max	1.62	1.65	125	ss (slow-slow)
Typ	1.8	1.8	25	tt (typical)

	Core voltage (volts)	I/O voltage (Volts)	Temp (^oC)	Process
Min	1.98	1.95	-40	ff (fast-fast)

3.4 Slope and Load variations - Look Up table

The characterization has been done using the following input slope and output load variations. Input slopes and output loads have the same values for all drives.

The Synopsys lookj-up table models 5x5 are derived from this characterization.

The thresholds for outputs transitions are measured from 30% to 70% and extrapolated to 0-100%

	Input slope variations				
core input slope variations (ns)	0.02 (1)	0.24	0.6	1.2	3 (2)
pad input slope variations (ns)	0.07	0.8	2	4	10(3)

	Output load variations				
core output load variations (pF)	0.004(4)	0.016	0.08	0.4	0.8
pad output load variations (pF)	0.4	1.6	8	40	80(5)

Note:
(1): this value match the minimum core input slope variation of the standard cell library.
(2): this value match the maximum core input slope variation of the standard cell library.
(3): this high value for pad input slope variation allow high simulation range without delay extrapolation.
(4): this value is recommended first index of Look Up table.
(5): this high value for pad output load allow high simulation range without delay extrapolation. This value does not specify the maximum load usable at the nominal frequency usage.

3.5 Propagation Delay Time

•For CMOS I/Os in output mode, the delay is measured from the 50% point of the input to the 50% point of the output.

•When CMOS I/Os are in input mode, the delay is measured from the 50% point of the input to the 50% point of the output.

•For TTL I/Os in output mode, the delay is measured from the 50% point of the input to the 50% point of the output.

•When TTL I/Os are in input mode, the delay is measured from the 50% point of the input to the 50% point of the output.

3.6 Bond-pad metal layer implementation

This library is based on a generic design of the bonding pad. After layer processing performed by the electronic Design Transfer Package (DTP), the resulting bond pad satisfies the foundry rules.

The Passport DRC and LVS are processed using an identical layer processing. It allows to check the design using the foundry rules.

3.7 Oscillator pad Characteristics.

The oscillator pads have been designed to insure a small startup oscillation time and to reduce the jitter effect.

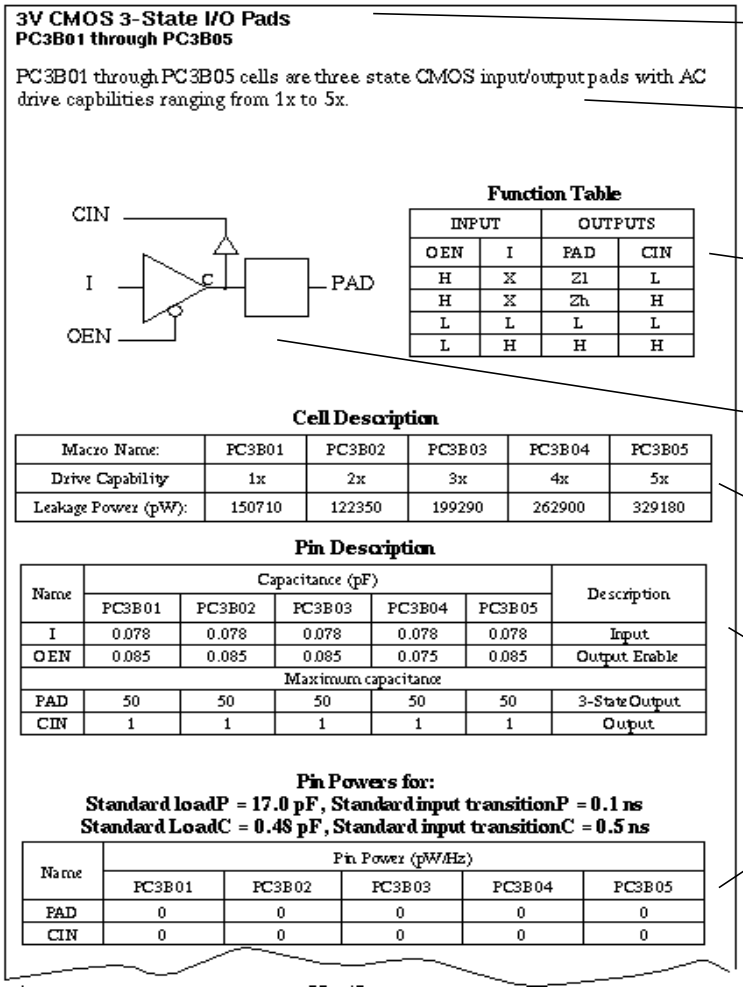
This pad can be used as amplifier in a pierce oscillator type. For more information on the basics of amplifier design, please refer to any electronic textbook.

The AC gain of the three provided pads amplifier is constant, but their respective drive allow different frequency usage. The PC3X13 that allows higher frequency usage than the PC3X12 and PC3X11. The designer must take in account the noise produced by the switching of the clock pad, in this way the three oscillator pads provides different rising and falling ramps. The PC3X11 provide the larger timing ramp delay. The PC3X13 provide the smaller timing ramp delay. The di/dt can be then controlled by the designer to insure lower noise on VDD and VSS power rings.

4.0 Cells

4.1 Reading the Datasheet

The first sheet of a standard datasheet contains the following elements:



3V CMOS 3-State I/O Pads
PC3B01 through PC3B05

PC3B01 through PC3B05 cells are three state CMOS input/output pads with AC drive capbilities ranging from 1x to 5x.

Function Table

INPUT		OUTPUTS	
OEN	I	PAD	CIN
H	X	Zl	L
H	X	Zh	H
L	L	L	L
L	H	H	H

Cell Description

Macro Name:	PC3B01	PC3B02	PC3B03	PC3B04	PC3B05
Drive Capability	1x	2x	3x	4x	5x
Leakage Power (pW):	150710	122350	199290	262900	329180

Pin Description

Name	Capacitance (pF)					Description
	PC3B01	PC3B02	PC3B03	PC3B04	PC3B05	
I	0.078	0.078	0.078	0.078	0.078	Input
OEN	0.085	0.085	0.085	0.075	0.085	Output Enable
Maximum capacitance						
PAD	50	50	50	50	50	3-State Output
CIN	1	1	1	1	1	Output

Pin Powers for:
Standard loadP = 17.0 pF, Standard input transitionP = 0.1 ns
Standard LoadC = 0.48 pF, Standard input transitionC = 0.5 ns

Name	Pin Power (pW/Hz)				
	PC3B01	PC3B02	PC3B03	PC3B04	PC3B05
PAD	0	0	0	0	0
CIN	0	0	0	0	0

These elements are described in the sections that follow.

Header and Description

The cell header in the large font describes the cell type, such as 1.8V CMOS 3-State I/O Pads. Under the header is a list of the cells included in the category in a

smaller font. The text block following the headers gives a brief description of the cells included in this data sheet.

Function Table:

L = LOW level		X = Any level (Don't care)	
L_r = Resistive LOW		Z = 3-state output	
H = HIGH level		Z_l = 3-state output, driven LOW from external source	
H_r = Resistive HIGH		Z_h = 3-state output, driven HIGH from external source	

Cell Information Table

The cell information is listed under the icon and function table for the cell; not all categories will be included for all cell types and libraries:

- Drive Capability
  - AC Drive – The transient output response of a circuit when the input is switched. The value describes both the time delay and the output load drive capability. For example, a circuit with an AC drive capability value of 4 normally has a shorter time delay and can drive larger capacitive loads than a circuit with an AC drive capability value of 3. The AC drive capability value is only a factor and should not be interpreted as an analog AC performance value.

Pin Description Table

The pin description table gives:

- The name of the pin
- The total capacitance that a signal driving in to that pin will have to drive; this includes gate capacitance as well as interconnect capacitance within the cell. For outputs, only the maximum capacitance used in the characterization is specified.
- A description of the pin's usage

Pin Power Table

The pin power table gives for each pin of the table a dissipated power from the Synopsys look-up table models.

This power is given for a standard load and a standard input transition.

The power data provided are the internal power for input pins when outputs doesn't switch, and the internal power for output pins.

The power data for output pins (*internalpower_out)* is according to synopsys power model:

$$internalpower\_out = totalswitchingpower - C \times (Vdd^2) / 2 - inputpower$$

In this equation, the *inputpower* is the internal power of the relative input that creates the switching of the output.

Due to the fact that C includes both the output pin load and the external load, the output pin internal power may be negative for some cells; this is effect of model.

The complete switching power when pin I makes the pin OUT switching is:

$$totalswitchingpower = internalpower(OUT) + C(OUT) \times (Vdd^2)/2 + inputpower($$

The internal power has been simulated for all outputs.

The internal power for the input pins of cells for which the input switching always creates an output switching (i.e. buffer) is not simulated. Therefore only the internal power of output pin for this type of cells appears in the datasheet and includes the internal power of the input pin.

In this case, the complete switching power when the input pin makes the output pin switching is:

$$totalswitchingpower = internalpower + C(OUT) \times (Vdd^2)/2$$

Note1: Leakage power of pull-up I/O includes the power dissipated through the pull-up resistor when PAD is set at Vil.

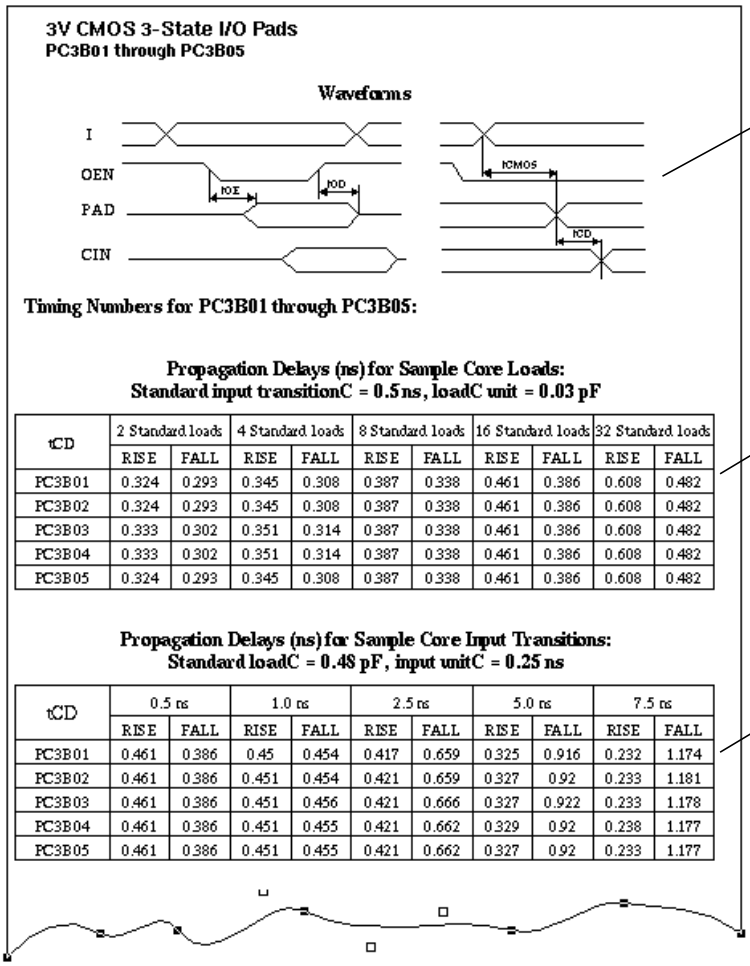
Unit of this value is "µW" for the following cells:

pc3t*u, pc3b*u, pt3t*u, pt3b*u and pc3d*u.

When PAD is set at Vih, Leakage power of pull-up I/O pc3t01u, pc3t02u,... pc3b01u,... are equal to the Leakage power of I/O pc3t01, pc3t02,... pc3b01,... correspondingly.

Note2: Pin Powers for output pins gives for RISE transition (rise_power) in this datasheet.

The second page of a standard datasheet contains the following information:



3V CMOS 3-State I/O Pads
PC3B01 through PC3B05

Waveforms

Timing Waveforms

Timing Numbers for PC3B01 through PC3B05:

Propagation Delays (ns) for Sample Core Loads:
Standard input transitionC = 0.5 ns, loadC unit = 0.03 pF

tCD	2 Standard loads		4 Standard loads		8 Standard loads		16 Standard loads		32 Standard loads	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B01	0.324	0.293	0.345	0.308	0.387	0.338	0.461	0.386	0.608	0.482
PC3B02	0.324	0.293	0.345	0.308	0.387	0.338	0.461	0.386	0.608	0.482
PC3B03	0.333	0.302	0.351	0.314	0.387	0.338	0.461	0.386	0.608	0.482
PC3B04	0.333	0.302	0.351	0.314	0.387	0.338	0.461	0.386	0.608	0.482
PC3B05	0.324	0.293	0.345	0.308	0.387	0.338	0.461	0.386	0.608	0.482

Propagation Delays for Sample Loads

Propagation Delays (ns) for Sample Core Input Transitions:
Standard loadC = 0.48 pF, input unitC = 0.25 ns

tCD	0.5 ns		1.0 ns		2.5 ns		5.0 ns		7.5 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B01	0.461	0.386	0.45	0.454	0.417	0.659	0.325	0.916	0.232	1.174
PC3B02	0.461	0.386	0.451	0.454	0.421	0.659	0.327	0.92	0.233	1.181
PC3B03	0.461	0.386	0.451	0.456	0.421	0.666	0.327	0.922	0.233	1.178
PC3B04	0.461	0.386	0.451	0.455	0.421	0.662	0.329	0.92	0.238	1.177
PC3B05	0.461	0.386	0.451	0.455	0.421	0.662	0.327	0.92	0.233	1.177

Propagation Delays for Sample Input Transitions

Waveforms

The waveforms graphically illustrate the critical timings in the Propagation Delays table.

Propagation Delays for Sample Loads and Input Transitions

The propagation delays for sample loads table uses look up table models. The delays for the chosen samples are interpolated using the 5x5 table points.

For I/Os in the input mode the propagation delay is given for sample core load (Core Load Fanout multiple at the Core Load Unit) and standard pad input transition in ns.

For I/Os in the output mode the propagation delay is given for sample pad load in pF and standard core input transition in ns.

The RISE and FALL times represent the total delay time from the change of the input pin to the corresponding response on the output pin. Actual interconnect length and load cannot be determined until a design has completed placement and routing. When using these tables, you must estimate the interconnect load in units of standard loads and add that to the fanout. A rough rule of thumb is that, for every input load, there is a corresponding interconnect load approximately equal to it. For example, to estimate the delay of a PC3B01 pad driving a fanout of 2, use the column in the data sheet specifying 4 standard loads: 2 for fanout and 2 for the interconnect loading.

4.2 Decoding the Cell Name

This section describes the naming conventions for the pad library cells. Each cell name begins with a two-letter code that tells what type of cell it is. This section gives the detailed naming convention for pads.

Cells supplied by analog power start from ‘0’ and other cells start from ‘1’.

I/O Naming Conventions:

(**0)1234567**

0 = A = cell supplied by analog power; not a variable (for I/O)

1 = P = Pad; not a variable (for I/O)

2 = The Input and/or Output level (standard) used for characterization:

C = CMOS

T = TTL

V = POWER (see POWER PADS NAMING CONVENTION below)

3 = Output signal level:

3 = mixed power voltage I/O library (VDDO=1.8V)

4 = Pad Function:

B = Bidirectional

T = Three-State Output

O= Output only

D = Input

C = Clock Input

X = Crystal Oscillator

5 = Pad-function-related options:

0 = Non-Inverting

1 = Inverting

2 = Schmitt Non-Inverting

3 = Schmitt Inverting

6 = Capability:

1 = 1X Drive

2 = 2X Drive

3 = 3X Drive

4 = 4X Drive

5 = 5X Drive

7 = Special Type:

D = Pulldown

ED = Controllable Pulldown

U = Pullup

EU = Controllable Pullup

HV = High Voltage Input Pin(Special for PC3O01HV)

Power Pads Naming Conventions:

(0)12345

0 = A = cell supplied by analog power (for I/O)

1 = P = Pad; not a variable (for I/O)

2 = 3 = Voltage I/O = 1.8V

3 = V = V is for Power

4 = Output signal level:

0 = Low signal voltage

D = High signal voltage

C = Power ring cut cell

5 = Bus Structure:

A = I/O noisy

I = Internal (CORE) Power

F = All power buses shorted.

C = Core only power supply.

5.0 System Design Considerations

5.1 Power Connection Types

These power pads include 4 powers buses (2 VDD and 2 VSS) in normal cell and 5 powers buses (2 AVDD , 2 AVSS and 1 VSS) in cells supplied by analog power that can be used in different ways.

The VDD and VSS buses can be splitted in 4 sets, the core buses (Vdd, Vss), the switching buses (Vddo, Vsso), the analog core bused (AVdd, AVss) and the analog switch buses (AVddo, AVsso).

The power pad cells that supply the power buses are describe in the following section.

5.2 Power Pad Combinations for the TSL18CIO150 Library

The following tables map the power cells to their respective sources. Details and recommendations on the optimum use of power buses is described in the *I/O usage application note & SSO guidelines.*

VSS Power Pad Combinations

Power buses				Library Cell Name	Usage		
Vss	Vsso	AVss	AVsso		(1)	(2)	(3)
•				PV0I	•		
	•			PV0A	•		
				PV0C	(•)	(•)	
•	•			PV0F		•	
		•		APV0I			•
			•	APV0A			•

VDD Power Pad Combinations

Power buses				Library Cell Name	Usage		
Vdd	Vddo	AVdd	AVddo		(1)	(2)	(3)
•				PVDI	•		
	•			PVDA	•		
				PVDC	(•)	(•)	
		•		APVDI			•
			•	APVDA			•

The previous tables give also the usage of the power pad in 3 configurations:

(1): 2 power pads VSS and 2 power pads VDD are used, each of them supply on bus.
(2): 1 power pad VSS is used, all types of ground buses are shorted.
(3): 2 power pad AVSS ,1 power pad VSS and 2 power pads AVDD are used, each of them supply on bus.

Note1: The pads PVDC/PV0C can be used optionally with any combination of the other power pads (1), (2).

Note2: The combinations (2) are not available for VDD power pads in mixed power voltage I/O library.

5.3 Frequently Asked Questions (FAQ)

These are the types of questions that a system designer might ask:

•*Should I use separate power busses*?

Separate busses are recommended to reduce SSO noise.

•*My chip is very low performance and does not produce much noise. Is there a power pad I could use to reduce the number of power pads?*

•*I want to supply two standard cell group by two different powers. One of the power is the same than the VDD used in the I/O. The other is used to supply only standard cells.*

You have to use PVDI to supply the first group of standard cells plus the VDD I/O ring. You need also PVDC to supply the second group of standard cells with the independent power supply.

•*I have two I/O groups whose one is very noisy and the other not. I want to sepa-*

rate the power supply of these I/O.

Use the pad PVCF to cut the ring if VDD, VSS is not common to every I/O, you need then to supply each part of the ring with a PVDI, PV0I pads. Use the pad PVCE to cut the ring if VDD, VSS is common to every I/O.

5.4 Cell Matrices

This section gives a quick-reference guide to the TSL18CIO150 library pads.

TABLE 5.4.1. CMOS I/O Pads

CMOS Cell Name	3-State I/O	Output Only	3-State Output Only	Drive Strength	Pulldown Device	Pullup Device	Pad Sites Used
PC3B01	•			1x			1
PC3B02	•			2x			1
PC3B03	•			3x			1
PC3B04	•			4x			1
PC3B05	•			5x			1
PC3B01D	•			1x	•		1
PC3B02D	•			2x	•		1
PC3B03D	•			3x	•		1
PC3B03ED	•			3x	•		1
PC3B04D	•			4x	•		1
PC3B05D	•			5x	•		1
PC3B01U	•			1x		•	1
PC3B02U	•			2x		•	1
PC3B03U	•			3x		•	1
PC3B04U	•			4x		•	1
PC3B21EU	•			1x		•	1
PC3B25EU	•			5x		•	1
PC3B05U	•			5x		•	1
PC3O01		•		1x			1
PC3O01HV		•		1x			1
PC3O02		•		2x			1

TABLE 5.4.1. CMOS I/O Pads (Continued)

CMOS Cell Name	3-State I/O	Output Only	3-State Output Only	Drive Strength	Pulldown Device	Pullup Device	Pad Sites Used
PC3O03		•		3x			1
PC3O04		•		4x			1
PC3O05		•		5x			1
PC3T01			•	1x			1
PC3T02			•	2x			1
PC3T03			•	3x			1
PC3T04			•	4x			1
PC3T05			•	5x			1
PC3T01D			•	1x	•		1
PC3T02D			•	2x	•		1
PC3T03D			•	3x	•		1
PC3T04D			•	4x	•		1
PC3T05D			•	5x	•		1
PC3T01U			•	1x		•	1
PC3T02U			•	2x		•	1
PC3T03U			•	3x		•	1
PC3T04U			•	4x		•	1
PC3T05U			•	5x		•	1

TABLE 5.4.2. TTL I/O Pads

TTL Cell Name	3-State I/O	Output Only	3-State Output Only	Drive Strength	Pulldown Device	Pullup Device	Pad Sites Used
PT3B01	•			2mA			1
PT3B02	•			6mA			1
PT3B03	•			10mA			1
PT3B01D	•			2mA	•		1

TABLE 5.4.2. TTL I/O Pads (Continued)

PT3B02D	•			6mA	•		1
PT3B03D	•			10mA	•		1
PT3B01U	•			2mA		•	1
PT3B02U	•			6mA		•	1
PT3B03U	•			10mA		•	1
PT3O01		•		2mA			1
PT3O02		•		6mA			1
PT3O03		•		10mA			1
PT3T01			•	2mA			1
PT3T02			•	6mA			1
PT3T03			•	10mA			1
PT3T01D			•	2mA	•		1
PT3T02D			•	6mA	•		1
PT3T03D			•	10mA	•		1
PT3T01U			•	2mA		•	1
PT3T02U			•	6mA		•	1
PT3T03U			•	10mA		•	1

TABLE 5.4.3. Analog I/O Pads

CMOS Cell Name	Input Levels	Schmitt Input Level Shifter	Non-Inverting	Inverting	Pulldown Device	Pullup Device	Pad Sites Used
PC3D00	ANALOG		•				1

TABLE 5.4.4. CMOS Input Only Pads

CMOS Cell Name	Input Levels	Schmitt Input Level Shifter	Non-Inverting	Inverting	Pulldown Device	Pullup Device	Pad Sites Used
APC3D01	CMOS		•				1
PC3D01	CMOS		•				1

TABLE 5.4.4. CMOS Input Only Pads (Continued)

PC3D01D	CMOS		•		•		1
PC3D01U	CMOS		•			•	1
PC3D11	CMOS			•			1
PC3D11D	CMOS			•	•		1
PC3D11U	CMOS			•		•	1
PC3D21	CMOS	•	•				1
PC3D21D	CMOS	•	•		•		1
PC3D21EU	CMOS	•	•			•	1
PC3D21U	CMOS	•	•			•	1
PC3D31	CMOS	•		•			1
PC3D31D	CMOS	•		•	•		1
PC3D31U	CMOS	•		•		•	1

TABLE 5.4.5. Crystal Oscillator Pads

Cell Name	Frequency Category	Maximum Operating Frequency	Pad Sites Used
PC3X11	Low	10MHz	2
PC3X12	Intermediate	40MHz	2
PC3X13	High	100MHz	2

TABLE 5.4.6. Core-Driven Clock Buffer Pad

Cell Name	Drive Strength	Non-Inverting	Inverting	Pad Sites Used
PC3C01	1x	•		1
PC3C02	2x	•		1
PC3C03	3x	•		1
PC3C04	4x	•		1

TABLE 5.4.7. Power Pads

	Power Bus Connections								Pad Sites Used
	vssi	vsso	avssi	avsso	vddi	vddo	avddi	avddo	
PV0I	•								1
PV0A		•							1
PV0C									1 (**)
PV0F	•	•							1
APV0I			•						1
APV0A				•					1
PVDI					•				1
PVDA						•			1
PVDC									1 (**)
APVDI							•		1
APVDA								•	1

**) Note: PVDC/PV0C is used to supply VDD/VSS to core only then do not supply any I/O power ring.

TABLE 5.4.8. Cut Power Pads

	Cut Power Bus							
	vssi	vsso	avss	avsso	vddi	vddo	avdd	avddo
PVCF		•	•	•	•	•	•	•
PVCE	•	•	•	•		•	•	•
APFEEDENDRINGL		•	•	•	•	•	•	•
APFEEDENDRINGR		•	•	•	•	•	•	•

5.5 I/O Filler and Corner Pads List

I/O filler pads are used to fill gaps in the pad ring of chip.
Corner pads are placed at corners of pad ring at different orientation.

Name	Width (um)
pfeed00010	0.01
pfeed00040	0.04
pfeed00120	0.12
pfeed00540	0.54
pfeed01000	1
pfeed02000	2
pfeed10000	10
pfeed30000	30
pfrelr	Corner Pad

5.6 Analog section I/O Filler and Corner Pads List

Analog section I/O filler pads are used to fill gaps in the cells supplied by analog power of chip.
Corner pads are placed at corners of cells supplied by analog power at different orientation.

Name	Width (um)
apfeed00010	0.01
apfeed00040	0.04
apfeed00120	0.12
apfeed00540	0.54
apfeed01000	1
apfeed02000	2
apfeed10000	10

Name	Width (um)
apfeed30000	30
apfrelr	Corner Pad

Chapter 2
Characteristics

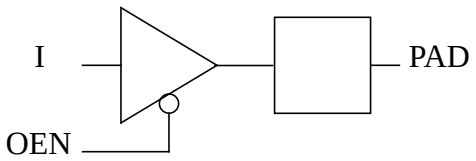
This chapter includes the characteristics tables for the following I/O Pads:

For a detailed description of each parameter, refer to *“Introduction” on page 1-1*.

1.8V CMOS 3-State Output Pads

PC3T01 through PC3T05

PC3T01 through PC3T05 cells are three state CMOS output pads with AC drive capabilities ranging from 1x to 5x.



Function Table

INPUT		OUTPUT
OEN	I	PAD
H	X	Z
L	L	L
L	H	H

Cell Description

Macro Name:	PC3T01	PC3T02	PC3T03	PC3T04	PC3T05
Drive Capability:	1x	2x	3x	4x	5x
Leakage Power (pW)	2853.3	2788.6	2855.4	2855.4	2858.1

Pin Description

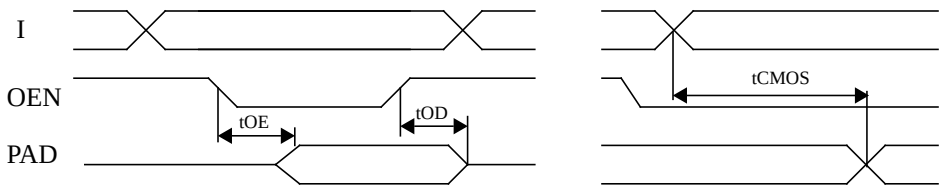
Name	Capacitance (pF)					Description
	PC3T01	PC3T02	PC3T03	PC3T04	PC3T05	
I	0.112	0.188	0.195	0.198	0.198	Input
OEN	0.11	0.11	0.11	0.11	0.11	Output Enable
PAD	3.185	3.182	3.188	3.188	3.188	3-StateOutput

Pin Powers for:
Standard Pad Load = 10.0 pF, Standard Core Input Transition = 0.1 ns

Name	Pin Power (pW/Hz)				
	PC3T01	PC3T02	PC3T03	PC3T04	PC3T05
PAD	21	21.5	22.3	22.9	23.8

1.8V CMOS 3-State Output Pads
PC3T01 through PC3T05

Waveforms



Timing Numbers for PC3T01 through PC3T05:

Propagation Delays (ns) for Sample Pad Loads:
Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3T01	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164
	tOEN	2.196	1.449	3.648	2.358	6.540	4.156	12.313	7.749
	tOD	1.001	1.497	1.001	1.497	1.001	1.497	1.001	1.497
PC3T02	tCMOS	2.236	1.832	2.975	2.326	4.430	3.241	7.329	5.049
	tOEN	1.617	1.336	2.356	1.832	3.809	2.747	6.703	4.559
	tOD	2.372	1.691	2.372	1.691	2.372	1.691	2.372	1.691
PC3T03	tCMOS	2.120	2.042	2.632	2.560	3.610	3.455	5.548	4.910
	tOEN	1.496	1.385	2.006	1.908	2.984	2.825	4.927	4.309
	tOD	2.498	1.875	2.500	1.875	2.497	1.875	2.495	1.875
PC3T04	tCMOS	2.147	2.065	2.556	2.497	3.306	3.223	4.773	4.418
	tOEN	1.481	1.275	1.888	1.726	2.640	2.458	4.112	3.677
	tOD	2.935	2.065	2.928	2.064	2.922	2.062	2.917	2.061
PC3T05	tCMOS	2.240	1.784	2.583	2.181	3.200	2.781	4.387	3.827
	tOEN	1.424	1.188	1.763	1.578	2.378	2.193	3.568	3.261
	tOD	3.338	2.265	3.338	2.265	3.349	2.265	3.354	2.265

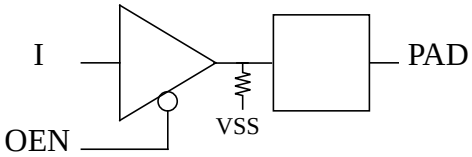
1.8V CMOS 3-State Output Pads
PC3T01 through PC3T05

Propagation Delays (ns) for Sample Core Input Transitions: Standard Pad Load = 16 pF

Cell Name	Type Delay	Core Input Transition							
		0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3T01	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135
	tOEN	3.648	2.358	3.687	2.400	3.797	2.490	3.956	2.676
	tOD	1.001	1.497	1.042	1.539	1.168	1.654	1.384	1.821
PC3T02	tCMOS	2.975	2.326	3.023	2.374	3.136	2.493	3.322	2.707
	tOEN	2.356	1.832	2.395	1.874	2.501	1.974	2.693	2.158
	tOD	2.372	1.691	2.446	1.746	2.563	1.860	2.763	2.010
PC3T03	tCMOS	2.632	2.560	2.680	2.601	2.797	2.712	3.000	2.909
	tOEN	2.006	1.908	2.044	1.950	2.152	2.039	2.335	2.239
	tOD	2.500	1.875	2.549	1.922	2.664	2.062	2.831	2.267
PC3T04	tCMOS	2.556	2.497	2.598	2.548	2.714	2.659	2.899	2.857
	tOEN	1.888	1.726	1.928	1.766	2.030	1.863	2.227	2.032
	tOD	2.928	2.064	2.958	2.104	3.070	2.223	3.294	2.423
PC3T05	tCMOS	2.583	2.181	2.625	2.229	2.748	2.339	2.948	2.523
	tOEN	1.763	1.578	1.796	1.608	1.905	1.705	2.089	1.890
	tOD	3.338	2.265	3.382	2.333	3.496	2.424	3.598	2.591

1.8V CMOS 3-State Output Pads with Pull-down Resistor
PC3T01D through PC3T05D

PC3T01D through PC3T05D cells are three state CMOS output pads with pull-down and AC drive capabilities ranging from 1x to 5x.



Function Table

INPUT		OUTPUT
OEN	I	PAD
H	X	Lr
L	L	L
L	H	H

Lr = Resistive-Low Drive Strength

Cell Description

Macro Name:	PC3T01D	PC3T02D	PC3T03D	PC3T04D	PC3T05D
Drive Capability:	1x	2x	3x	4x	5x
Leakage Power (pW)	2853.3	2788.6	2855.4	2855.4	2858.1

Pin Description

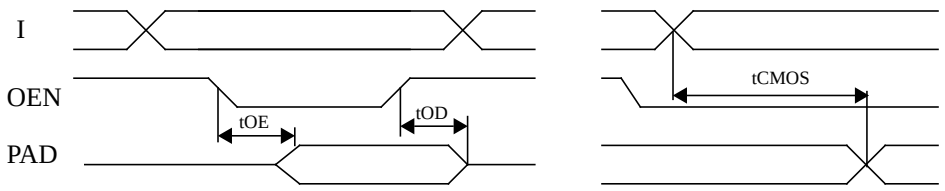
Name	Capacitance (pF)					Description
	PC3T01D	PC3T02D	PC3T03D	PC3T04D	PC3T05D	
I	0.112	0.192	0.19	0.198	0.198	Input
OEN	0.11	0.11	0.11	0.11	0.11	Output Enable
PAD	3.185	3.172	3.178	3.18	3.18	3-StateOutput

Pin Powers for:
Standard Pad Load = 10.0 pF, Standard Core Input Transition = 0.1 ns

Name	Pin Power (pW/Hz)				
	PC3T01D	PC3T02D	PC3T03D	PC3T04D	PC3T05D
PAD	21	21.9	22.7	23.3	24.1

1.8V CMOS 3-State Output Pads with Pull-down Resistor
PC3T01D through PC3T05D

Waveforms



Timing Numbers for PC3T01D through PC3T05D:

Propagation Delays (ns) for Sample Pad Loads:
Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3T01D	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164
	tOEN	2.196	1.449	3.648	2.358	6.540	4.156	12.313	7.749
	tOD	1.001	1.497	1.001	1.497	1.001	1.497	1.001	1.497
PC3T02D	tCMOS	2.245	1.831	2.986	2.322	4.439	3.234	7.334	5.042
	tOEN	1.618	1.298	2.358	1.802	3.816	2.717	6.714	4.526
	tOD	2.371	1.687	2.370	1.687	2.367	1.687	2.365	1.687
PC3T03D	tCMOS	2.127	2.039	2.636	2.554	3.614	3.449	5.553	4.906
	tOEN	1.493	1.340	2.008	1.874	2.991	2.795	4.931	4.278
	tOD	2.499	1.875	2.501	1.875	2.501	1.875	2.501	1.875
PC3T04D	tCMOS	2.145	2.071	2.554	2.501	3.306	3.221	4.773	4.412
	tOEN	1.480	1.244	1.889	1.703	2.644	2.435	4.114	3.654
	tOD	2.935	2.055	2.932	2.055	2.928	2.055	2.925	2.055
PC3T05D	tCMOS	2.243	1.777	2.589	2.172	3.206	2.772	4.394	3.822
	tOEN	1.411	1.156	1.750	1.550	2.375	2.172	3.567	3.245
	tOD	3.336	2.282	3.328	2.282	3.341	2.282	3.351	2.279

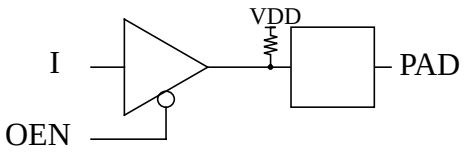
1.8V CMOS 3-State Output Pads with Pull-down Resistor
PC3T01D through PC3T05D

Propagation Delays (ns) for Sample Core Input Transitions: Standard Pad Load = 16 pF

Cell Name	Type Delay	Core Input Transition							
		0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3T01D	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135
	tOEN	3.648	2.358	3.687	2.400	3.797	2.490	3.956	2.676
	tOD	1.001	1.497	1.042	1.539	1.168	1.654	1.384	1.821
PC3T02D	tCMOS	2.986	2.322	3.020	2.365	3.138	2.488	3.321	2.718
	tOEN	2.358	1.802	2.396	1.844	2.503	1.936	2.698	2.120
	tOD	2.370	1.687	2.455	1.737	2.568	1.860	2.784	2.010
PC3T03D	tCMOS	2.636	2.554	2.679	2.600	2.799	2.712	2.999	2.912
	tOEN	2.008	1.874	2.051	1.917	2.158	2.007	2.356	2.193
	tOD	2.501	1.875	2.542	1.922	2.674	2.049	2.843	2.263
PC3T04D	tCMOS	2.554	2.501	2.595	2.547	2.716	2.659	2.900	2.859
	tOEN	1.889	1.703	1.935	1.740	2.031	1.835	2.231	2.004
	tOD	2.932	2.055	2.975	2.102	3.068	2.222	3.284	2.422
PC3T05D	tCMOS	2.589	2.172	2.628	2.220	2.745	2.343	2.931	2.541
	tOEN	1.750	1.550	1.794	1.587	1.909	1.677	2.107	1.861
	tOD	3.328	2.282	3.374	2.342	3.491	2.436	3.606	2.569

1.8V CMOS 3-State Output Pads with Pull-up Resistor
PC3T01U through PC3T05U

PC3T01U through PC3T05U cells are three state CMOS output pads with pullup and AC drive capabilities ranging from 1x to 5x



Function Table

INPUT		OUTPUT
OEN	I	PAD
H	X	Hr
L	L	L
L	H	H

Hr = Resistive-High Drive Strength

Cell Description

Macro Name:	PC3T01U	PC3T02U	PC3T03U	PC3T04U	PC3T05U
Drive Capability:	1x	2x	3x	4x	5x
Leakage Power (µW)	30.611	30.611	30.611	30.611	30.611

Pin Description

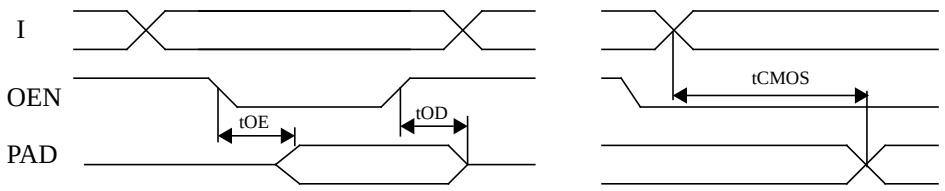
Name	Capacitance (pF)					Description
	PC3T01U	PC3T02U	PC3T03U	PC3T04U	PC3T05U	
I	0.112	0.188	0.195	0.198	0.198	Input
OEN	0.11	0.11	0.11	0.11	0.11	Output Enable
PAD	3.185	3.168	3.172	3.175	3.172	3-StateOutput

Pin Powers for:
Standard Pad Load = 10.0 pF, Standard Core Input Transition = 0.1 ns

Name	Pin Power (pW/Hz)				
	PC3T01U	PC3T02U	PC3T03U	PC3T04U	PC3T05U
PAD	21	22	22.9	23.4	24.3

1.8V CMOS 3-State Output Pads with Pull-up Resistor
PC3T01U through PC3T05U

Waveforms



Timing Numbers for PC3T01U through PC3T05U:

Propagation Delays (ns) for Sample Pad Loads:
Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3T01U	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164
	tOEN	2.196	1.449	3.648	2.358	6.540	4.156	12.313	7.749
	tOD	1.001	1.497	1.001	1.497	1.001	1.497	1.001	1.497
PC3T02U	tCMOS	2.237	1.833	2.976	2.327	4.429	3.242	7.319	5.053
	tOEN	1.578	1.337	2.317	1.833	3.770	2.748	6.661	4.563
	tOD	2.372	1.685	2.372	1.685	2.372	1.685	2.372	1.685
PC3T03U	tCMOS	2.121	2.045	2.627	2.561	3.609	3.456	5.544	4.911
	tOEN	1.467	1.389	1.982	1.912	2.957	2.825	4.895	4.308
	tOD	2.501	1.881	2.501	1.881	2.501	1.881	2.501	1.881
PC3T04U	tCMOS	2.146	2.071	2.552	2.503	3.299	3.226	4.767	4.420
	tOEN	1.456	1.280	1.869	1.733	2.622	2.463	4.094	3.686
	tOD	2.922	2.065	2.911	2.065	2.911	2.065	2.911	2.063
PC3T05U	tCMOS	2.242	1.785	2.580	2.182	3.199	2.782	4.388	3.828
	tOEN	1.398	1.190	1.741	1.578	2.360	2.193	3.550	3.258
	tOD	3.336	2.275	3.337	2.275	3.345	2.275	3.348	2.279

1.8V CMOS 3-State Output Pads with Pull-up Resistor
PC3T01U through PC3T05U

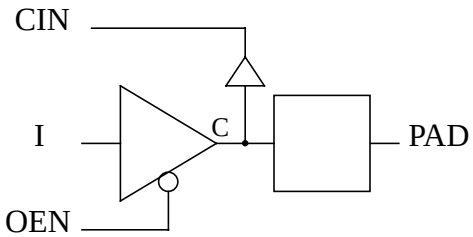
Propagation Delays (ns) for Sample Core Input Transitions: Standard Pad Load = 16 pF

Cell Name	Type Delay	Core Input Transition							
		0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3T01U	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135
	tOEN	3.648	2.358	3.687	2.400	3.797	2.490	3.956	2.676
	tOD	1.001	1.497	1.042	1.539	1.168	1.654	1.384	1.821
PC3T02U	tCMOS	2.976	2.327	3.017	2.375	3.136	2.493	3.322	2.708
	tOEN	2.317	1.833	2.355	1.875	2.457	1.971	2.635	2.141
	tOD	2.372	1.685	2.446	1.732	2.563	1.864	2.763	2.031
PC3T03U	tCMOS	2.627	2.561	2.674	2.609	2.798	2.713	2.998	2.913
	tOEN	1.982	1.912	2.021	1.948	2.124	2.045	2.305	2.228
	tOD	2.501	1.881	2.547	1.936	2.664	2.062	2.831	2.267
PC3T04U	tCMOS	2.552	2.503	2.589	2.549	2.710	2.660	2.910	2.857
	tOEN	1.869	1.733	1.906	1.770	2.010	1.859	2.208	2.042
	tOD	2.911	2.065	2.952	2.104	3.081	2.223	3.348	2.423
PC3T05U	tCMOS	2.580	2.182	2.623	2.230	2.745	2.340	2.931	2.523
	tOEN	1.741	1.578	1.775	1.609	1.886	1.705	2.069	1.891
	tOD	3.337	2.275	3.381	2.342	3.457	2.424	3.671	2.591

1.8V CMOS 3-State I/O Pads

PC3B01 through PC3B05

PC3B01 through PC3B05 cells are three state CMOS input/output pads with AC drive capabilities ranging from 1x to 5x.



Function Table

INPUT		OUTPUTS	
OEN	I	PAD	CIN
H	X	Zl	L
H	X	Zh	H
L	L	L	L
L	H	H	H

Cell Description

Macro Name:	PC3B01	PC3B02	PC3B03	PC3B04	PC3B05
Drive Capability	1x	2x	3x	4x	5x
Leakage Power (pW):	2853.3	3051.6	3118.4	3118.4	3121.1

Pin Description

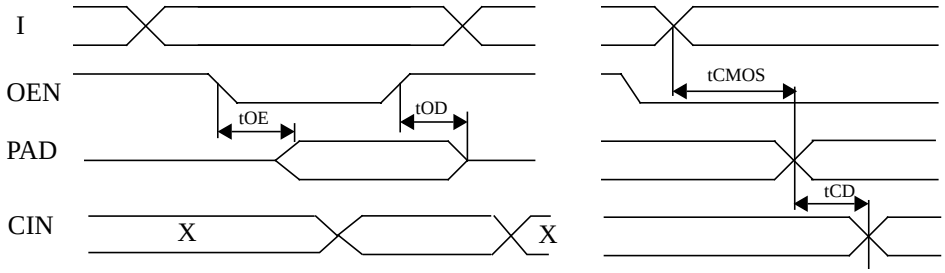
Name	Capacitance (pF)					Description
	PC3B01	PC3B02	PC3B03	PC3B04	PC3B05	
I	0.112	0.198	0.18	0.18	0.18	Input
OEN	0.11	0.11	0.11	0.11	0.11	Output Enable
PAD	3.185	3.182	3.188	3.188	3.188	3-StateOutput
Maximum capacitance						
CIN	0.8	0.8	0.8	0.8	0.8	Output

Pin Powers for:
Standard Pad load = 10.0 pF, Standard Core Input Transition = 0.1 ns
Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns

Name	Pin Power (pW/Hz)				
	PC3B01	PC3B02	PC3B03	PC3B04	PC3B05
PAD	21	21.5	22.4	23	23.9
CIN	5.6	5.6	5.6	5.6	5.4

1.8V CMOS 3-State I/O Pads
PC3B01 through PC3B05

Waveforms



Timing Numbers for PC3B01 through PC3B05:

Propagation Delays tCD (ns) for Sample Core Loads:
Standard Pad Input Transition = 1 ns, Core Load Unit = 0.01 pF

Cell Name	Core Load Fanout									
	2		4		8		16		32	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B01	0.553	0.897	0.565	0.913	0.590	0.947	0.632	1.012	0.715	1.142
PC3B02	0.541	0.879	0.553	0.897	0.578	0.933	0.619	0.999	0.700	1.130
PC3B03	0.541	0.880	0.553	0.899	0.578	0.935	0.621	1.000	0.706	1.130
PC3B04	0.541	0.880	0.553	0.899	0.578	0.935	0.621	1.000	0.706	1.130
PC3B05	0.541	0.880	0.553	0.899	0.578	0.935	0.621	1.000	0.706	1.130

Propagation Delays tCD (ns) for Sample Pad Input Transitions:
Standard Core Load = 0.16 pF

Cell Name	Pad Input Transition									
	1 ns		2 ns		5 ns		10 ns		15 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B01	0.632	1.012	0.778	1.245	0.979	1.736	1.163	2.355	1.346	2.974
PC3B02	0.619	0.999	0.763	1.218	0.960	1.717	1.135	2.340	1.310	2.963
PC3B03	0.621	1.000	0.763	1.225	0.960	1.717	1.135	2.338	1.310	2.958
PC3B04	0.621	1.000	0.763	1.225	0.960	1.717	1.135	2.338	1.310	2.958
PC3B05	0.621	1.000	0.763	1.225	0.960	1.717	1.135	2.338	1.310	2.958

1.8V CMOS 3-State I/O Pads
PC3B01 through PC3B05

Propagation Delays (ns) for Sample Pad Loads:
Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B01	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164
	tOEN	2.196	1.449	3.648	2.358	6.540	4.156	12.313	7.749
	tOD	1.001	1.497	1.001	1.497	1.001	1.497	1.001	1.497
PC3B02	tCMOS	2.241	1.832	2.978	2.326	4.428	3.241	7.322	5.049
	tOEN	1.619	1.334	2.359	1.838	3.810	2.753	6.703	4.560
	tOD	2.378	1.691	2.378	1.691	2.378	1.691	2.378	1.691
PC3B03	tCMOS	2.127	2.044	2.635	2.559	3.612	3.451	5.555	4.910
	tOEN	1.493	1.377	2.005	1.902	2.980	2.818	4.923	4.306
	tOD	2.501	1.887	2.501	1.887	2.503	1.887	2.505	1.887
PC3B04	tCMOS	2.145	2.069	2.553	2.503	3.305	3.228	4.771	4.421
	tOEN	1.478	1.272	1.887	1.725	2.637	2.454	4.109	3.674
	tOD	2.920	2.094	2.913	2.094	2.908	2.094	2.905	2.094
PC3B05	tCMOS	2.240	1.780	2.583	2.176	3.200	2.781	4.394	3.829
	tOEN	1.416	1.180	1.755	1.570	2.375	2.192	3.563	3.263
	tOD	3.315	2.268	3.314	2.268	3.317	2.268	3.339	2.268

1.8V CMOS 3-State I/O Pads
PC3B01 through PC3B05

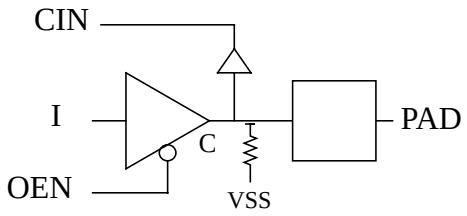
Propagation Delays (ns) for Sample Core Input Transitions: Standard Pad Load = 16 pF

Cell Name	Type Delay	Core Input Transition							
		0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B01	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135
	tOEN	3.648	2.358	3.687	2.400	3.797	2.490	3.956	2.676
	tOD	1.001	1.497	1.042	1.539	1.168	1.654	1.384	1.821
PC3B02	tCMOS	2.978	2.326	3.024	2.374	3.136	2.493	3.319	2.710
	tOEN	2.359	1.838	2.396	1.868	2.501	1.968	2.693	2.166
	tOD	2.378	1.691	2.461	1.732	2.556	1.864	2.747	2.031
PC3B03	tCMOS	2.635	2.559	2.676	2.601	2.797	2.712	3.000	2.909
	tOEN	2.005	1.902	2.050	1.943	2.153	2.044	2.334	2.227
	tOD	2.501	1.887	2.549	1.922	2.673	2.035	2.873	2.204
PC3B04	tCMOS	2.553	2.503	2.596	2.550	2.715	2.659	2.901	2.862
	tOEN	1.887	1.725	1.933	1.760	2.036	1.862	2.219	2.060
	tOD	2.913	2.094	2.967	2.114	3.108	2.223	3.286	2.423
PC3B05	tCMOS	2.583	2.176	2.625	2.223	2.745	2.344	2.929	2.544
	tOEN	1.755	1.570	1.794	1.612	1.905	1.705	2.089	1.890
	tOD	3.314	2.268	3.354	2.314	3.505	2.442	3.641	2.711

1.8V CMOS 3-State I/O Pads with Pull-down Resistor

PC3B01D through PC3B05D

PC3B01D through PC3B05D cells are three state CMOS input/output pads with pulldown and with AC drive capabilities ranging from 1x to 5x.



Function Table

INPUT		OUTPUTS	
OEN	I	PAD	CIN
H	X	Lr	L
L	L	L	L
L	H	H	H

Lr = Resistive-Low Drive Strength

Cell Description

Macro Name:	PC3B01D	PC3B02D	PC3B03D	PC3B04D	PC3B05D
Drive Capability	1x	2x	3x	4x	5x
Leakage Power (pW):	2853.3	3051.6	3118.4	3118.4	3121.1

Pin Description

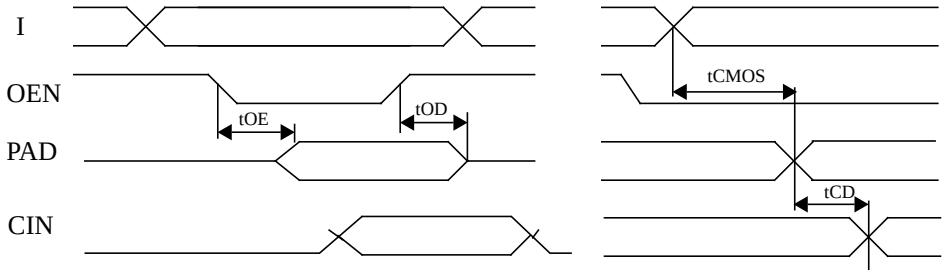
Name	Capacitance (pF)					Description
	PC3B01D	PC3B02D	PC3B03D	PC3B04D	PC3B05D	
I	0.112	0.2	0.18	0.178	0.18	Input
OEN	0.11	0.11	0.11	0.11	0.11	Output Enable
PAD	3.185	3.17	3.178	3.18	3.18	3-StateOutput
Maximum capacitance						
CIN	0.8	0.8	0.8	0.8	0.8	Output

Pin Powers for:
Standard Pad load = 10.0 pF, Standard Core Input Transition = 0.1 ns
Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns

Name	Pin Power (pW/Hz)				
	PC3B01D	PC3B02D	PC3B03D	PC3B04D	PC3B05D
PAD	21	21.9	22.8	23.3	24.2
CIN	5.6	5.5	5.5	5.6	5.5

1.8V CMOS 3-State I/O Pads with Pull-down Resistor
PC3B01D through PC3B05D

Waveforms



Timing Numbers for PC3B01D through PC3B05D:

Propagation Delays tCD (ns) for Sample Core Loads:
Standard Pad Input Transition = 1 ns, Core Load Unit = 0.01 pF

Cell Name	Core Load Fanout									
	2		4		8		16		32	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B01D	0.553	0.897	0.565	0.913	0.590	0.947	0.632	1.012	0.715	1.142
PC3B02D	0.553	0.889	0.565	0.908	0.590	0.947	0.632	1.013	0.716	1.145
PC3B03D	0.553	0.890	0.565	0.908	0.590	0.943	0.632	1.008	0.716	1.138
PC3B04D	0.553	0.890	0.565	0.909	0.590	0.945	0.632	1.008	0.716	1.133
PC3B05D	0.553	0.890	0.565	0.908	0.590	0.943	0.630	1.010	0.710	1.145

Propagation Delays tCD (ns) for Sample Pad Input Transitions:
Standard Core Load = 0.16 pF

Cell Name	Pad Input Transition									
	1 ns		2 ns		5 ns		10 ns		15 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B01D	0.632	1.012	0.778	1.245	0.979	1.736	1.163	2.355	1.346	2.974
PC3B02D	0.632	1.013	0.780	1.240	0.996	1.707	1.203	2.305	1.409	2.903
PC3B03D	0.632	1.008	0.780	1.225	0.995	1.710	1.195	2.308	1.395	2.905
PC3B04D	0.632	1.008	0.780	1.233	0.995	1.709	1.195	2.305	1.395	2.901
PC3B05D	0.630	1.010	0.780	1.225	0.995	1.707	1.195	2.293	1.395	2.878

1.8V CMOS 3-State I/O Pads with Pull-down Resistor
PC3B01D through PC3B05D

Propagation Delays (ns) for Sample Pad Loads:
Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B01D	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164
	tOEN	2.196	1.449	3.648	2.358	6.540	4.156	12.313	7.749
	tOD	1.001	1.497	1.001	1.497	1.001	1.497	1.001	1.497
PC3B02D	tCMOS	2.245	1.828	2.987	2.317	4.442	3.232	7.344	5.043
	tOEN	1.616	1.299	2.354	1.803	3.807	2.718	6.705	4.528
	tOD	2.374	1.691	2.374	1.691	2.374	1.691	2.374	1.691
PC3B03D	tCMOS	2.127	2.039	2.636	2.555	3.616	3.453	5.559	4.909
	tOEN	1.493	1.338	2.006	1.874	2.983	2.794	4.928	4.283
	tOD	2.503	1.887	2.502	1.887	2.506	1.887	2.508	1.887
PC3B04D	tCMOS	2.148	2.069	2.554	2.501	3.306	3.221	4.776	4.415
	tOEN	1.478	1.244	1.889	1.703	2.642	2.433	4.117	3.653
	tOD	2.939	2.068	2.931	2.068	2.921	2.068	2.915	2.068
PC3B05D	tCMOS	2.243	1.784	2.585	2.181	3.206	2.778	4.396	3.824
	tOEN	1.416	1.153	1.756	1.545	2.377	2.170	3.567	3.250
	tOD	3.306	2.262	3.298	2.262	3.309	2.262	3.316	2.259

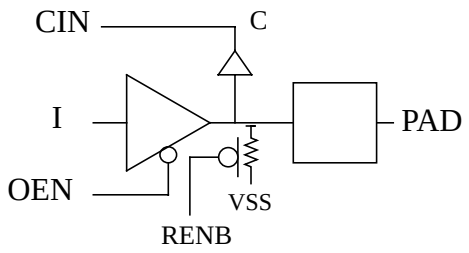
1.8V CMOS 3-State I/O Pads with Pull-down Resistor
PC3B01D through PC3B05D

Propagation Delays (ns) for Sample Core Input Transitions: Standard Pad Load = 16 pF

Cell Name	Type Delay	Core Input Transition							
		0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B01D	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135
	tOEN	3.648	2.358	3.687	2.400	3.797	2.490	3.956	2.676
	tOD	1.001	1.497	1.042	1.539	1.168	1.654	1.384	1.821
PC3B02D	tCMOS	2.987	2.317	3.028	2.365	3.137	2.488	3.323	2.719
	tOEN	2.354	1.803	2.399	1.846	2.507	1.940	2.688	2.112
	tOD	2.374	1.691	2.445	1.732	2.566	1.853	2.728	2.024
PC3B03D	tCMOS	2.636	2.555	2.684	2.600	2.799	2.712	2.999	2.915
	tOEN	2.006	1.874	2.051	1.922	2.163	2.012	2.346	2.204
	tOD	2.502	1.887	2.549	1.922	2.673	2.034	2.873	2.201
PC3B04D	tCMOS	2.554	2.501	2.602	2.549	2.711	2.660	2.911	2.857
	tOEN	1.889	1.703	1.933	1.738	2.036	1.834	2.220	2.032
	tOD	2.931	2.068	2.976	2.107	3.098	2.223	3.238	2.420
PC3B05D	tCMOS	2.585	2.181	2.626	2.222	2.749	2.339	2.947	2.520
	tOEN	1.756	1.545	1.801	1.587	1.909	1.677	2.107	1.861
	tOD	3.298	2.262	3.373	2.307	3.496	2.422	3.626	2.615

1.8V CMOS 3-State I/O Pad with Controllable Pull-down Resistor
PC3B03ED

PC3B03ED cell is three state CMOS input/output pad with controllable pulldown resistor, and with AC drive capabilities ranging 3x.



Function Table

	INPUT		OUTPUT	
RENB	OEN	I	PAD	CIN
X	H	X	L	L
X	H	X	H	H
L	H	X	Lr	L
H	H	X	Z	X
X	L	L	L	L
X	L	H	H	H

Cell Description

Macro Name:	PC3B03ED
Drive Capability	3x
Leakage Power (pW):	2855.4

Pin Description

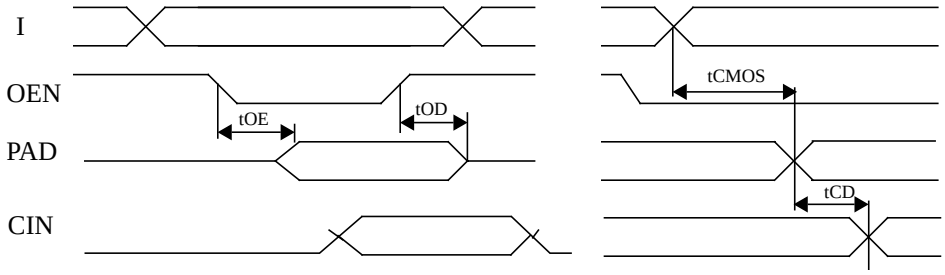
Name	Capacitance (pF)	Description
	PC3B03ED	
I	0.195	Input
RENB	0.11	Input
OEN	0.11	Output Enable
PAD	3.188	3-StateOutput
Maximum capacitance		
CIN	0.8	Output

Pin Powers for:
Standard Pad load = 10.0 pF, Standard Core Input Transition = 0.1 ns
Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns

Name	Pin Power (pW/Hz)
	PC3B03ED
PAD	22.3
CIN	9.9

1.8V CMOS 3-State I/O Pad with Controllable Pull-down Resistor
PC3B03ED

Waveforms



Timing Numbers for PC3B03ED:

Propagation Delays tCD (ns) for Sample Core Loads:
Standard Pad Input Transition = 1 ns, Core Load Unit = 0.01 pF

Cell Name	Core Load Fanout									
	2		4		8		16		32	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B03ED	0.455	0.410	0.465	0.420	0.485	0.438	0.528	0.469	0.613	0.530

Propagation Delays tCD (ns) for Sample Pad Input Transitions:
Standard Core Load = 0.16 pF

Cell Name	Pad Input Transition									
	1 ns		2 ns		5 ns		10 ns		15 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B03ED	0.528	0.469	0.553	0.613	0.574	0.927	0.530	1.385	0.486	1.843

1.8V CMOS 3-State I/O Pad with Controllable Pull-down Resistor
PC3B03ED

Propagation Delays (ns) for Sample Pad Loads:
Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B03ED	tCMOS	2.120	2.042	2.632	2.560	3.610	3.455	5.548	4.910
	tOEN	1.496	1.385	2.006	1.908	2.984	2.825	4.927	4.309
	tOD	2.498	1.875	2.500	1.875	2.497	1.875	2.495	1.875

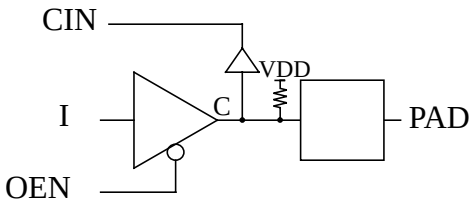
Propagation Delays (ns) for Sample Core Input Transitions:
Standard Pad Load = 16 pF

Cell Name	Type Delay	Core Input Transition							
		0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B03ED	tCMOS	2.632	2.560	2.680	2.601	2.797	2.712	3.000	2.909
	tOEN	2.006	1.908	2.044	1.950	2.152	2.039	2.335	2.239
	tOD	2.500	1.875	2.549	1.922	2.664	2.062	2.831	2.267

1.8V CMOS 3-State I/O Pads with Pull-up Resistor

PC3B01U through PC3B05U

PC3B01U through PC3B05U cells are three state CMOS input/output pads with pullup and with AC drive capabilities ranging from 1x to 5x.



Function Table

INPUT		OUTPUTS	
OEN	I	PAD	CIN
H	X	Hr	H
L	L	L	L
L	H	H	H

Hr = Resistive-High Drive Strength

Cell Description

Macro Name:	PC3B01U	PC3B02U	PC3B03U	PC3B04U	PC3B05U
Drive Capability	1x	2x	3x	4x	5x
Leakage Power (µW):	30.611	30.611	30.611	30.611	30.611

Pin Description

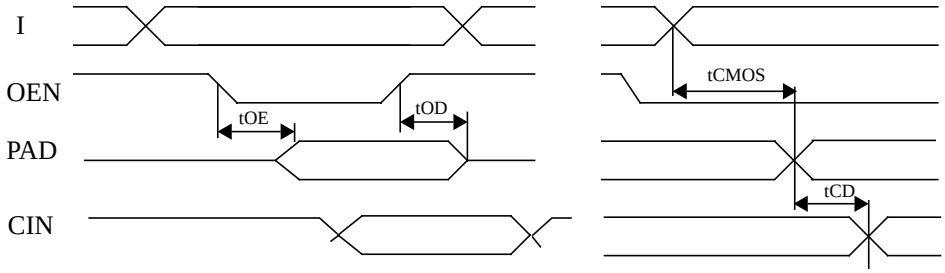
Name	Capacitance (pF)					Description
	PC3B01U	PC3B02U	PC3B03U	PC3B04U	PC3B05U	
I	0.112	0.195	0.18	0.18	0.18	Input
OEN	0.11	0.11	0.11	0.11	0.11	Output Enable
PAD	3.185	3.168	3.172	3.178	3.172	3-StateOutput
Maximum capacitance						
CIN	0.8	0.8	0.8	0.8	0.8	Output

Pin Powers for:
Standard Pad load = 10.0 pF, Standard Core Input Transition = 0.1 ns
Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns

Name	Pin Power (pW/Hz)				
	PC3B01U	PC3B02U	PC3B03U	PC3B04U	PC3B05U
PAD	21	22	22.9	23.4	24.3
CIN	5.6	5.8	5.6	5.7	5.6

1.8V CMOS 3-State I/O Pads with Pull-up Resistor
PC3B01U through PC3B05U

Waveforms



Timing Numbers for PC3B01U through PC3B05U:

Propagation Delays tCD (ns) for Sample Core Loads:
Standard Pad Input Transition = 1 ns, Core Load Unit = 0.01 pF

Cell Name	Core Load Fanout									
	2		4		8		16		32	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B01U	0.553	0.897	0.565	0.913	0.590	0.947	0.632	1.012	0.715	1.142
PC3B02U	0.539	0.883	0.552	0.903	0.578	0.945	0.620	1.010	0.705	1.140
PC3B03U	0.541	0.883	0.553	0.903	0.578	0.945	0.621	1.010	0.706	1.140
PC3B04U	0.541	0.883	0.553	0.904	0.578	0.947	0.621	1.011	0.706	1.140
PC3B05U	0.541	0.890	0.553	0.905	0.578	0.937	0.621	1.002	0.706	1.132

Propagation Delays tCD (ns) for Sample Pad Input Transitions:
Standard Core Load = 0.16 pF

Cell Name	Pad Input Transition									
	1 ns		2 ns		5 ns		10 ns		15 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B01U	0.632	1.012	0.778	1.245	0.979	1.736	1.163	2.355	1.346	2.974
PC3B02U	0.620	1.010	0.760	1.235	0.937	1.740	1.095	2.388	1.253	3.035
PC3B03U	0.621	1.010	0.763	1.235	0.937	1.744	1.095	2.378	1.253	3.011
PC3B04U	0.621	1.011	0.763	1.243	0.937	1.738	1.095	2.378	1.253	3.017
PC3B05U	0.621	1.002	0.763	1.235	0.937	1.746	1.095	2.390	1.253	3.034

1.8V CMOS 3-State I/O Pads with Pull-up Resistor
PC3B01U through PC3B05U

Propagation Delays (ns) for Sample Pad Loads:
Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B01U	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164
	tOEN	2.196	1.449	3.648	2.358	6.540	4.156	12.313	7.749
	tOD	1.001	1.497	1.001	1.497	1.001	1.497	1.001	1.497
PC3B02U	tCMOS	2.239	1.833	2.977	2.327	4.422	3.242	7.309	5.055
	tOEN	1.580	1.337	2.320	1.834	3.771	2.752	6.661	4.563
	tOD	2.385	1.697	2.385	1.697	2.385	1.697	2.385	1.694
PC3B03U	tCMOS	2.123	2.045	2.632	2.560	3.609	3.452	5.549	4.911
	tOEN	1.464	1.382	1.976	1.909	2.951	2.824	4.897	4.300
	tOD	2.498	1.881	2.495	1.881	2.497	1.881	2.498	1.881
PC3B04U	tCMOS	2.142	2.071	2.548	2.503	3.303	3.228	4.770	4.422
	tOEN	1.453	1.276	1.865	1.726	2.617	2.456	4.089	3.678
	tOD	2.906	2.075	2.906	2.075	2.913	2.075	2.917	2.075
PC3B05U	tCMOS	2.240	1.778	2.580	2.173	3.199	2.776	4.388	3.822
	tOEN	1.393	1.184	1.739	1.571	2.359	2.194	3.547	3.266
	tOD	3.312	2.268	3.329	2.268	3.342	2.268	3.351	2.268

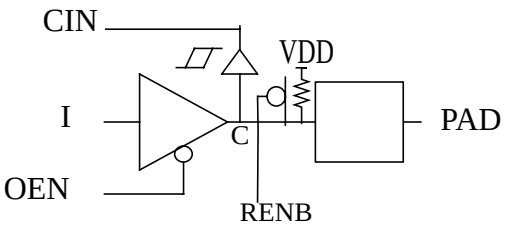
1.8V CMOS 3-State I/O Pads with Pull-up Resistor
PC3B01U through PC3B05U

Propagation Delays (ns) for Sample Core Input Transitions: Standard Pad Load = 16 pF

Cell Name	Type Delay	Core Input Transition							
		0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B01U	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135
	tOEN	3.648	2.358	3.687	2.400	3.797	2.490	3.956	2.676
	tOD	1.001	1.497	1.042	1.539	1.168	1.654	1.384	1.821
PC3B02U	tCMOS	2.977	2.327	3.018	2.375	3.136	2.494	3.322	2.711
	tOEN	2.320	1.834	2.357	1.876	2.462	1.975	2.626	2.159
	tOD	2.385	1.697	2.446	1.746	2.556	1.869	2.749	2.022
PC3B03U	tCMOS	2.632	2.560	2.674	2.602	2.789	2.713	2.989	2.910
	tOEN	1.976	1.909	2.021	1.944	2.129	2.041	2.295	2.236
	tOD	2.495	1.881	2.557	1.929	2.663	2.039	2.863	2.222
PC3B04U	tCMOS	2.548	2.503	2.595	2.556	2.715	2.660	2.898	2.860
	tOEN	1.865	1.726	1.911	1.761	2.015	1.864	2.198	2.062
	tOD	2.906	2.075	2.965	2.136	3.097	2.223	3.278	2.423
PC3B05U	tCMOS	2.580	2.173	2.623	2.220	2.745	2.341	2.931	2.526
	tOEN	1.739	1.571	1.778	1.613	1.881	1.706	2.079	1.889
	tOD	3.329	2.268	3.356	2.329	3.495	2.442	3.626	2.711

1.8V CMOS 3-State I/O Pads with Controllable Pull-up Resistor
PC3B21EU PC3B25EU

PC3B21EU PC3B25EU cells are three state CMOS Schmitt non inverting input/ output pads with controllable pullup resistor, AC drive capabilities ranging 1x, 5x.



Function Table

INPUT			OUTPUT	
RENB	OEN	I	PAD	CIN
X	H	X	L	L
X	H	X	H	H
L	H	X	Hr	H
H	H	X	Z	X
X	L	L	L	L
X	L	H	H	H

Cell Description

Macro Name:	PC3B21EU	PC3B25EU
Drive Capability	1x	5x
Leakage Power (µW):	30.611	30.611

Pin Description

Name	Capacitance (pF)		Description
	PC3B21EU	PC3B25EU	
I	0.112	0.18	Input
RENB	0.11	0.11	Input
OEN	0.11	0.11	Output Enable
PAD	3.185	3.172	3-StateOutput
Maximum capacitance			
CIN	0.8	0.8	Output

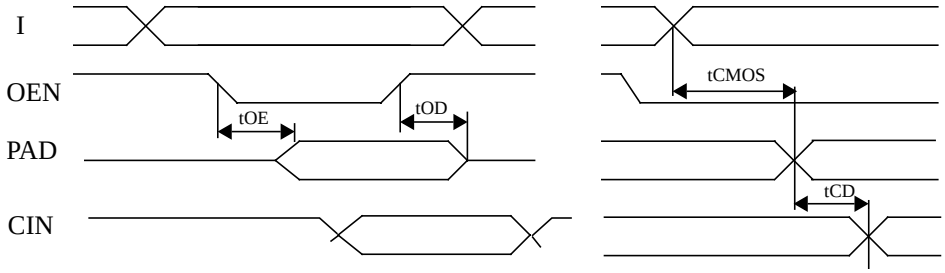
Pin Powers for:
Standard Pad load = 10.0 pF, Standard Core Input Transition = 0.1 ns
Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns

Name	Pin Power (pW/Hz)	
	PC3B21EU	PC3B25EU
PAD	21	24.3
CIN	5.6	5.6

1.8V CMOS 3-State I/O Pads with Controllable Pull-up Resistor

PC3B21EU PC3B25EU

Waveforms



Timing Numbers for PC3B21EU PC3B25EU:

Propagation Delays tCD (ns) for Sample Core Loads:
Standard Pad Input Transition = 1 ns, Core Load Unit = 0.01 pF

Cell Name	Core Load Fanout									
	2		4		8		16		32	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B21EU	0.553	0.897	0.565	0.913	0.590	0.947	0.632	1.012	0.715	1.142
PC3B25EU	0.541	0.890	0.553	0.905	0.578	0.937	0.621	1.002	0.706	1.132

Propagation Delays tCD (ns) for Sample Pad Input Transitions:
Standard Core Load = 0.16 pF

Cell Name	Pad Input Transition									
	1 ns		2 ns		5 ns		10 ns		15 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B21EU	0.632	1.012	0.778	1.245	0.979	1.736	1.163	2.355	1.346	2.974
PC3B25EU	0.621	1.002	0.763	1.235	0.937	1.746	1.095	2.390	1.253	3.034

1.8V CMOS 3-State I/O Pads with Controllable Pull-up Resistor
PC3B21EU PC3B25EU

Propagation Delays (ns) for Sample Pad Loads: Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B21EU	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164
	tOEN	2.196	1.449	3.648	2.358	6.540	4.156	12.313	7.749
	tOD	1.001	1.497	1.001	1.497	1.001	1.497	1.001	1.497
PC3B25EU	tCMOS	2.240	1.778	2.580	2.173	3.199	2.776	4.388	3.822
	tOEN	1.393	1.184	1.739	1.571	2.359	2.194	3.547	3.266
	tOD	3.312	2.268	3.329	2.268	3.342	2.268	3.351	2.268

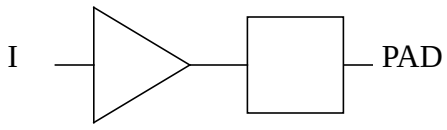
Propagation Delays (ns) for Sample Core Input Transitions: Standard Pad Load = 16 pF

Cell Name	Type Delay	Core Input Transition							
		0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3B21EU	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135
	tOEN	3.648	2.358	3.687	2.400	3.797	2.490	3.956	2.676
	tOD	1.001	1.497	1.042	1.539	1.168	1.654	1.384	1.821
PC3B25EU	tCMOS	2.580	2.173	2.623	2.220	2.745	2.341	2.931	2.526
	tOEN	1.739	1.571	1.778	1.613	1.881	1.706	2.079	1.889
	tOD	3.329	2.268	3.356	2.329	3.495	2.442	3.626	2.711

1.8V CMOS Output Pads

PC3O01 through PC3O05

PC3O01 through PC3O05 cells are CMOS output pads with AC drive capabilities ranging from 1x to 5x.



Function Table

INPUT	OUTPUT
I	PAD
L	L
H	H

Cell Description

Macro Name:	PC3O01	PC3O02	PC3O03	PC3O04	PC3O05
Drive Capability	1x	2x	3x	4x	5x
Leakage Power (pW)	2853.3	1804.1	1873.6	1873.6	1873.6

Pin Description

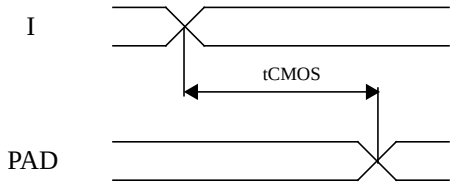
Name	Capacitance (pF)					Description
	PC3O01	PC3O02	PC3O03	PC3O04	PC3O05	
I	0.112	0.178	0.188	0.188	0.175	Input
Maximum capacitance						
PAD	80	80	80	80	80	Output

Pin Powers for:
Standard Pad load = 10.0 pF, Standard Core Input Transition = 0.1 ns

Name	Pin Power (pW/Hz)				
	PC3O01	PC3O02	PC3O03	PC3O04	PC3O05
PAD	21	27.8	29	29.7	30.8

1.8V CMOS Output Pads
PC3O01 through PC3O05

Waveforms



Timing Numbers for PC3O01 through PC3O05:

Propagation Delays (ns) for Sample Pad Loads:
Standard Core Input Transition = 0.1 ns

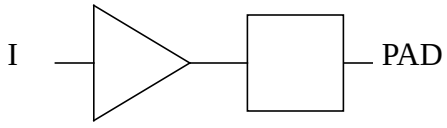
Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3O01	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164
PC3O02	tCMOS	2.295	1.935	3.034	2.395	4.513	3.317	7.456	5.154
PC3O03	tCMOS	2.174	1.961	2.665	2.413	3.646	3.318	5.593	4.739
PC3O04	tCMOS	2.121	1.931	2.494	2.291	3.240	3.011	4.722	4.187
PC3O05	tCMOS	2.141	1.965	2.448	2.270	3.061	2.882	4.253	3.907

Propagation Delays (ns) for Sample Core Input Transitions:
Standard Pad Load = 16 pF

Cell Name	Type Delay	Core Input Transition							
		0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3O01	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135
PC3O02	tCMOS	3.034	2.395	3.081	2.446	3.195	2.562	3.391	2.774
PC3O03	tCMOS	2.665	2.413	2.700	2.460	2.814	2.581	3.019	2.773
PC3O04	tCMOS	2.494	2.291	2.539	2.337	2.664	2.453	2.855	2.653
PC3O05	tCMOS	2.448	2.270	2.485	2.316	2.606	2.434	2.798	2.617

1.8V CMOS Output Pad with High Voltage Input Pin
PC3O01HV

PC3O01HV cell is CMOS output pad with AC drive capabilities ranging 1x. Its input pin I can be connected to the buses which can swing between 0V and 1.95V.



Function Table

INPUT	OUTPUT
I	PAD
L	L
H	H

Cell Description

Macro Name:	PC3O01HV
Drive Capability	1x
Leakage Power (pW)	2853.3

Pin Description

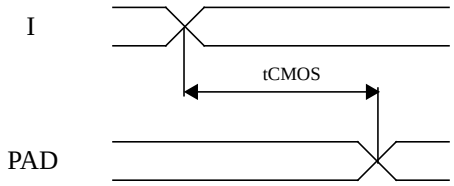
Name	Capacitance (pF)	Description
	PC3O01HV	
I	0.112	Input
Maximum capacitance		
PAD	3.185	Output

Pin Powers for:
Standard Pad load = 10.0 pF, Standard Core Input Transition = 0.1 ns

Name	Pin Power (pW/ Hz)
	PC3O01HV
PAD	21

1.8V CMOS Output Pad with High Voltage Input Pin
PC3O01HV

Waveforms



Timing Numbers for PC3O01HV :

Propagation Delays (ns) for Sample Pad Loads:
Standard Core Input Transition = 0.1 ns

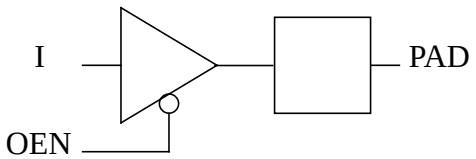
Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3O01HV	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164

Propagation Delays (ns) for Sample Core Input Transitions:
Standard Pad Load = 16 pF

Cell Name	Type Delay	Core Input Transition							
		0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3O01HV	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135

1.8V TTL 3-State Output Pads
PT3T01 through PT3T03

PT3T01 through PT3T03 cells are three state TTL output pads with AC drive capabilities of 2mA, 6mA, 10mA respectively.



Function Table

INPUT		OUTPUT
OEN	I	PAD
H	X	Z
L	L	L
L	H	H

Cell Description

Macro Name:	PT3T01	PT3T02	PT3T03
Drive Capability:	1x	2x	3x
Leakage Power (pW)	2853.3	2855.4	2858.1

Pin Description

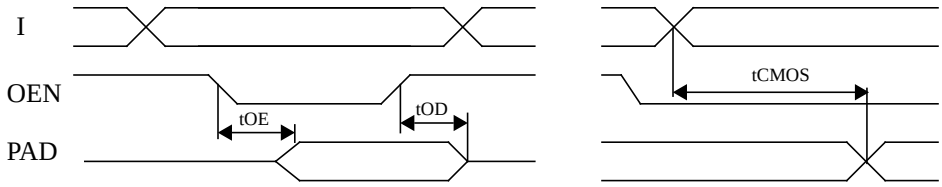
Name	Capacitance (pF)			Description
	PT3T01	PT3T02	PT3T03	
I	0.112	0.195	0.198	Input
OEN	0.11	0.11	0.11	Output Enable
PAD	3.185	3.188	3.188	3-StateOutput

Pin Powers for:
Standard Pad Load = 10.0 pF, Standard Core Input Transition = 0.1 ns

Name	Pin Power (pW/Hz)		
	PT3T01	PT3T02	PT3T03
PAD	21	22.3	23.8

1.8V TTL 3-State Output Pads
PT3T01 through PT3T03

Waveforms



Timing Numbers for PT3T01 through PT3T03:

Propagation Delays (ns) for Sample Pad Loads:
Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3T01	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164
	tOEN	2.196	1.449	3.648	2.358	6.540	4.156	12.313	7.749
	tOD	1.001	1.497	1.001	1.497	1.001	1.497	1.001	1.497
PT3T02	tCMOS	2.120	2.042	2.632	2.560	3.610	3.455	5.548	4.910
	tOEN	1.496	1.385	2.006	1.908	2.984	2.825	4.927	4.309
	tOD	2.498	1.875	2.500	1.875	2.497	1.875	2.495	1.875
PT3T03	tCMOS	2.240	1.784	2.583	2.181	3.200	2.781	4.387	3.827
	tOEN	1.424	1.188	1.763	1.578	2.378	2.193	3.568	3.261
	tOD	3.338	2.265	3.338	2.265	3.349	2.265	3.354	2.265

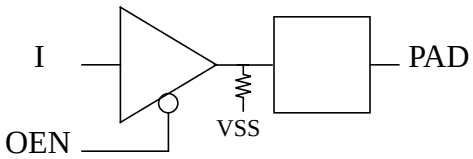
1.8V TTL 3-State Output Pads
PT3T01 through PT3T03

Propagation Delays (ns) for Sample Core Input Transitions: Standard Pad Load = 16 pF

Cell Name	Core Input Transition								
	Type Delay	0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3T01	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135
	tOEN	3.648	2.358	3.687	2.400	3.797	2.490	3.956	2.676
	tOD	1.001	1.497	1.042	1.539	1.168	1.654	1.384	1.821
PT3T02	tCMOS	2.632	2.560	2.680	2.601	2.797	2.712	3.000	2.909
	tOEN	2.006	1.908	2.044	1.950	2.152	2.039	2.335	2.239
	tOD	2.500	1.875	2.549	1.922	2.664	2.062	2.831	2.267
PT3T03	tCMOS	2.583	2.181	2.625	2.229	2.748	2.339	2.948	2.523
	tOEN	1.763	1.578	1.796	1.608	1.905	1.705	2.089	1.890
	tOD	3.338	2.265	3.382	2.333	3.496	2.424	3.598	2.591

1.8V TTL 3-State Output Pads with Pull-down Resistor
PT3T01D through PT3T03D

PT3T01D through PT3T03D cells are three state TTL output pads with pulldown and with AC drive capabilities of 2mA, 6mA, 10mA respectively.



Function Table

INPUT		OUTPUT
OEN	I	PAD
H	X	Lr
L	L	L
L	H	H

Lr = Resistive-Low Drive Strength

Cell Description

Macro Name:	PT3T01D	PT3T02D	PT3T03D
Drive Capability:	1x	2x	3x
Leakage Power (pW)	2853.3	2855.4	2858.1

Pin Description

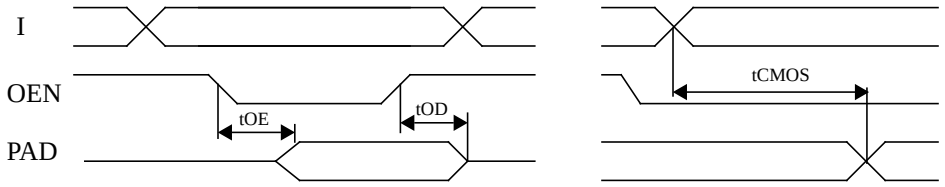
Name	Capacitance (pF)			Description
	PT3T01D	PT3T02D	PT3T03D	
I	0.112	0.19	0.198	Input
OEN	0.11	0.11	0.11	Output Enable
PAD	3.185	3.178	3.18	3-StateOutput

Pin Powers for:
Standard Pad Load = 10.0 pF, Standard Core Input Transition = 0.1 ns

Name	Pin Power (pW/Hz)		
	PT3T01D	PT3T02D	PT3T03D
PAD	21	22.7	24.1

1.8V TTL 3-State Output Pads with Pull-down Resistor
PT3T01D through PT3T03D

Waveforms



Timing Numbers for PT3T01D through PT3T03D:

Propagation Delays (ns) for Sample Pad Loads:
Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3T01D	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164
	tOEN	2.196	1.449	3.648	2.358	6.540	4.156	12.313	7.749
	tOD	1.001	1.497	1.001	1.497	1.001	1.497	1.001	1.497
PT3T02D	tCMOS	2.127	2.039	2.636	2.554	3.614	3.449	5.553	4.906
	tOEN	1.493	1.340	2.008	1.874	2.991	2.795	4.931	4.278
	tOD	2.499	1.875	2.501	1.875	2.501	1.875	2.501	1.875
PT3T03D	tCMOS	2.243	1.777	2.589	2.172	3.206	2.772	4.394	3.822
	tOEN	1.411	1.156	1.750	1.550	2.375	2.172	3.567	3.245
	tOD	3.336	2.282	3.328	2.282	3.341	2.282	3.351	2.279

1.8V TTL 3-State Output Pads with Pull-down Resistor
PT3T01D through PT3T03D

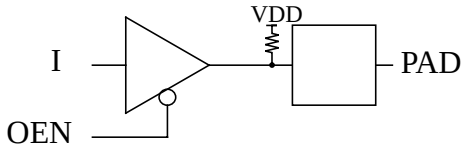
Propagation Delays (ns) for Sample Core Input Transitions: Standard Pad Load = 16 pF

Cell Name	Core Input Transition								
	Type Delay	0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3T01D	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135
	tOEN	3.648	2.358	3.687	2.400	3.797	2.490	3.956	2.676
	tOD	1.001	1.497	1.042	1.539	1.168	1.654	1.384	1.821
PT3T02D	tCMOS	2.636	2.554	2.679	2.600	2.799	2.712	2.999	2.912
	tOEN	2.008	1.874	2.051	1.917	2.158	2.007	2.356	2.193
	tOD	2.501	1.875	2.542	1.922	2.674	2.049	2.843	2.263
PT3T03D	tCMOS	2.589	2.172	2.628	2.220	2.745	2.343	2.931	2.541
	tOEN	1.750	1.550	1.794	1.587	1.909	1.677	2.107	1.861
	tOD	3.328	2.282	3.374	2.342	3.491	2.436	3.606	2.569

1.8V TTL 3-State Output Pads with Pull-up Resistor

PT3T01U through PT3T03U

PT3T01U through PT3T03U cells are three state TTL output pads with pullup and with AC drive capabilities of 2mA, 6mA, 10mA respectively



Function Table

INPUT		OUTPUT
OEN	I	PAD
H	X	Hr
L	L	L
L	H	H

Hr = Resistive-High Drive Strength

Cell Description

Macro Name:	PT3T01U	PT3T02U	PT3T03U
Drive Capability:	1x	2x	3x
Leakage Power (µW)	30.611	30.611	30.611

Pin Description

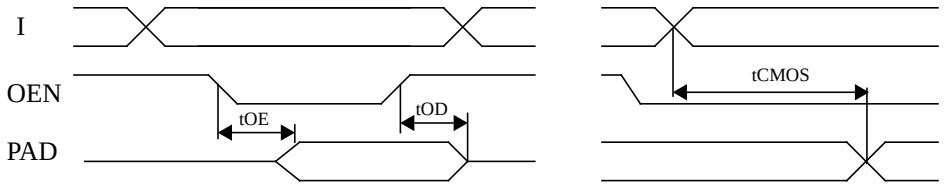
Name	Capacitance (pF)			Description
	PT3T01U	PT3T02U	PT3T03U	
I	0.112	0.195	0.198	Input
OEN	0.11	0.11	0.11	Output Enable
PAD	3.185	3.172	3.172	3-StateOutput

Pin Powers for:
Standard Pad Load = 10.0 pF, Standard Core Input Transition = 0.1 ns

Name	Pin Power (pW/Hz)		
	PT3T01U	PT3T02U	PT3T03U
PAD	21	22.9	24.3

1.8V TTL 3-State Output Pads with Pull-up Resistor
PT3T01U through PT3T03U

Waveforms



Timing Numbers for PT3T01U through PT3T03U:

Propagation Delays (ns) for Sample Pad Loads:
Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3T01U	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164
	tOEN	2.196	1.449	3.648	2.358	6.540	4.156	12.313	7.749
	tOD	1.001	1.497	1.001	1.497	1.001	1.497	1.001	1.497
PT3T02U	tCMOS	2.121	2.045	2.627	2.561	3.609	3.456	5.544	4.911
	tOEN	1.467	1.389	1.982	1.912	2.957	2.825	4.895	4.308
	tOD	2.501	1.881	2.501	1.881	2.501	1.881	2.501	1.881
PT3T03U	tCMOS	2.242	1.785	2.580	2.182	3.199	2.782	4.388	3.828
	tOEN	1.398	1.190	1.741	1.578	2.360	2.193	3.550	3.258
	tOD	3.336	2.275	3.337	2.275	3.345	2.275	3.348	2.279

1.8V TTL 3-State Output Pads with Pull-up Resistor
PT3T01U through PT3T03U

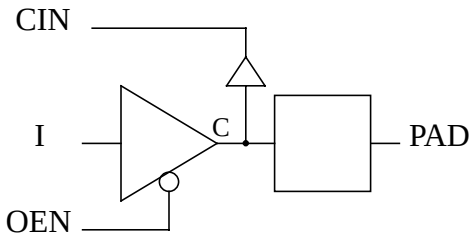
Propagation Delays (ns) for Sample Core Input Transitions: Standard Pad Load = 16 pF

Cell Name	Core Input Transition								
	Type Delay	0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3T01U	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135
	tOEN	3.648	2.358	3.687	2.400	3.797	2.490	3.956	2.676
	tOD	1.001	1.497	1.042	1.539	1.168	1.654	1.384	1.821
PT3T02U	tCMOS	2.627	2.561	2.674	2.609	2.798	2.713	2.998	2.913
	tOEN	1.982	1.912	2.021	1.948	2.124	2.045	2.305	2.228
	tOD	2.501	1.881	2.547	1.936	2.664	2.062	2.831	2.267
PT3T03U	tCMOS	2.580	2.182	2.623	2.230	2.745	2.340	2.931	2.523
	tOEN	1.741	1.578	1.775	1.609	1.886	1.705	2.069	1.891
	tOD	3.337	2.275	3.381	2.342	3.457	2.424	3.671	2.591

1.8V TTL 3-State I/O Pads

PT3B01 through PT3B03

PT3B01 through PT3B03 cells are three state TTL input/output pads with AC drive capabilities of 2mA, 6mA, 10mA respectively.



Function Table

INPUT		OUTPUTS	
OEN	I	PAD	CIN
H	X	Zl	L
H	X	Zh	H
L	L	L	L
L	H	H	H

Cell Description

Macro Name:	PT3B01	PT3B02	PT3B03
Drive Capability	1x	2x	3x
Leakage Power (pW):	2853.3	3118.4	3121.1

Pin Description

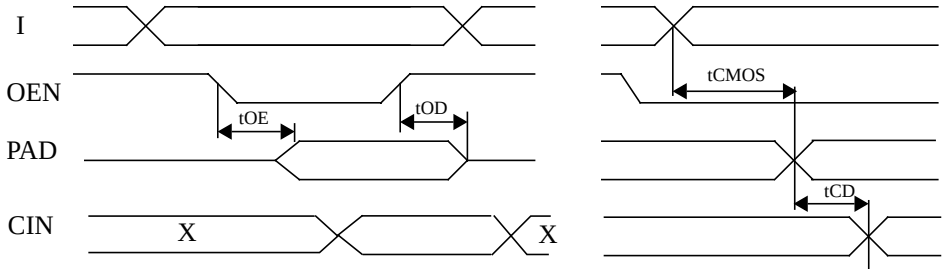
Name	Capacitance (pF)			Description
	PT3B01	PT3B02	PT3B03	
I	0.112	0.18	0.18	Input
OEN	0.11	0.11	0.11	Output Enable
PAD	3.185	3.188	3.188	3-StateOutput
Maximum capacitance				
CIN	0.8	0.8	0.8	Output

Pin Powers for:
Standard Pad Load = 10.0 pF, Standard Core Input Transition = 0.1 ns
Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns

Name	Pin Power (pW/Hz)		
	PT3B01	PT3B02	PT3B03
PAD	21	22.4	23.9
CIN	5.6	5.6	5.4

1.8V TTL 3-State I/O Pads
PT3B01 through PT3B03

Waveforms



Timing Numbers for PT3B01 through PT3B03:

Propagation Delays tCD (ns) for Sample Core Loads: Standard Pad Input Transition = 1 ns, Core Load Unit = 0.01 pF

Cell Name	Core Load Fanout									
	2		4		8		16		32	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3B01	0.553	0.897	0.565	0.913	0.590	0.947	0.632	1.012	0.715	1.142
PT3B02	0.541	0.880	0.553	0.899	0.578	0.935	0.621	1.000	0.706	1.130
PT3B03	0.541	0.880	0.553	0.899	0.578	0.935	0.621	1.000	0.706	1.130

Propagation Delays tCD (ns) for Sample Pad Input Transitions: Standard Core Load = 0.16 pF

Cell Name	Pad Input Transition									
	1 ns		2 ns		5 ns		10 ns		15 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3B01	0.632	1.012	0.778	1.245	0.979	1.736	1.163	2.355	1.346	2.974
PT3B02	0.621	1.000	0.763	1.225	0.960	1.717	1.135	2.338	1.310	2.958
PT3B03	0.621	1.000	0.763	1.225	0.960	1.717	1.135	2.338	1.310	2.958

1.8V TTL 3-State I/O Pads
PT3B01 through PT3B03

Propagation Delays (ns) for Sample Pad Loads: Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3B01	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164
	tOEN	2.196	1.449	3.648	2.358	6.540	4.156	12.313	7.749
	tOD	1.001	1.497	1.001	1.497	1.001	1.497	1.001	1.497
PT3B02	tCMOS	2.127	2.044	2.635	2.559	3.612	3.451	5.555	4.910
	tOEN	1.493	1.377	2.005	1.902	2.980	2.818	4.923	4.306
	tOD	2.501	1.887	2.501	1.887	2.503	1.887	2.505	1.887
PT3B03	tCMOS	2.240	1.780	2.583	2.176	3.200	2.781	4.394	3.829
	tOEN	1.416	1.180	1.755	1.570	2.375	2.192	3.563	3.263
	tOD	3.315	2.268	3.314	2.268	3.317	2.268	3.339	2.268

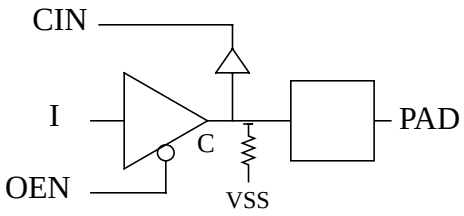
Propagation Delays (ns) for Sample Core Input Transitions: Standard Pad Load = 16 pF

Cell Name	Type Delay	Core Input Transition							
		0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3B01	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135
	tOEN	3.648	2.358	3.687	2.400	3.797	2.490	3.956	2.676
	tOD	1.001	1.497	1.042	1.539	1.168	1.654	1.384	1.821
PT3B02	tCMOS	2.635	2.559	2.676	2.601	2.797	2.712	3.000	2.909
	tOEN	2.005	1.902	2.050	1.943	2.153	2.044	2.334	2.227
	tOD	2.501	1.887	2.549	1.922	2.673	2.035	2.873	2.204
PT3B03	tCMOS	2.583	2.176	2.625	2.223	2.745	2.344	2.929	2.544
	tOEN	1.755	1.570	1.794	1.612	1.905	1.705	2.089	1.890
	tOD	3.314	2.268	3.354	2.314	3.505	2.442	3.641	2.711

1.8V TTL 3-State I/O Pads with Pull-down Resistor

PT3B01D through PT3B03D

PT3B01D through PT3B03D cells are three state TTL input/output pads with pull-down and with AC drive capabilities of 2mA, 6mA, 10mA respectively.



Function Table

INPUT		OUTPUTS	
OEN	I	PAD	CIN
H	X	Lr	L
L	L	L	L
L	H	H	H

Lr = Resistive-Low Drive Strength

Cell Description

Macro Name:	PT3B01D	PT3B02D	PT3B03D
Drive Capability	1x	2x	3x
Leakage Power (pW):	2853.3	3118.4	3121.1

Pin Description

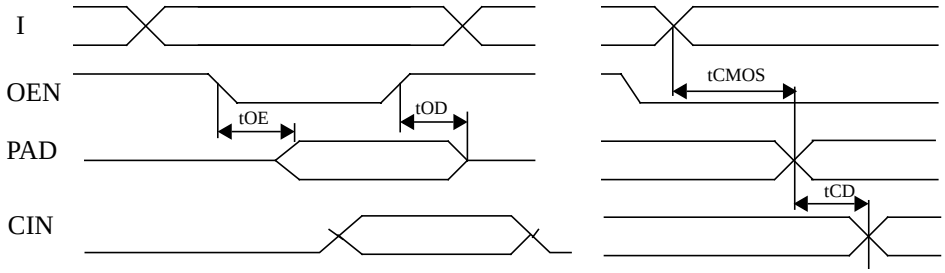
Name	Capacitance (pF)			Description
	PT3B01D	PT3B02D	PT3B03D	
I	0.112	0.18	0.18	Input
OEN	0.11	0.11	0.11	Output Enable
PAD	3.185	3.178	3.18	3-StateOutput
Maximum capacitance				
CIN	0.8	0.8	0.8	Output

Pin Powers for:
Standard Pad Load = 10.0 pF, Standard Core Input Transition = 0.1 ns
Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns

Name	Pin Power (pW/Hz)		
	PT3B01D	PT3B02D	PT3B03D
PAD	21	22.8	24.2
CIN	5.6	5.5	5.5

1.8V TTL 3-State I/O Pads with Pull-down Resistor
PT3B01D through PT3B03D

Waveforms



Timing Numbers for PT3B01D through PT3B03D:

Propagation Delays tCD (ns) for Sample Core Loads:
Standard Pad Input Transition = 1 ns, Core Load Unit = 0.01 pF

Cell Name	Core Load Fanout									
	2		4		8		16		32	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3B01D	0.553	0.897	0.565	0.913	0.590	0.947	0.632	1.012	0.715	1.142
PT3B02D	0.553	0.890	0.565	0.908	0.590	0.943	0.630	1.008	0.710	1.138
PT3B03D	0.553	0.890	0.565	0.908	0.590	0.943	0.630	1.010	0.710	1.145

Propagation Delays tCD (ns) for Sample Pad Input Transitions:
Standard Core Load = 0.16 pF

Cell Name	Pad Input Transition									
	1 ns		2 ns		5 ns		10 ns		15 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3B01D	0.632	1.012	0.778	1.245	0.979	1.736	1.163	2.355	1.346	2.974
PT3B02D	0.630	1.008	0.780	1.225	0.995	1.710	1.195	2.308	1.395	2.905
PT3B03D	0.630	1.010	0.780	1.225	0.995	1.707	1.195	2.293	1.395	2.878

1.8V TTL 3-State I/O Pads with Pull-down Resistor
PT3B01D through PT3B03D

Propagation Delays (ns) for Sample Pad Loads: Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3B01D	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164
	tOEN	2.196	1.449	3.648	2.358	6.540	4.156	12.313	7.749
	tOD	1.001	1.497	1.001	1.497	1.001	1.497	1.001	1.497
PT3B02D	tCMOS	2.127	2.039	2.636	2.553	3.616	3.445	5.559	4.902
	tOEN	1.500	1.338	2.013	1.873	2.989	2.789	4.928	4.273
	tOD	2.503	1.881	2.503	1.882	2.510	1.885	2.515	1.887
PT3B03D	tCMOS	2.243	1.784	2.585	2.181	3.206	2.778	4.396	3.824
	tOEN	1.416	1.153	1.756	1.545	2.377	2.170	3.567	3.250
	tOD	3.306	2.262	3.298	2.262	3.309	2.262	3.316	2.259

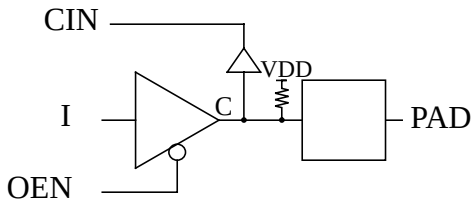
Propagation Delays (ns) for Sample Core Input Transitions: Standard Pad Load = 16 pF

Cell Name	Type Delay	Core Input Transition							
		0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3B01D	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135
	tOEN	3.648	2.358	3.687	2.400	3.797	2.490	3.956	2.676
	tOD	1.001	1.497	1.042	1.539	1.168	1.654	1.384	1.821
PT3B02D	tCMOS	2.636	2.553	2.683	2.600	2.799	2.712	2.999	2.915
	tOEN	2.013	1.873	2.053	1.916	2.163	2.012	2.346	2.204
	tOD	2.503	1.882	2.557	1.914	2.673	2.034	2.873	2.201
PT3B03D	tCMOS	2.585	2.181	2.626	2.222	2.749	2.339	2.947	2.520
	tOEN	1.756	1.545	1.801	1.587	1.909	1.677	2.107	1.861
	tOD	3.298	2.262	3.373	2.307	3.496	2.422	3.626	2.615

1.8V TTL 3-State I/O Pads with Pull-up Resistor

PT3B01U through PT3B03U

PT3B01U through PT3B03U cells are three state TTL input/output pads with pullup and with AC drive capabilities of 2mA, 6mA, 10mA respectively.



Function Table

INPUT		OUTPUTS	
OEN	I	PAD	CIN
H	X	Hr	H
L	L	L	L
L	H	H	H

Hr = Resistive-High Drive Strength

Cell Description

Macro Name:	PT3B01U	PT3B02U	PT3B03U
Drive Capability	1x	2x	3x
Leakage Power (µW):	30.611	30.611	30.611

Pin Description

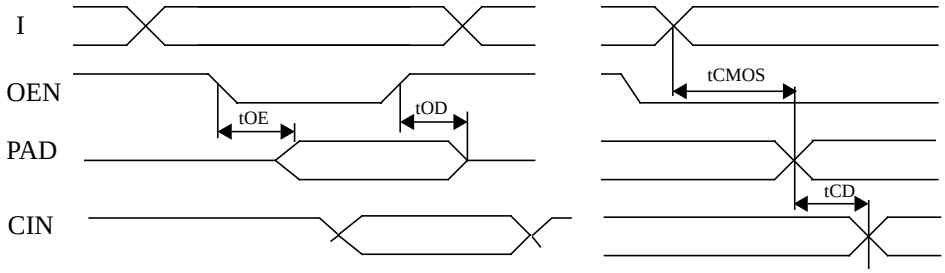
Name	Capacitance (pF)			Description
	PT3B01U	PT3B02U	PT3B03U	
I	0.112	0.18	0.18	Input
OEN	0.11	0.11	0.11	Output Enable
PAD	3.185	3.172	3.172	3-StateOutput
Maximum capacitance				
CIN	0.8	0.8	0.8	Output

Pin Powers for:
Standard Pad Load = 10.0 pF, Standard Core Input Transition = 0.1
Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns

Name	Pin Power (pW/Hz)		
	PT3B01U	PT3B02U	PT3B03U
PAD	21	22.9	24.3
CIN	5.6	5.6	5.6

1.8V TTL 3-State I/O Pads with Pull-up Resistor
PT3B01U through PT3B03U

Waveforms



Timing Numbers for PT3B01U through PT3B03U:

Propagation Delays tCD (ns) for Sample Core Loads:
Standard Pad Input Transition = 1 ns, Core Load Unit = 0.01 pF

Cell Name	Core Load Fanout									
	2		4		8		16		32	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3B01U	0.553	0.897	0.565	0.913	0.590	0.947	0.632	1.012	0.715	1.142
PT3B02U	0.541	0.883	0.553	0.903	0.578	0.945	0.621	1.010	0.706	1.140
PT3B03U	0.541	0.890	0.553	0.905	0.578	0.937	0.621	1.002	0.706	1.132

Propagation Delays tCD (ns) for Sample Pad Input Transitions:
Standard Core Load = 0.16 pF

Cell Name	Pad Input Transition									
	1 ns		2 ns		5 ns		10 ns		15 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3B01U	0.632	1.012	0.778	1.245	0.979	1.736	1.163	2.355	1.346	2.974
PT3B02U	0.621	1.010	0.763	1.235	0.937	1.744	1.095	2.378	1.253	3.011
PT3B03U	0.621	1.002	0.763	1.235	0.937	1.746	1.095	2.390	1.253	3.034

1.8V TTL 3-State I/O Pads with Pull-up Resistor
PT3B01U through PT3B03U

Propagation Delays (ns) for Sample Pad Loads: Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3B01U	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164
	tOEN	2.196	1.449	3.648	2.358	6.540	4.156	12.313	7.749
	tOD	1.001	1.497	1.001	1.497	1.001	1.497	1.001	1.497
PT3B02U	tCMOS	2.123	2.045	2.632	2.560	3.609	3.452	5.549	4.911
	tOEN	1.464	1.382	1.976	1.909	2.951	2.824	4.897	4.300
	tOD	2.498	1.881	2.495	1.881	2.497	1.881	2.498	1.881
PT3B03U	tCMOS	2.240	1.778	2.580	2.173	3.199	2.776	4.388	3.822
	tOEN	1.393	1.184	1.739	1.571	2.359	2.194	3.547	3.266
	tOD	3.312	2.268	3.329	2.268	3.342	2.268	3.351	2.268

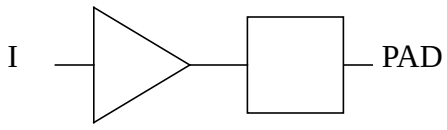
Propagation Delays (ns) for Sample Core Input Transitions: Standard Pad Load = 16 pF

Cell Name	Type Delay	Core Input Transition							
		0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3B01U	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135
	tOEN	3.648	2.358	3.687	2.400	3.797	2.490	3.956	2.676
	tOD	1.001	1.497	1.042	1.539	1.168	1.654	1.384	1.821
PT3B02U	tCMOS	2.632	2.560	2.674	2.602	2.789	2.713	2.989	2.910
	tOEN	1.976	1.909	2.021	1.944	2.129	2.041	2.295	2.236
	tOD	2.495	1.881	2.557	1.929	2.663	2.039	2.863	2.222
PT3B03U	tCMOS	2.580	2.173	2.623	2.220	2.745	2.341	2.931	2.526
	tOEN	1.739	1.571	1.778	1.613	1.881	1.706	2.079	1.889
	tOD	3.329	2.268	3.356	2.329	3.495	2.442	3.626	2.711

1.8V TTL Output Pads

PT3O01 through PT3O03

PT3O01 through PT3O03 cells are TTL output pads with AC drive capabilities of 2mA, 6mA, 10mA respectively.



Function Table

INPUT	OUTPUT
I	PAD
L	L
H	H

Cell Description

Macro Name:	PT3O01	PT3O02	PT3O03
Drive Capability	1x	2x	3x
Leakage Power (pW)	2853.3	1873.6	1873.6

Pin Description

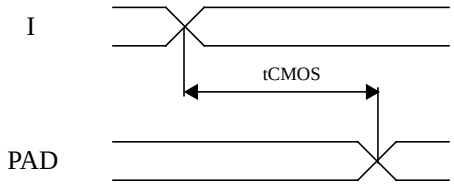
Name	Capacitance (pF)			Description
	PT3O01	PT3O02	PT3O03	
I	0.112	0.188	0.175	Input
Maximum capacitance				
PAD	80	80	80	Output

Pin Powers for:
Standard Pad load = 10.0 pF, Standard Core Input Transition = 0.1 ns

Name	Pin Power (pW/Hz)		
	PT3O01	PT3O02	PT3O03
PAD	21	29	30.8

1.8V TTL Output Pads
PT3O01 through PT3O03

Waveforms



Timing Numbers for PT3O01 through PT3O03:

Propagation Delays (ns) for Sample Pad Loads:
Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3O01	tCMOS	2.799	1.858	4.250	2.773	7.138	4.573	12.923	8.164
PT3O02	tCMOS	2.174	1.961	2.665	2.413	3.646	3.318	5.593	4.739
PT3O03	tCMOS	2.141	1.965	2.448	2.270	3.061	2.882	4.253	3.907

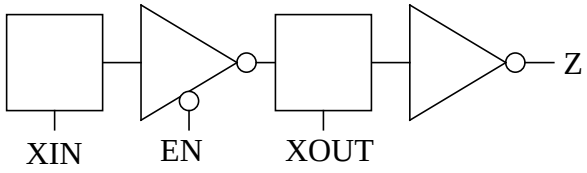
Propagation Delays (ns) for Sample Core Input Transitions:
Standard Pad Load = 16 pF

Cell Name	Type Delay	Core Input Transition							
		0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PT3O01	tCMOS	4.250	2.773	4.285	2.821	4.404	2.935	4.606	3.135
PT3O02	tCMOS	2.665	2.413	2.700	2.460	2.814	2.581	3.019	2.773
PT3O03	tCMOS	2.448	2.270	2.485	2.316	2.606	2.434	2.798	2.617

1.8V Crystal Oscillator Pads

PC3X11, PC3X12 and PC3X13

PC3X11, PC3X12 and PC3X13 are crystal oscillator macros with low, medium and high frequency capabilities. The crystal connects across the XIN and XOUT pads. When this macros is placed, the input pad appears at one die pad number higher than the output pad. Z is the buffered clock input to the chip's core. In his regular behaviour, the PC3X11 generate between XIN and XOUT a sinusoidal oscillation. The pins XIN and XOUT of the cells PC3X11, PC3X12 and PC3X13 are only 1.8V (VDD core, 1.62 v up to 1.98 v) tolerant.



Function Table

INPUTS		OUTPUTS	
EN	XIN	XOUT	Z
1	x	z	1
0	1	0	1
0	0	1	0

Cell Description

Macro Name:	PC3X11	PC3X12	PC3X13
Drive Capability	1x	2x	3x
Leakage Power (pW)	2853.3	6408.0	3379.9

Pin Description

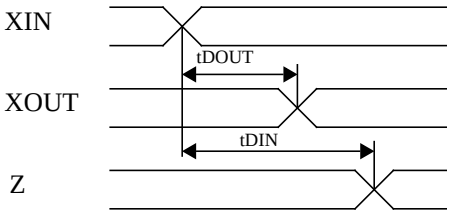
Name	Capacitance (pF)			Description
	PC3X11	PC3X12	PC3X13	
EN	0.135	0.16	0.16	Data Input
XIN	3.642	3.15	3.235	Data Input
XOUT	3.462	3.305	3.388	Data Output
Maximum capacitance				
Z	0.8	0.8	0.8	Data Output

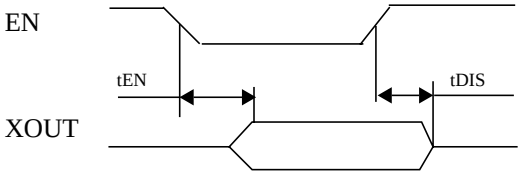
1.8V Crystal Oscillator Pads
PC3X11, PC3X12 and PC3X13

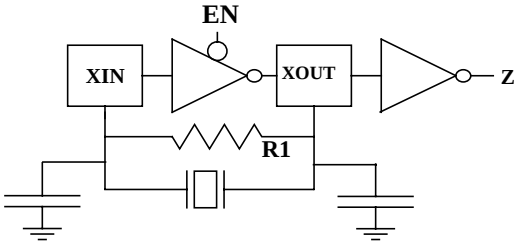
Pin Powers for:
Standard Pad Load = 10.0 pF, Standard Core Input Transition = 0.1 ns
Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns

Name	Pin Power (pW/Hz)		
	PC3X11	PC3X12	PC3X13
XOUT	20.9	19.2	18.8
Z	5.7	6	5

Waveforms







1.8V Crystal Oscillator Pads
PC3X11, PC3X12 and PC3X13

Timing Numbers for PC3X11 through PC3X13:

Propagation Delays XIN -> Z (ns) for Sample Core Loads:
Standard Pad Input Transition = 1 ns, Core Load Unit = 0.01 pF

Cell Name	Core Load Fanout									
	2		4		8		16		32	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3X11	1.662	3.031	1.665	3.037	1.672	3.048	1.687	3.064	1.718	3.095
PC3X12	1.816	1.953	1.823	1.959	1.837	1.972	1.852	1.987	1.882	2.017
PC3X13	1.898	1.937	1.907	1.940	1.923	1.947	1.939	1.964	1.970	1.998

Propagation Delays XIN -> Z (ns) for Sample Pad Input Transitions:
Standard Core Load = 0.16 pF

Cell Name	Pad Input Transition									
	1 ns		2 ns		5 ns		10 ns		15 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3X11	1.687	3.064	1.848	3.208	2.272	3.836	2.795	4.893	3.318	5.949
PC3X12	1.852	1.987	1.985	2.145	2.394	2.625	2.925	3.275	3.456	3.925
PC3X13	1.939	1.964	2.058	2.095	2.430	2.518	2.908	3.085	3.385	3.652

Propagation Delays to XOUT (ns) for Sample Pad Loads:
Standard Core Input Transition = 0.1 ns

Cell Name	Type Delay	Pad Load							
		8 pF		16 pF		32 pF		64 pF	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3X11	tDOUT	4.478	1.555	8.340	2.803	15.985	5.278	31.269	10.209
	tEN	4.377	1.438	8.235	2.675	15.887	5.147	31.169	10.080
	tDIS	0.161	0.527	0.161	0.527	0.161	0.527	0.161	0.527
PC3X12	tDOUT	2.122	1.707	3.365	2.603	5.770	4.318	10.548	7.728
	tEN	2.000	1.244	3.223	2.120	5.620	3.833	10.394	7.242
	tDIS	0.224	0.667	0.227	0.667	0.227	0.667	0.227	0.667
PC3X13	tDOUT	1.932	1.711	2.764	2.361	4.309	3.551	7.336	5.867
	tEN	1.787	1.055	2.600	1.674	4.136	2.842	7.147	5.137
	tDIS	0.257	0.844	0.257	0.844	0.257	0.844	0.257	0.844

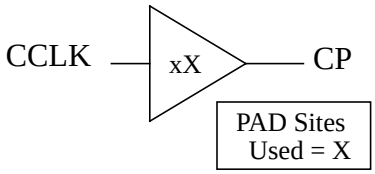
1.8V Crystal Oscillator Pads
PC3X11, PC3X12 and PC3X13

Propagation Delays to XOUT (ns) for Sample Core Input Transitions: Standard Pad Load = 16 pF

Cell Name	Type Delay	Core Input Transition							
		0.1 ns		0.5 ns		2 ns		5 ns	
		RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3X11	tDOUT	8.340	2.803	8.357	2.820	8.480	2.999	8.960	3.509
	tEN	8.235	2.675	8.312	2.733	8.524	2.958	8.876	3.325
	tDIS	0.161	0.527	0.209	0.583	0.321	0.714	0.438	0.881
PC3X12	tDOUT	3.365	2.603	3.355	2.597	3.520	2.715	4.026	3.198
	tEN	3.223	2.120	3.290	2.182	3.532	2.432	3.934	2.846
	tDIS	0.227	0.667	0.283	0.723	0.419	0.906	0.602	1.189
PC3X13	tDOUT	2.764	2.361	2.748	2.329	2.871	2.441	3.360	2.892
	tEN	2.600	1.674	2.662	1.730	2.910	1.997	3.358	2.444
	tDIS	0.257	0.844	0.321	0.900	0.498	1.114	0.714	1.431

1.8V CMOS Non-Inverting Clock Buffer Pad
PC3C01 through PC3C04

PC3C01 cell is non-inverting clock buffer. The current usage of this pad is the clock tree buffering. This pad is powered with the core power supply. However, PC3D00 cell can be used to provide an off-chip input signal to this cell.



Function Table

INPUT	OUTPUT
CCLK	CP
L	L
H	H

Cell Description

Macro Name:	PC3C01	PC3C02	PC3C03	PC3C04
Drive Capability	1x	2x	3x	4x
Leakage Power (pW):	2853.3	13347.3	26694.5	53389.1

Pin Description

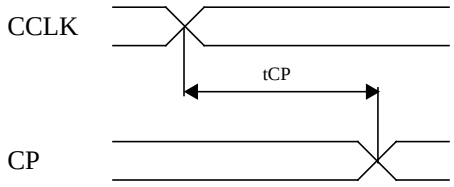
Name	Capacitance (pF)				Description
	PC3C01	PC3C02	PC3C03	PC3C04	
CCLK	0.152	0.32	0.598	1.172	Input
Maximum capacitance					
CP	3.185	88.125	176.25	352.5	Output

Pin Powers for:
Standard Core Load = 32 pF, Standard Core Input Transition = 0.1 ns

Name	Pin Power (pW/Hz)			
	PC3C01	PC3C02	PC3C03	PC3C04
CP	66.4	82.3	120.1	204.9

1.8V CMOS Non-Inverting Clock Buffer Pad
PC3C01 through PC3C04

Waveforms



Timing Numbers for PC3C01 through PC3C04:

Propagation Delays tCP (ns) for Sample Core Output Loads: Standard Core Input Transition = 0.1 ns

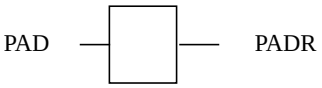
Cell Name	Core Load									
	8 pF		16 pF		32 pF		64 pF		96 pF	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3C01	0.445	0.500	0.679	0.724	1.153	1.168	2.104	2.051	3.054	2.934
PC3C02	0.325	0.384	0.444	0.498	0.680	0.721	1.152	1.166	1.624	1.611
PC3C03	0.259	0.316	0.325	0.384	0.444	0.498	0.680	0.721	0.916	0.943
PC3C04	0.226	0.282	0.259	0.316	0.325	0.384	0.444	0.498	0.562	0.609

Propagation Delays tCP (ns) for Sample Core Input Transitions: Standard Core Load = 32 pF

Cell Name	Core Input Transition									
	0.1 ns		0.5 ns		1 ns		3 ns		5 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3C01	1.153	1.168	1.256	1.267	1.368	1.392	1.686	1.742	1.992	2.076
PC3C02	0.680	0.721	0.777	0.825	0.895	0.946	1.212	1.302	1.512	1.647
PC3C03	0.444	0.498	0.541	0.602	0.659	0.723	0.976	1.080	1.276	1.424
PC3C04	0.325	0.384	0.422	0.488	0.540	0.610	0.855	0.964	1.154	1.306

1.8V Analog IO Pad
PC3D00

PC3D00 cell is a direct input/output pad, without buffer, suitable for bringing analog signals or reference voltages onto the chip. The current function of this pad is to provide to the core an external chip signal without any gain. In this usage it is mandatory not apply to this pad greater voltage than allowed by the core cell connected to this pad.



Function Table

INPUT	OUTPUT
PAD	PADR
L	L
H	H

Cell Description

Macro Name:	PC3D00
Leakage Power (pW)	2853.3

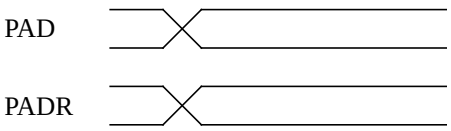
Pin Description

Name	Capacitance (pF)	Description
	PC3D00	
PAD	3.185	Input
PADR	3.185	Output

Pin Powers for:
Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns

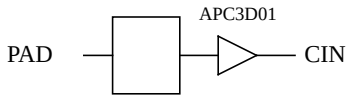
Name	Pin Power (pW/Hz)
	PC3D00
PADR	0
PAD	0

Waveforms



1.8V CMOS Input Only Pad Supplied by Analog Power
APC3D01

APC3D01 cell is input pad supplied by analog power. APC3D01 is CMOS non inverting.



Function Table

INPUT	OUTPUT
PAD	CIN
L	L
H	H

Cell Description

Macro Name:	APC3D01
Leakage Power (pW)	2853.3

Pin Description

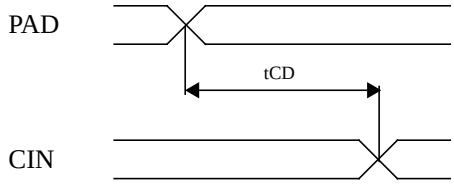
Name	Capacitance (pF)	Description
	APC3D01	
PAD	3.185	Input
Maximum capacitance		
CIN	0.8	Output

Pin Powers for:
Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns

Name	Pin Power (pW/Hz)	Description
	APC3D01	
CIN	5.6	Output

1.8V CMOS Input Only Pad Supplied by Analog Power
APC3D01

Waveforms



Timing Numbers for APC3D01:

Propagation Delays tCD (ns) for Sample Core Loads:
Standard Pad Input Transition = 1 ns, Core Load Unit = 0.01 pF

Cell Name	Core Load Fanout									
	2		4		8		16		32	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
APC3D01	0.553	0.897	0.565	0.913	0.590	0.947	0.632	1.012	0.715	1.142

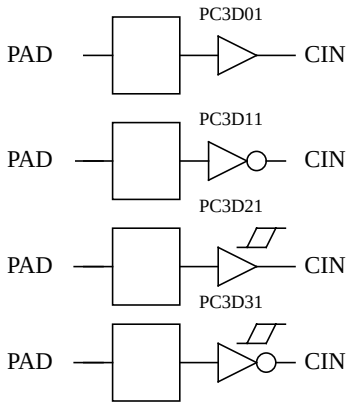
Propagation Delays tCD (ns) for Sample Pad Input Transitions:
Standard Core Load = 0.16 pF

Cell Name	Pad Input Transition									
	1 ns		2 ns		5 ns		10 ns		15 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
APC3D01	0.632	1.012	0.778	1.245	0.979	1.736	1.163	2.355	1.346	2.974

1.8V CMOS Input Only Pads

PC3D01, PC3D11, PC3D21 and PC3D31

PC3D01, PC3D11, PC3D21 and PC3D31 cells are inputs pads. PC3D01 is CMOS non inverting, PC3D11 is CMOS inverting, PC3D21 is CMOS Schmitt non inverting, and PC3D31 is a CMOS Schmitt inverting input pad.



Function Table

INPUT	OUTPUT
PAD	CIN
L	L
H	H

Function Table for PC3D11 & PC3D31

INPUT	OUTPUT
PAD	CIN
L	H
H	L

Cell Description

Macro Name:	PC3D01	PC3D11	PC3D21	PC3D31
Leakage Power (pW)	2853.3	1410.7	1652.9	1588.2

Pin Description

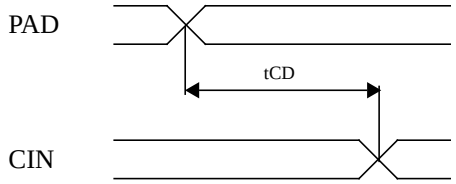
Name	Capacitance (pF)				Description
	PC3D01	PC3D11	PC3D21	PC3D31	
PAD	3.185	3.158	3.148	3.148	Input
Maximum capacitance					
CIN	0.8	0.8	0.8	0.8	Output

Pin Powers for:
Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns

Name	Pin Power (pW/Hz)				Description
	PC3D01	PC3D11	PC3D21	PC3D31	
CIN	5.6	5.7	5.3	5.8	Output

1.8V CMOS Input Only Pads
PC3D01, PC3D11, PC3D21 and PC3D31

Waveforms



Timing Numbers for PC3D01, PC3D11, PC3D21 and PC3D31:

Propagation Delays tCD (ns) for Sample Core Loads:
Standard Pad Input Transition = 1 ns, Core Load Unit = 0.01 pF

Cell Name	Core Load Fanout									
	2		4		8		16		32	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3D01	0.553	0.897	0.565	0.913	0.590	0.947	0.632	1.012	0.715	1.142
PC3D11	0.960	0.735	0.970	0.754	0.988	0.792	1.028	0.850	1.108	0.965
PC3D21	0.711	1.373	0.724	1.405	0.750	1.468	0.790	1.569	0.870	1.770
PC3D31	1.399	1.015	1.409	1.039	1.428	1.088	1.464	1.176	1.536	1.352

Propagation Delays tCD (ns) for Sample Pad Input Transitions:
Standard Core Load = 0.16 pF

Cell Name	Pad Input Transition									
	1 ns		2 ns		5 ns		10 ns		15 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3D01	0.632	1.012	0.778	1.245	0.979	1.736	1.163	2.355	1.346	2.974
PC3D11	1.028	0.850	1.270	1.010	1.790	1.232	2.440	1.440	3.090	1.648
PC3D21	0.790	1.569	1.040	1.863	1.570	2.783	2.305	4.183	3.040	5.583
PC3D31	1.464	1.176	1.760	1.420	2.669	1.989	4.138	2.773	5.606	3.556

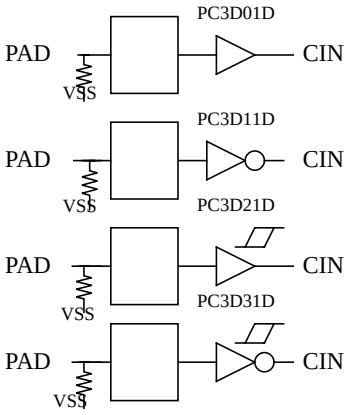
1.8V CMOS Input Only Pads
PC3D01, PC3D11, PC3D21 and PC3D31

Schmitt Trigger Input Thresholds for 1.8V Process Option

Cell Name	VT+			VT-			Hysteresis		
	Min.	Max.	Typical	Min.	Max.	Typical	Min.	Max.	Typical
PC3D21	0.9401V	1.1460V	1.0425V	0.4866V	0.6933V	0.5886V	0.3862V	0.4995V	0.4537V
PC3D31	0.9431V	1.1493V	1.0792V	0.4877V	0.6916V	0.5877V	0.3863V	0.4997V	0.4539V

1.8V CMOS Input Only Pads with Pull-down Resistor
PC3D01D, PC3D11D, PC3D21D and PC3D31D

PC3D01D, PC3D11D, PC3D21D and PC3D31D cells are inputs pads with pull-down. PC3D01D is CMOS non inverting, PC3D11D is CMOS inverting, PC3D21D is CMOS Schmitt non inverting, and PC3D31D is a CMOS Schmitt inverting input pads.



Function Table

INPUT		OUTPUT
PAD(n-1)	PAD(n)	CIN
L	L	L
H	H	H
X	Lr	L
r = resistive drive strength		

Function Table

INPUT		OUTPUT
PAD(n-1)	PAD(n)	CIN
L	L	H
H	H	L
X	Lr	H
r = resistive drive strength		

Cell Description

Macro Name:	PC3D01D	PC3D11D	PC3D21D	PC3D31D
Leakage Power (pW)	2853.3	1410.7	1652.9	1588.2

Pin Description

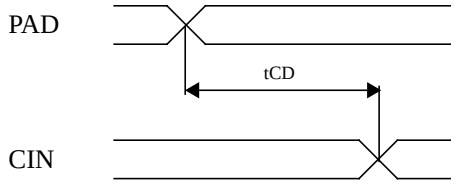
Name	Capacitance (pF)				Description
	PC3D01D	PC3D11D	PC3D21D	PC3D31D	
PAD	3.185	3.148	3.138	3.14	Input
Maximum capacitance					
CIN	0.8	0.8	0.8	0.8	Output

Pin Powers for:
Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns

Name	Pin Power (pW/Hz)				Description
	PC3D01D	PC3D11D	PC3D21D	PC3D31D	
CIN	5.6	5.9	5.3	5.9	Output

1.8V CMOS Input Only Pads with Pull-down Resistor
PC3D01D, PC3D11D, PC3D21D and PC3D31D

Waveforms



Timing Numbers for PC3D01D, PC3D11D, PC3D21D and PC3D31D:

Propagation Delays tCD (ns) for Sample Core Loads:
Standard Pad Input Transition = 1 ns, Core Load Unit = 0.01 pF

Cell Name	Core Load Fanout									
	2		4		8		16		32	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3D01D	0.553	0.897	0.565	0.913	0.590	0.947	0.632	1.012	0.715	1.142
PC3D11D	0.971	0.755	0.983	0.770	1.007	0.802	1.047	0.862	1.127	0.982
PC3D21D	0.723	1.396	0.735	1.427	0.760	1.488	0.802	1.588	0.886	1.788
PC3D31D	1.420	1.024	1.430	1.047	1.448	1.092	1.483	1.183	1.553	1.367

Propagation Delays tCD (ns) for Sample Pad Input Transitions:
Standard Core Load = 0.16 pF

Cell Name	Pad Input Transition									
	1 ns		2 ns		5 ns		10 ns		15 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3D01D	0.632	1.012	0.778	1.245	0.979	1.736	1.163	2.355	1.346	2.974
PC3D11D	1.047	0.862	1.280	1.020	1.779	1.258	2.410	1.498	3.041	1.737
PC3D21D	0.802	1.588	1.050	1.880	1.595	2.774	2.318	4.130	3.040	5.486
PC3D31D	1.483	1.183	1.775	1.438	2.688	2.013	4.090	2.790	5.492	3.567

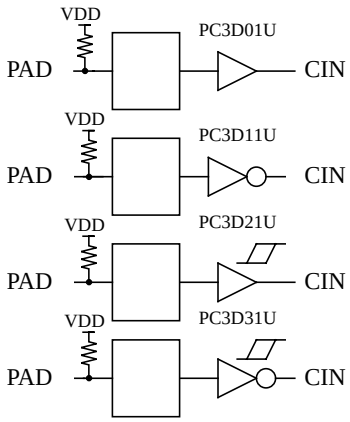
1.8V CMOS Input Only Pads with Pull-down Resistor
PC3D01D, PC3D11D, PC3D21D and PC3D31D

Schmitt Trigger Input Thresholds for 1.8V Process Option

Cell Name	VT+			VT-			Hysteresis		
	Min.	Max.	Typical	Min.	Max.	Typical	Min.	Max.	Typical
PC3D21D	0.9401V	1.1460V	1.0425V	0.4866V	0.6933V	0.5886V	0.3862V	0.4995V	0.4537V
PC3D31D	0.9431V	1.1493V	1.0792V	0.4877V	0.6916V	0.5877V	0.3863V	0.4997V	0.4539V

1.8V CMOS Input Only Pads with Pull-up Resistor
PC3D01U, PC3D11U, PC3D21U and PC3D31U

PC3D01U, PC3D11U, PC3D21U and PC3D31U cells are inputs pads with pull-up. PC3D01U is CMOS non inverting, PC3D11U is CMOS inverting, PC3D21U is CMOS Schmitt non inverting, and PC3D31U is a CMOS Schmitt inverting input pad.



Function Table

INPUT		OUTPUT
PAD(n-1)	PAD(n)	CIN
L	L	L
H	H	H
X	Hr	H
r = resistive drive strength		

Function Table

INPUT		OUTPUT
PAD(n-1)	PAD(n)	CIN
L	L	H
H	H	L
X	Hr	L
r = resistive drive strength		

Cell Description

Macro Name:	PC3D01U	PC3D11U	PC3D21U	PC3D31U
Leakage Power (μW)	30.610	30.609	30.610	30.610

Pin Description

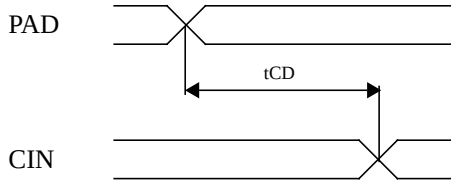
Name	Capacitance (pF)				Description
	PC3D01U	PC3D11U	PC3D21U	PC3D31U	
PAD	3.185	3.142	3.135	3.135	Input
Maximum capacitance					
CIN	0.8	0.8	0.8	0.8	Output

Pin Powers for:
Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns

Name	Pin Power (pW/Hz)				Description
	PC3D01U	PC3D11U	PC3D21U	PC3D31U	
CIN	5.6	5.9	5.5	6	Output

1.8V CMOS Input Only Pads with Pull-up Resistor
PC3D01U, PC3D11U, PC3D21U and PC3D31U

Waveforms



Timing Numbers for PC3D01U, PC3D11U, PC3D21U and PC3D31U:

Propagation Delays tCD (ns) for Sample Core Loads:
Standard Pad Input Transition = 1 ns, Core Load Unit = 0.01 pF

Cell Name	Core Load Fanout									
	2		4		8		16		32	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3D01U	0.553	0.897	0.565	0.913	0.590	0.947	0.632	1.012	0.715	1.142
PC3D11U	0.971	0.743	0.983	0.759	1.007	0.790	1.045	0.848	1.122	0.964
PC3D21U	0.711	1.395	0.726	1.426	0.757	1.490	0.796	1.588	0.875	1.784
PC3D31U	1.422	1.015	1.431	1.040	1.450	1.090	1.485	1.178	1.556	1.353

Propagation Delays tCD (ns) for Sample Pad Input Transitions:
Standard Core Load = 0.16 pF

Cell Name	Pad Input Transition									
	1 ns		2 ns		5 ns		10 ns		15 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3D01U	0.632	1.012	0.778	1.245	0.979	1.736	1.163	2.355	1.346	2.974
PC3D11U	1.045	0.848	1.283	1.000	1.813	1.208	2.480	1.400	3.147	1.592
PC3D21U	0.796	1.588	1.028	1.890	1.556	2.809	2.288	4.303	3.019	5.796
PC3D31U	1.485	1.178	1.788	1.428	2.702	1.983	4.185	2.760	5.668	3.537

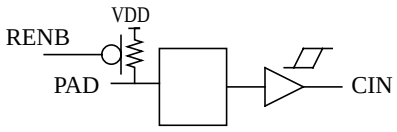
1.8V CMOS Input Only Pads with Pull-up Resistor
PC3D01U, PC3D11U, PC3D21U and PC3D31U

Schmitt Trigger Input Thresholds for 1.8V Process Option

Cell Name	VT+			VT-			Hysteresis		
	Min.	Max.	Typical	Min.	Max.	Typical	Min.	Max.	Typical
PC3D21U	0.9401V	1.1460V	1.0425V	0.4866V	0.6933V	0.5886V	0.3862V	0.4995V	0.4537V
PC3D31U	0.9431V	1.1493V	1.0792V	0.4877V	0.6916V	0.5877V	0.3863V	0.4997V	0.4539V

1.8V CMOS Input Only Pad with Controllable Pull-up Resistor
PC3D21EU

PC3D21EU cell is CMOS Schmitt non inverting input pad with controllable pull-up resistor.



Function Table

INPUT			OUTPUT
RENB	PAD(n-1)	PAD(n)	CIN
X	L	L	L
X	H	H	H
L	Hr	Hr	H
H	Z	Z	X
r = resistive drive strength			

Cell Description

Macro Name:	PC3D21EU
Leakage Power (µW)	30.610

Pin Description

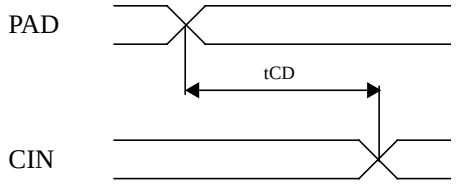
Name	Capacitance (pF)	Description
	PC3D21EU	
PAD	3.135	Input
RENB	0.11	Input
Maximum capacitance		
CIN	0.8	Output

Pin Powers for:
Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns

Name	Pin Power (pW/Hz)	Description
	PC3D21EU	
CIN	5.5	Output

1.8V CMOS Input Only Pad with Controllable Pull-up Resistor
PC3D21EU

Waveforms



Timing Numbers for PC3D21EU:

Propagation Delays tCD (ns) for Sample Core Loads: Standard Pad Input Transition = 1 ns, Core Load Unit = 0.01 pF

Cell Name	Core Load Fanout									
	2		4		8		16		32	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3D21EU	0.711	1.395	0.726	1.426	0.757	1.490	0.796	1.588	0.875	1.784

Propagation Delays tCD (ns) for Sample Pad Input Transitions: Standard Core Load = 0.16 pF

Cell Name	Pad Input Transition									
	1 ns		2 ns		5 ns		10 ns		15 ns	
	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL	RISE	FALL
PC3D21EU	0.796	1.588	1.028	1.890	1.556	2.809	2.288	4.303	3.019	5.796

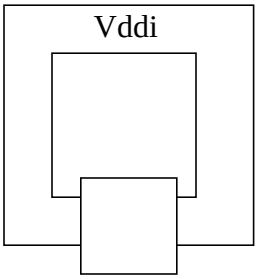
Schmitt Trigger Input Thresholds for 1.8V Process Option

Cell Name	VT+			VT-			Hysteresis		
	Min.	Max.	Typical	Min.	Max.	Typical	Min.	Max.	Typical
PC3D21EU	0.9401V	1.1460V	1.0425V	0.4866V	0.6933V	0.5886V	0.3862V	0.4995V	0.4537V

VDD Pads

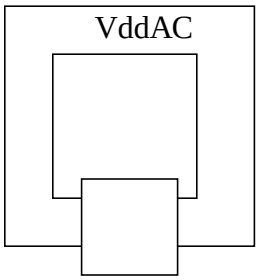
PVDI, PVDA, PVDC and PVCF/PVCE.

PVDI is a power pad that supplies VDD to the core and IO predriver circuitry.



Pad Site Required:	1
Pin Power (pW/Hz) of pin PAD for Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns	0.0

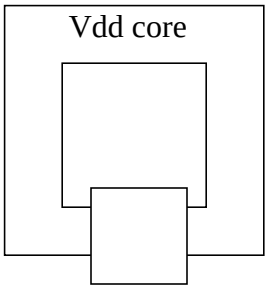
PVDA is a power pad that supplies VDDO to the AC section of the I/O buffer circuitry.



Pad Site Required:	1
Pin Power (pW/Hz) of pin VDDO for Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns	0.0

VDD Pads
PVDI, PVDA, PVDC and PVCF/PVCE

PVDC is a power pad that supplies VDD to core only.



Pad Site Required:	1
Pin Power (pW/Hz) of pin VDDC for Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns	0.0

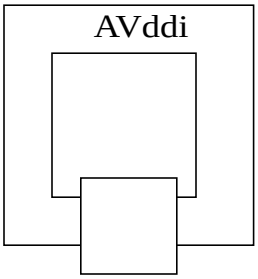
PVCF, PVCE:

There is no icon for these two cells.

For more details on these cells *See "New Features" on page 1-2.*

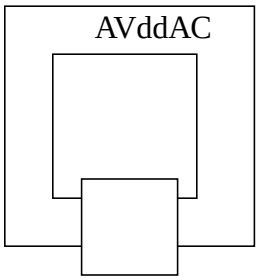
AVDD Pads
APVDI and APVDA.

APVDI is a power pad that supplies AVDD to analog core and the predrive of cells supplied by analog power .



Pad Site Required:	1
Pin Power (pW/Hz) of pin AVDD for Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns	0.0

APVDA is a power pad that supplies AVDDO to the AC section of the cell supplied by analog power I/O buffer circuitry.

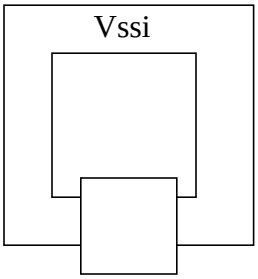


Pad Site Required:	1
Pin Power (pW/Hz) of pin AVDDO for Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns	0.0

VSS Pads

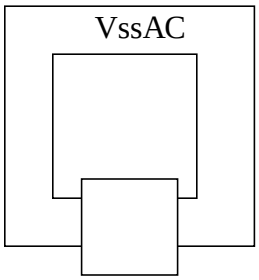
PV0I, PV0A, PV0C and PV0F.

PV0I is a power pad that supplies VSS to the core and IO predriver circuitry.



Pad Site Required:	1
Pin Power (pW/Hz) of pin VSS for Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns	0.0

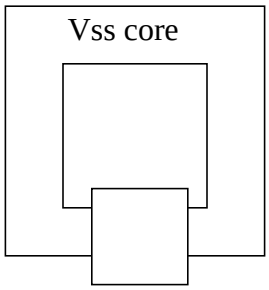
PV0A is a power pad that supplies VSSO to the AC section of the I/O buffer circuitry.



Pad Site Required:	1
Pin Power (pW/Hz) of pin VSSO for Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns	0.0

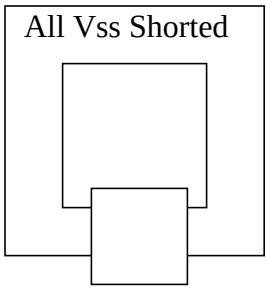
VSS Pads
PV0I, PV0A, PV0C and PV0F

PV0C is a power pad that supplies VSS to core only.



Pad Site Required:	1
Pin Power (pW/Hz) of pin VSS for Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns	0.0

PV0F is a power pad that shorts all VSS and VSSO power busses together.

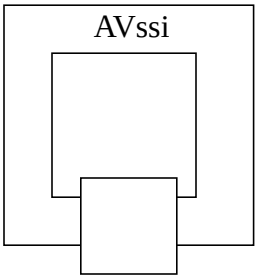


Pad Site Required:	1
Pin Power (pW/Hz) of pin VSS for Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns	0.0

AVSS Pads

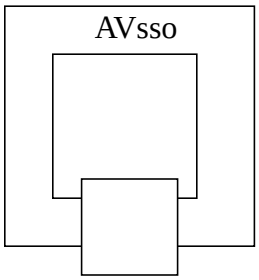
APV0I and APV0A .

APV0I is a power pad that supplies AVSS to the core.



Pad Site Required:	1
Pin Power (pW/Hz) of pin AVSS for Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns	0.0

APV0A is a power pad that supplies AVSSO to the AC section of the cells supplied by analog power I/O circuitry .



Pad Site Required:	1
Pin Power (pW/Hz) of pin AVSSO for Standard Core Load = 0.16 pF, Standard Pad Input Transition = 0.5 ns	0.0

Chapter 3
Derating Information

The propagation delay and power values apply only to the specified operating conditions of VDD = 1.8 volt, VDDO = 1.8 volt, junction temperature = 25 degrees C, and typical-case process. You can estimate the delay and power under different conditions by using tables in this chapter. The sections in this chapter provide information on the following:

Timing Derating

To calculate the delay under different conditions you can use the following timing constraint equations:

***timing_rise* (new) = *timing_rise* (datasheet) * Ev_rise * Et_rise * Ep_rise**

***timing_fall* (new) = *timing_fall* (datasheet) * Ev_fall * Et_fall * Ep_fall**

where:

Ev_rise = 1 + (VDDnew - VDD) * k_*voltage_timing_rise*
Et_rise = 1 + (T_new - T) * k_*temperature_timing_rise*
Ep_rise= 1 + (P_new - P) * k_*process_timing_rise*

Ev_fall = 1 + (VDDnew - VDD) * k_*voltage_timing_fall*
Et_fall = 1 + (T_new - T) * k_*temperature_timing_fall*
Ep_fall= 1 + (P_new - P) * k_*process_timing_fall*

The timing coefficients of the delay propagation are shown in the following tables:

k_voltage

Transition	Delay propagation
Rise	-0.8895
Fall	-0.8527

k_temperature

Transition	Delay propagation
Rise	0.0012
Fall	0.0013

k_process

Transition	Delay propagation
Rise	1.3072
Fall	1.2549

The process bias index are shown in the following table:

Process	Index (P)
Slow	1.2
Typical	1.0
Fast	0.8

Timing Derating Example.

The following example shows a delay propagation assessment in the below conditions:

Junction Temperature = 80 degrees C
VDD = 1.3 Volts
Process = slow
tDelay_Rise (datasheet, PC3T01) = 2.799 ns

tDelay_Rise (new) = tDelay (datasheet, PC3T01) * Ev_rise * Et_rise * Ep_rise

where:

Ev_rise = 1 + (1.3 - 1.8) * (-0.8895) = 1.4448
Et_rise = 1 + (80 - 25) * 0.0012 = 1.0660
Ep_rise = 1 + (1.2 - 1.0) * 1.3072 = 1.2614

tDelay_Rise (new) = 2.799 * 1.4448 * 1.0660 * 1.2614 = 5.437 ns

Power Derating

To calculate leakage power or internal power under different conditions you can use the following power constraint equations:

***Leakage power* (new) = *Leakage power* (datasheet) * Ev_leakPwr * Et_leakPwr *Ep_leakPwr**

***Internal power* (new) = *Internal power* (datasheet) * Ev_intrnPwr * Et_intrnPwr * Ep_intrnPwr**

where:

Ev_leakPwr = 1 + (VDDnew - VDD) * k_*voltage_Leakage_power*
Et_leakPwr = 1 + (T_new - T) * k_*temperature_Leakage_power*
Ep_leakPwr= 1 + (P_new - P) * k_*process_Leakage_power*

Ev_intrnPwr = 1 + (VDDnew - VDD) * k_*voltage_Internal_power*
Et_intrnPwr = 1 + (T_new - T) * k_*temperature_Internal_power*
Ep_intrnPwr = 1 + (P_new - P) * k_*process_Internal_power*

The power coefficients are shown in the following tables:

k_voltage

Leakage_power	Internal_power
0.0000	0.0000

k_temperature

Leakage_power	Internal_power
0.0000	0.0000

k_process

Leakage_power	Internal_power
0.0000	0.0000

Derating Leakage Power Example.

The following example shows a Leakage Power assessment in the below conditions:

Junction Temperature = 80 degrees C
VDD = 1.3 Volts
Process = slow
Leakage Power (datasheet, PC3T01) = 2853.3 pW

Leakage Power (new) = Leakage Power (datasheet, PC3T01) * Ev_leakPwr * Et_leakPwr * Ep_leakPwr

where:

Ev_leakPwr = 1 + (1.3 - 1.8) * (0.0000) = 1.0000
Et_leakPwr = 1 + (80 - 25) * 0.0000 = 1.0000
Ep_leakPwr = 1 + (1.2 - 1.0) * 0.0000 = 1.0000

Leakage Power (new) = 2853.3 * 1.0000 * 1.0000 * 1.0000 = 2853.3 pW

Derating Internal Power Example.

The following example shows an Internal Power assessment in the below conditions:

Junction Temperature = 80 degrees C
VDD = 1.3 Volts
Process = slow
Internal Power (datasheet, PC3T01) = 21 pW/Hz

Internal Power (new) = Internal Power (datasheet, PC3T01) * Ev_intrnPwr * Et_intrnPwr * Ep_intrnPwr

where:

Ev_intrnPwr = 1 + (1.3 - 1.8) * (0.0000) = 1.0000
Et_intrnPwr = 1 + (80 - 25) * 0.0000 = 1.0000
Ep_intrnPwr = 1 + (1.2 - 1.0) * 0.0000 = 1.0000

Internal Power (new) = 21 * 1.0000 * 1.0000 * 1.0000 = 21.015 pW/Hz

Chapter 4

Pull-up and pull-down resistors

The pull-up/pull-down function is realized by the resistance of the active devices. The internal pull-up/pull-down resistance must be defined due to the nonlinear nature of the active devices.The internal pull-up resistance is defined by the value when the input pad is at its low level, while the internal pull-down resistance is defined when the pad is at its high level. The following table is used for the max, typ, and min cases:

	I/O voltage (Volts)	Temp (^{o}C)	Process
Max	1.65	125	ss
Typ	1.8	25	tt
Min	1.95	-40	ff

The resistance value of the pull-up device is showed below (when the pad voltage is at 0):

	Max	Typ	Min
Pull-up Resistance	167K	106K	68K

The resistance of the pull-down device is showed below (when the pad voltage is at VDDO):

	Max	Typ	Min
Pull-down Resistance	152K	88K	46K
pc3b03ed Pull-down Resistance	199K	122K	70K

Note: Synopsys, Inc. recommends that the pull-up/pull-down cells are used if the pull-up/pull-down function is needed. If this implementation is impossible, an external resistor with value of no greater than 19K Ohms is recommended.

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