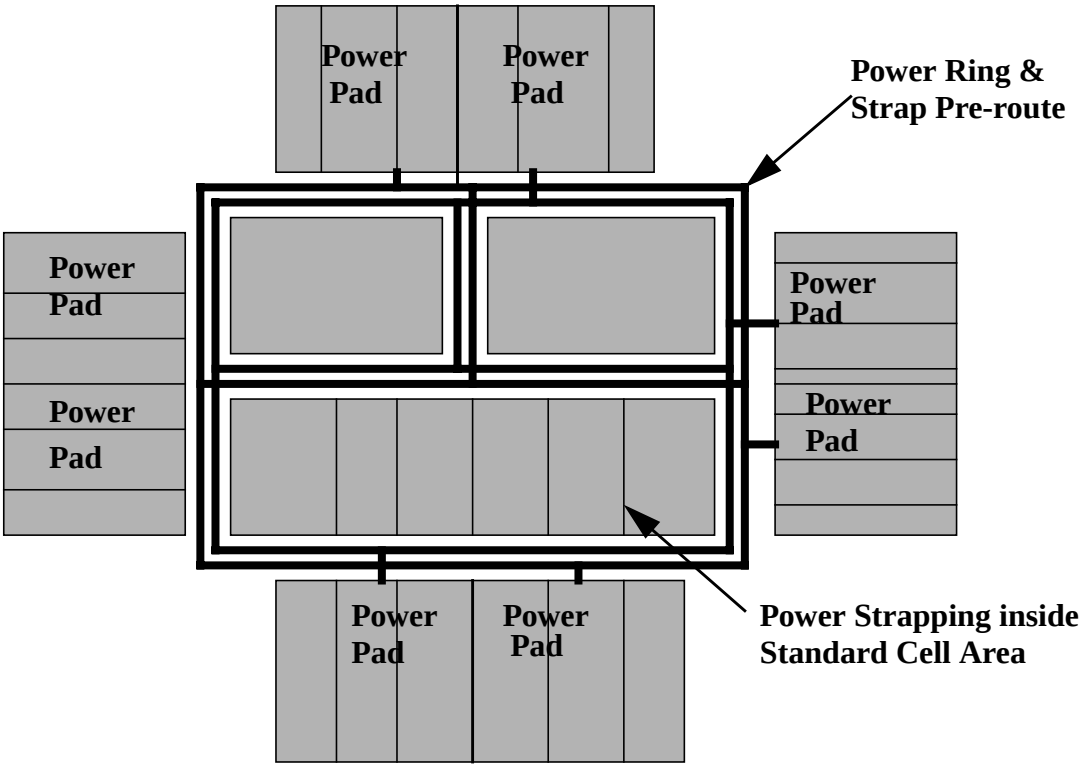
POWER DISTRIBUTION GUIDELINES FOR TOWER 0.18 μm LIBRARIES

I. INTRODUCTION TO POWER SUPPLY GUIDELINES

For the power supply of your design you have to distinguish between the global power supply for the core area and the power supply inside standard cell areas, known as ***power strapping.***

For the global power supply you have to estimate the power consumption of your macro and standard cell blocks to calculate the power ring width and number pads, for standard cell areas common guidelines and equations for power strapping are given in this document.

Fig.1:Schematic Power Supply



II. POWER STRAPS INSIDE STANDARD CELL AREAS

A. Why use power straps?

Power straps are an important part of the standard cell power supply. Normally the standard cells are too big to guarantee sufficient power supply just through the horizontal power rails inside the standard cells. Depending on the length of the rows, the operating frequency, the power bus resistance and other parameters a voltage drop or inflated current density could occur along the power rail.

To prevent these effects, the following guidelines should be used for standard cell block design:

B. End and Internal Power Straps

At the beginning and the end of a standard cell row a pair of power straps (Vdd and Vss) should always be added. In general each P&R tool provides different functions to add power straps or a power ring at the block boundary. Some tools might give you the choice to add a power strap on one side and a ground strap on the other side, but we recommend to always add a pair of power and ground straps on each side.

Cadence Cell Ensemble builds a power ring all around the standard cell block and in Synopsys Apollo you have the choice, on which sides and top or bottom you want to have a strap.

III. Spacing between Power Straps

The TOWER 0.18 µm libraries have been characterized for power. The power model of each of the cell is complex, and deriving manually a power figure for a block is complicated. There are tools like MARS-RAIL, which can interpreted this data, take into account simulation data and size properly the power rails. It is highly recommended to stop reading this guideline here, and use these tools.

IV. CORE POWER STRAP AND RING PREROUTE

For the core power supply you have to consider the power consumption of your macros and standard cell blocks.Based on these values you have to calculate the width of the power buses.

A. Maximum current

Based on your foundry, the maximum current per µ wire width can vary between 0.5mA/µm up to1.0mA/µm, but don’t forget to contact your foundry for reliability data. Since the thickness increases on the upper layers, their maximum current capability is slightly higher.

You have to consider the current for the width of your power pre-routes as well as for the number of power pads you need, depending on their connector

width. See “Manual Power Strap Estimations For Maximum current” on page 4 for hand calculation.

For Power Pad usage, please refer to Power Pad Usage (SSO guidelines) corresponding to your foundry to define the number of VDD and VSS PAD required.

B. Maximum IR-drop

During the power pre-route you have to check the length of the wires, so that the IR-drop does not exceed 0.1V. Otherwise you have to increase the wire with or add some additional power pads. It is difficult to derive equation to calculate this the width of the power lines depending on the maximum IR drop. Studies always involve simulation of resistance matrices with Star-Hspice. Tools are always needed even for the study, it is why it is highly recommended to use tools dedicated to these analysis.

V. ELECTROMIGRATION RULES

To avoid electro-migration problems, the output pin of some specific cells (bufbda, buffda, buftda, inv0da & invtda) have been enlarged to 0.5 µm.

It is advised to make sure that the router uses wires with the same width of metal as the pin width.

Apendix A: Manual Power Strap Estimations For Maximum current

A. Average power of a block.

DI: incremental current due to the number of cells in the row, in units of μA/(MHz*μm). This term takes into account the bus current needed to supply cells in the standard cell row, and it is basically the total current-per-MHz of all the cells in a statistical row divided by the row length in μm. On average there are M 1x inverters driving an 1x load per micron and N 1x inverters driving a 4x load. The current used by these inverters are I_M and I_N respectively. This number need to be divided by the length of the inverter.

$$DI = \frac{\frac{M \times I_M + N \times I_N}{M + N}}{L_{Inv}}$$

With the parameters for the TOWER 0.18 μm library you get the following results:

Number of 1x drive	M	0.7/μm
Number of 4x drive	N	0.3/μm
Current 1x drive	I_M	0.013pA
Current 4x drive	I_N	0.020pA
Length 1x Inverter	L_{inv}	1.73μm
Incremental Current	**DI**	**0.009pA/μm/Mhz**

B. Calculation of the total current I_t

$$I_t = DI \times L_c \times N_c \times F$$

N_c: number of rows

L_c: length of one row in μm.

I_t: total Current used in a block

F: frequency in Mega Hertz

C. The maximum current in the horizontal Power lines.

The factor2 assumes power lines supplied from both ends:

$$I_c = W_c \times N_c \times 2 \times D_c$$

I_c: current in a horizontal M1 power line.

D_c: Max current density in a horizontal M1 power line.

W_c: Width of horizontal M1 power line.

D. Current In all vertical straps

The rest of the current needed for the block needs to be supplied by the vertical strips (here again we divide by 2 because the vertical strips are assumed to be supplied by both ends):

$$I_s = \frac{I_t - I_c}{2}$$

I_S: Total current supported by the vertical strips in mA

E. Total vertical strip width

$$W_{Ts} = \frac{I_s}{D_s}$$

D_S: Current density of vertical strip.

W_{Ts}: Total width of the vertical strip in μm.

F. Number of vertical strips and width of each vertical strip.

$$N_s = \frac{I_t}{I_c} \qquad W_s = \frac{W_{Ts}}{N_s}$$

N_S: Number of vertical strips.

W_S: width of the vertical power lines in μm.

G. Example

Incremental Current	*DI*	*0.009pA/μm/Mhz*
Frequency	F	100Mz
Number of rows	N_c	100
Length of row	L_c	5000μm
Total Current of the block	I_t	*450mA*
Width of M1 power line	W_c	0.74μm
M1 current density	D_c	1.0mA/μm
Max Horizontal Current	I_c	*148mA*
Total Vertical current	I_s	*151mA*
M2 current density	D_s	1.0mA/μm
Total vertical strap width	W_{Ts}	*151μm*
Number of vertical straps	**N_s**	**3**
Width of vertical straps	**W_s**	**50μm**