TSL18CIO150
SSO Guidelines (Power Pad Usage Rules)
Application Notes

Version 1.0

October 2003

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Printed in the U.S.A.
Document Order Number:

Revision History

Document Version Number	Library Name	Date	Notes
1.0	TSL18CIO150	October 2003	Production Release

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Introduction

The purpose of this document is to help the 0.18 µm IO library users to calculate the number of power pads to be used in their design.

This document give the basic guidelines for **Simultaneously Switching Outputs** (SSO), for **currents density** and for **electrostatic discharge** (ESD) issues, to allow to optimize the placement the power pads. However this document does not intend to give a complete description of the electromigration and ESD phenomenon.

Noise is created across the parasitic inductors in the power and ground networks of a chip when an output pad switches from one state to another. The noise is equal to:

$$v = L \cdot \frac{di}{dt}$$

(eq. 1)

where *L* is the effective inductance of the power or ground network and *di/dt* is the rate of change of the charging or discharging current.

When several outputs switch simultaneously the increased rate of change of current can produce a large enough voltage spike which appears at the output of the nearby non-switching (quiet) output pads to cause system errors. To reduce noise the effective inductance of the power or ground network L and the *di/dt* must be reduced. The I/O pads in the tsl18cio150 library have 5 different CMOS drive strengths (1X, 2X, 3X, 4X and 5X) and all the I/O pads are built to have reduced *di/dt* using a patented design.

Definition of SSO Window

For the purpose of this guideline, a *SSO window* is defined as *beginning* when an output pad begins to switch and *ending* when the output pad finishes switching. One way to get the approximate size of the SSO window is to know the rise and falling transition of the IO cell. This delay is not available in the data sheet. You can get this information in the Synopsys model for example.

The transition time is Synopsys model from Tower library is extrapolated from 0% to 100%. That is to say the SSO window for one IO is equal to this transition time. If the Synopsys model you are referring is not stuffed with *transition* timing from rail to rail, you have to adjust the SSO window value because the SSO window doesn't end until the output finishes switching completely.

Definition of SSO Group.

Simultaneously Switching Output Group is defined as the *group* of output pads whose

individual SSO window may overlap either fully or partially with others. If, for example, a 32 bit bus switches then there are 32 SSO windows, one for each output. The number of SSOs can be determined from the maximum number of SSO windows which overlap. If no special care is taken to stagger the switching of the bus then it is likely that all SSOs windows overlap and resulting in 32 SSOs. For instance, a 32-bit bus is likely designed with 32 SSO, meaning the 32-bit SSO windows are overlapped during switching.

Power and Ground pins placement

General rules

- If possible, select the pins with the lowest inductance for power and ground pads. Don't forget to include approximately 1.0 nH for the *bond wire inductance* if it's true value is not known. For more details about the power pad placement see the specific application note *"Power Pad Placement Application Note"*.

Power pads for core power and core ground (PVDI, PV0I, PVDC, PV0C)

- Distribute them as evenly as possible around the chip. Their number depend on the *power consumption* of the core of the design.
- The *PVDI* is designed to allow a DC current up to 126mA. This value assume that all metal layer up to metal 6 are used. The table below give the DC current for the corresponding *topmetal layer* used at 110^{o}C.

Top metal layer	max DC current
metal 6	**126mA**
metal 5	70mA
metal 4	70mA

Core power pad current density

- To avoid ESD trouble (see “ESD trouble considerations” on page 4.) the resistivity of the power bus must be lower than 2 Ohms. Then, the distance of any IO pad to any PVDI must be lower than the value of the following table:

Top metal layer	max distance to PVDI (in IO number)
metal 6	18

Top metal layer	max distance to PVDI (in IO number)
metal 5	15
metal 4	9

Core power pad max distance to I/O

This max distance is given by the equation:

$$MaxIoNumber = \frac{MaxResistanceAllowed}{MetalResistivity \times \frac{IoPitch}{MetalWidth}}$$

Power pads for noisy I/O power and ground (PVDA and PV0A)

- These power pads must be placed close to each SSO group. It is recommended to use power pads for each group even if they are SSO window are not overlapping in the case the SSO group are not enough close.
- For the number of power pad to be used for an SSO group please refer to the chapter “Power and ground pin number.” on page 4.
- Do not put the power (PVDA) and ground (PV0A) pads farther than 8 pad slots away from one IO of the SSO group.

See also power rail metal width at the section “Metal Electromigration Considerations” on page 15.

Power and ground pin number.

This chapter treat about the number of power pad used to supply the noisy power ring of the I/O cells. For the other power pad see “General rules” on page 2.

The power and ground pin number you must use in your design is depending on three parameters:

- The DC current need by your design.
- The ESD threshold.
- The *sso* I/Os number.

DC current consideration

Due to the risk of metal electromigration, each power or ground pad must be limited to a maximum average DC *current density* of 96 mA when **metal6** is used as top metal layer.

For more details see “Metal Electromigration Considerations” on page 15.

ESD trouble considerations

There is no ESD trouble for the power pads. The distance for the power pad for VDDO buses can be at any distance of the IO. See also “Power pads for noisy I/O power and ground (PVDA and PV0A)” on page 3.

SSO number considerations

Power pad number

A SSO group is generating noise on the VDDO and VSSO power ring due to the second order circuit created by the capacitive load of the I/O and the inductance of the pins which are connected to the bonding of the I/O cells and power cells.

The capacitance can be specific to each output of the SSO group. But for this study we will consider that all I/O are connected to the same load (*Cload*).

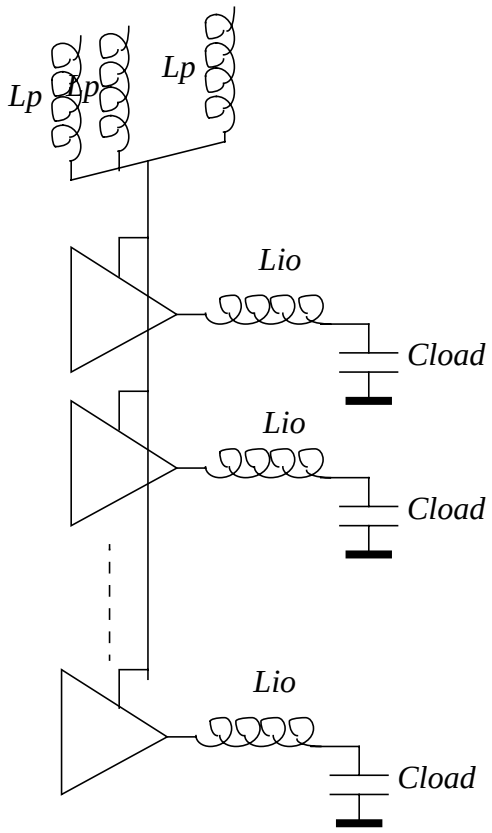
Since the load of each pin is the same, we can assume that all the IO of the SSO group will be the same.

We will also consider that:

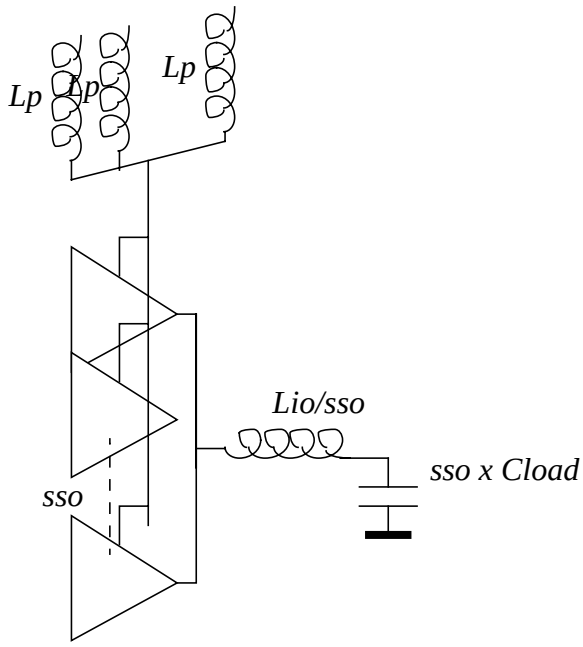
- the I/O cell are connected to the same type of pin in the package and these pin have the same inductance *Lio*.
- the power pads are connected to the same type of pin in the package which inductance is *Lp*.

Simulation model

The following schematic shows the considered *pin package model*:



This schematic can be simplified as following:



Where the total inductance *Lt* will be:

$$Lt = \frac{Lp}{np} + \frac{Lio}{sso}$$

(eq. 2)

Where *sso* is the number of IO into the SSO window.

Where *np* is the number of power pad needed to be placed in parallel to supply the power ring to meet the SSO guidelines.

The measuring of the maximum value of *Lt* must be done using a SSO group of *sso* I/Os.

The number of power pad *np* can be then easily calculated using the (eq. 2):

$$np = \frac{Lp}{Lt - \frac{Lio}{sso}}$$

(eq. 3)

If *sso* > 8, the inductance of the IO pin can be negligible and *np* becomes independent of

sso. The (eq. 3) becomes:

$$np \approx \frac{Lp}{Lt}$$

(eq. 4)

If we integrate the (eq. 1) where *L* is *Lt* from (eq. 2), that yields:

$$v \times To = Lt \times Iref$$

(eq. 5)

Where *Iref* is the current strength of the IO. Since the IO of the SSO window are supposed to be the same, the current *Iref* is linear with the sso number and can be written:

$$Iref = sso \times i$$

(eq. 6)

Where *i* is the drive of the 1X IO.

The (eq. 2) becomes:

$$\frac{v \times To}{i} = Lt \times sso$$

(eq. 7)

That lead the term *sso x Lt* to be constant at the time To since *v* is the max excursion for the noise voltage, and *i* is constant.

The following equation can be then written:

$$Leff \times ssoref = Lt \times sso$$

(eq. 8)

Where *Leff* and *ssoref* are the respective measured max inductance for the correspondent sso in the following tables see “The Inductance table” on page 8.

Then if we consider the number of sso enough large to neglect *Lio*, the (eq. 4) and the (eq. 8) give:

$$np \approx \frac{Lp \times sso}{ssoref \times Leff}$$

(eq. 9)

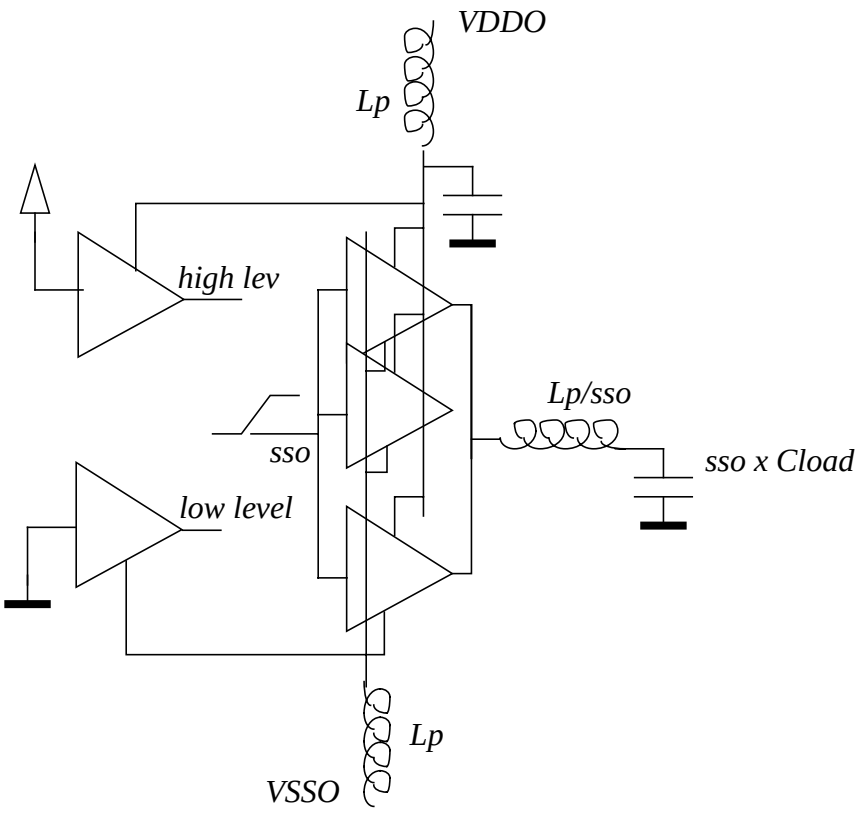
Where *sso* is any number of IO in the SSO window.

In this document the usable *ssoref* is 8.

The Inductance table

The table page 8 shows the maximum effective pin inductance allowed for each type of CMOS pad to limit the VDDO or VSSO bouncing noise to a value that respect 0.25*VDDO and 0.75*VDDO and as max values VDDO+0.7V and min value VSSO-0.7V.

Simulated models



In the optimization, *Lio* is considered equal to *Lp*, that is to say the pin package inductance is assumed to be the same for the one used as power pin and the others.

Process effect

The typical and best cases have been used to run simulation in typical and worst noise conditions.

The *typical conditions* are:

- Typical corner model
- Temperature is 25°C
- Voltages are 1.8 volt for I/Os and 1.8 volt for the core and I/O logical structure.

The *best conditions* are:

- Fast-Fast corner model
- Temperature is -40°C
- Voltages are 1.95 volt for I/Os and 1.98 volt for the core and I/O logical structure.

SSO measurements.

The *optimization* has been performed with an SSO group of 8,12 and 16 I/Os. For other SSO values see “Extrapolation to other SSO group” on page 9.

Extrapolation to other SSO group

The extrapolation from the measured value in the next table to other SSO number can calculated using the following equation:

$$np \approx \frac{Lp \times sso}{8 \times Leffref}$$

(eq. 10)

From (eq. 9), where sso is a number above 8 and *Leffref* is the *Leff* for the corresponding I/O at the determined loading for SSO=8.

Example:

Calculate the *np* for a *sso* of 32 pads 1X and for Cload=5pf, the power pin inductance is 2nH.

The inductance table (page 10) gives for the drive 1X with 5pf an inductance value of 13.29nH for 8 *sso*, the *np* values is then:

$$np = \frac{2.0 \times 32}{8 \times 13.29} \approx 1$$

(eq. 11)

As a results, 1 power pad will be needed for VDDO and 1 power pad will be needed for VSSO.

Typical case inductance measurement

Leff (nH)	1X IO Drive					
	100 MHz			130 MHz		
sso	2.5pF	5pF	7.5pF	2.5pF	5pF	7.5pF
8	20.64	13.29	10.46	13.59	11.11	10.21
12	14.37	8.42	6.51	9.63	7.68	6.43
16	**11.06**	**6.2**	**4.89**	**7.31**	**5.76**	**5.2**

Leff (nH)	2X IO Drive					
	100 MHz			130 MHz		
sso	7.5p	10p	15p	7.5p	10p	15p
8	8.48	6.93	4.91	5.08	3.87	3.33
12	5.8	4.62	3.29	3.25	2.67	2.19
16	**4.44**	**3.45**	**2.52**	**2.47**	**2.02**	**1.65**

Leff (nH)	3X IO Drive					
	100 MHz			130 MHz		
sso	10p	15p	20p	10p	15p	20p
8	7.53	4.58	3.45	3.23	2.46	2
12	4.42	3.1	2.35	2.21	1.62	1.31
16	**3.32**	**2.36**	**1.77**	**1.66**	**1.22**	**0.97**

Leff (nH)	4X IO Drive					
	100 MHz			130 MHz		
sso	15p	20p	25p	15p	20p	25p
8	4.44	3.47	2.59	2.17	1.73	1.49
12	3.06	2.34	1.75	1.46	1.1	0.94
16	**2.3**	**1.76**	**1.29**	**1.08**	**0.81**	**0.68**

Leff (nH)	5X IO Drive					
	100 MHz			130 MHz		
sso	20p	25p	30p	20p	25p	30p
8	3.42	2.6	2.01	1.54	1.28	1.19
12	2.33	1.71	1.33	0.98	0.82	0.76
16	**1.74**	**1.31**	**0.99**	**0.73**	**0.63**	**0.57**

Note: A few data might miss to the table that are due to non convergency in the hspice simulation optimization.

Best cases inductance measurement

Leff (nH)	1X IO Drive					
	100 MHz			130 MHz		
sso	2.5pF	5pF	7.5pF	2.5pF	5pF	7.5pF
8	8.14	9.96	8.14	8.74	6.54	4.92
12	5.52	6.88	5.52	6.36	4.26	3.38
16	**4.25**	**5.15**	**4.31**	**4.85**	**3.36**	**2.66**

Leff (nH)	2X IO Drive					
	100 MHz			130 MHz		
sso	7.5p	10p	15p	7.5p	10p	15p
8	4.59	5.15	4.96	4.72	4.08	2.75
12	3.29	3.33	3.43	3.16	2.87	1.89
16	**2.39**	**2.58**	**2.6**	**2.37**	**2.19**	**1.43**

Leff (nH)	3X IO Drive					
	100 MHz			130 MHz		
sso	10p	15p	20p	10p	15p	20p
8	3.57	4.18	4.26	3.1	2.97	2.16
12	2.35	2.84	2.9	2.23	2.04	1.46
16	**1.73**	**2.15**	**2.14**	**1.71**	**1.55**	**1.11**

Leff (nH)	4X IO Drive					
	100 MHz			130 MHz		
sso	15p	20p	25p	15p	20p	25p
8	2.69	3.14	3.21	2.5	2.25	1.72
12	1.81	2.17	2.23	1.68	1.54	1.15
16	**1.32**	**1.6**	**1.73**	**1.3**	**1.16**	**0.86**

Leff (nH)	5X IO Drive					
	100 MHz			130 MHz		
sso	20p	25p	30p	20p	25p	30p
8	2.38	2.61	2.57	2.05	1.82	1.42
12	1.58	1.77	1.76	1.35	1.22	0.95
16	**1.17**	**1.32**	**1.38**	**1.09**	**0.92**	**0.72**

Note: A few data might miss to the table that are due to non convergency in the hspice simulation optimization.

Extrapolation to other CMOS and TTL pads

The value of the previous table have been simulated using output pad (PC3O01 to PC3O05) of the I/O library. The other *CMOS pad* guidelines can be derived from this results using the corresponding drive.

For the *TTL pad* the corresponding table between CMOS IO and TTL can be used to determine the *Leff* inductance:

TTL pad	Cmos pad drive matching
Drive 1 TTL pad (1X)	Drive 1 CMOS pad (1X)
Drive 2 TTL pad (2X)	Drive 3 CMOS pad (3X)
Drive 3 TTL pad (3X)	Drive 5 CMOS pad (5X)

Calculation examples

Example 1

Your bus is 32 bits wide. You are using only 2x bidirectional IO (PC3B02). The

capacitance of the bus is 10pF. The max frequency is 100MHz. The pin's inductance of your package is 5nH. All the pins have the same inductance.

- Determine the number of power pad needed for this SSO group:

$$np = \frac{5 \times 32}{8 \times 6.93} \approx 3$$

- If you decide to make your design working at 130MHz the number of power pads would be:

$$np = \frac{5 \times 32}{8 \times 3.87} \approx 6$$

Example 2

Your bus is 32 bits wide. You are using 2x and 4x bidirectional IO (16 PC3B02 and 16 PC3B04). The capacitance of the bus is 10pF. The max frequency is 100MHz. The pin's inductance of your package is 5nH. All the pins have the same inductance.

This case is equivalent to consider two SSO groups independent. Determine *np* is equivalent to calculate *np1* and *np2* for each SSO group

- The value of the capacitance does not appear in the table for 4X drive, use the closest one (15pF).
- Calculate the number of power pad for the SSO window made by the 16 PC3B02:

$$np1 = \frac{5 \times 16}{8 \times 6.93} \approx 2$$

- Calculate the number of power pad for the SSO window made by the 16 PC3B04:

$$np2 = \frac{5 \times 16}{8 \times 4.44} \approx 3$$

- Calculate the number of power pad for the total SSO window made by the 5 I/Os:

$$np = np1 + np2 = 5$$

Note: this number has to be compared to np of the first example.

Example 3

Your design includes two buses. The design insures that they are not switching at the same time. They do not belong to the same SSO group. You will be then allowed to reduce the number of power pad with the following method.

- First of all the bus must be located on the same portion of the guarding. If the I/O buses are far away one for the other it is advised to give to each SSO group its own power pad set.
- Calculate the np of each bus.
- Compare the np and keep the bigger np.
- Place the power IO as evenly as possible between the IO of the two buses.

In the “Example 2” on page 13, if the 16 PC3B02 and 16 PC3B04 belong to two different SSO windows, the number of power pads will be 3.

Example 4

Your design includes several buses or single I/O which you do not know the SSO window overlap. Then consider all the I/O of your design like a single SSO group and calculate the number of power pad like if all of them were able to switch at the same time (see “Example 2” on page 13.).

Metal Electromigration Considerations

The pin inductance is not the only limitation for the number of power pads. Actually if the inductance can be reduced by bonding several pin package on the same power pad, the power pad has a current limitation due to the electromigration effect.

Due to the risk of metal *electromigration*, each power or ground pad must be limited to a maximum average DC current density.

This values are proportional to the width of Metals which supply power. The following table give the total metal width of each power ring related to the used topmetal layer:

Metal layer	Power rail ring total metal width (µm)								
	VDD	VDDO	VSS	VSSO	AVDD	AVDDO	AVSS	AVSSO	VSS(*)
2lm	10.9	9.1	10	7.4	10.9	8.4	3.2	7.4	-
3lm	-	43.9	-	30.7	-	43.9	-	30.7	-
4lm	31	49.3	30.7	37.9		49.3	8	37.9	17
5lm	-	-	-	-	-		-		-
6lm	31	49.3	30.7	37.9	8	49.3	8	37.9	17

Metal layer	Bonding connection total metal width for different cell types (µm)										
	VDD	VDDO	VSS	VSSO	AVDD	AVDDO	AVSS	AVSSO	VSS(*)	I/O(2)	Direct Input(3)
2lm	34(4)	34(4)	34(4)	34(4)	34(4)	34(4)	34(4)	34(4)	29(4)	27(4)	27(4)
3lm	34(4)	34(4)	34(4)	34(4)	34(4)	34(4)	34(4)	34(4)	29(4)	27(4)	27(4)
4lm	-	-	-	-					-	-	-
5lm	59	59	59	59	59	59	59	59	59	59	59
6lm	-	-	-	-					-	-	-

Note(*): This VSS is in cells supplied by analog power.

Note(2): I/O type refer to all the bidir, tristate, output and inputs buffer cells.
Note(3): This type refer to lower capacitance direct input pad cells.
Note(4): This width is not available all along the IO cell, the width to be considered is the min width between those tagged with this corresponding label "(4)".

The following table give the current limit for power pads. This table assumes that the IO were processed using up to 6 metal layers. The values are given using the table values

according to the main usage of the cell.

Current Limits for Power and Ground Pads

Power Pads			Ground Pads		
Cell Name	Current Limit (mA)		Cell Name	Current Limit (mA)	
	110°C	125°C		110°C	125°C
pvda(1)	95	63	pv0a(1)	95	63
-	-	63	pv0f(1)	95	63
pvdi(2)	95	63	pv0i(2)	95	63
pvdc(2)	95	63	pv0c(2)	95	63
apvda(1)	95	63	apv0a(1)	95	63
apvdi(2)	95	63	apv0i(2)	95	63

Note(1): The value is the min between power rail ring data values and bonding connection total metal width.

Note(2): The value is determined with the bonding connection total metal width that allow to feed the current to the core.

To calculate the number of power pad relative to the electromigration, add the max DC current possible through the power pad using the following table that gives the DC current available in the IO pads for each drive:

DRIVE	DC current I_{OH} (mA) @ Voh=VDDO-0.45V		
	Min	Typ	Max
1 X	-2.188	-3.647	-5.560
2 X	-4.376	-7.294	-11.12
3 X	-6.565	-10.94	-16.68
4 X	-8.754	-14.59	-22.24
5 X	-10.94	-18.24	-27.80

DRIVE	DC current I_{OL} (mA) @ Vol=0.45V		
	Min	Typ	Max
1 X	2.970	5.782	9.254
2 X	5.940	11.56	18.51
3 X	8.910	17.34	27.76

DRIVE	DC current I_{OL} (mA) @ Vol=0.45V		
	Min	Typ	Max
4 X	11.88	23.13	37.02
5 X	14.85	28.91	46.27

The following table gives the maximum number of IO allowed for each pair of PVDA, PV0A to prevent electromigration. The given temperature is the junction temperature and the typical process is considered.

DRIVE	I/O number	
	110°C	125°C
1X	9	6
2X	4	3
3X	3	2
4X	2	1
5X	1	1

Noise Induced Delay In Propagation time.

The *propagation* time that can be found in the data sheet and the models, are characterized assuming that the power generator is delivering a constant voltage value. The introduction of parasitics on the power nodes introduce noise see “The Inductance table” on page 8. This noise associated to the parasitic networks inductance will increase the propagation delay time that is given in the data sheet.

The inductance will introduce it own delay issued from the second order circuit feature. The induced delay is the one due to the of *built-in noise* suppressing feedback circuitry that will reduce the output slew rate following the noise magnitude.

The magnitude of noise is the highest under the best conditions and the lowest under the worst condition process.

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