ANALOG STAGGERED I/O LIBRARY

USAGE

APPLICATION-NOTE

Table 1: Revision History

Revision	Date	Who	Contents
1.0	19-Sep-02	Chuanhai Li Darui Wang	Modified from digital IO to explain the usage of analog lib ASIO220 for Tower

A - How to use this document

The purpose of this application note is to give the user the basic material to use the Synopsys analog library pads.

This document can be read as a flow, or as a list of solution for any issues that you can find. These solutions have been checked in our QA testing flow. This document doesn't intend to reflect all the specific cases related to each design but to provide useful solutions. These solutions might not be optimum for your application.

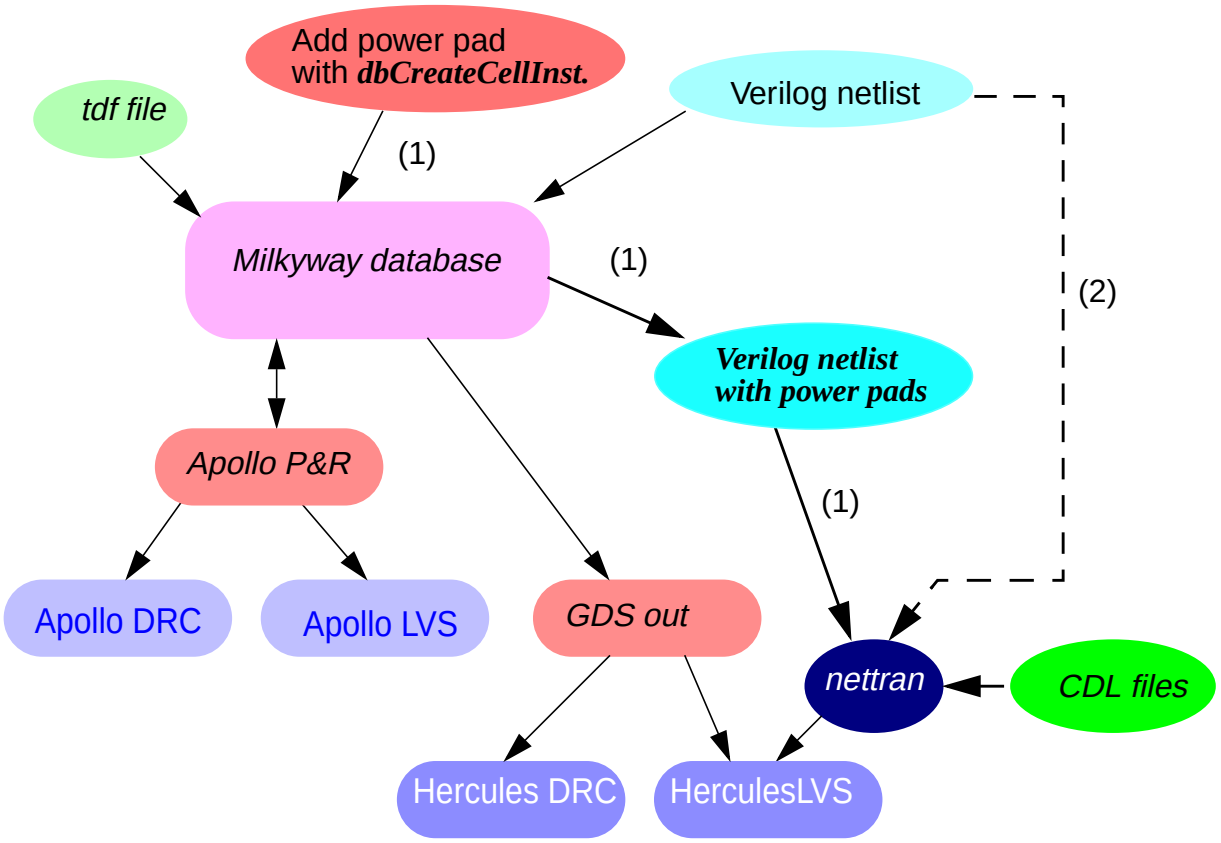
This document is written with the aim to be a generic document independent of the library technology. That is to say this document can be applied to any Synopsys analog library, but does not include specific values for each of them.

In the electronic version of this document, the cross-references are in ***italic red.*** The words that can be found in the index are in ***italic bold.***

B - Design flow

The ***Figure 2.0.0.1*** shows the proposed flow using the IO library.

Figure 2.0.0.1: Proposed flow usage.



The are two options for the Verilog netlist:

-1- pads added in apollo, and new netlist generated including the power pads.

-2- with pads always

The ***Figure 2.0.0.1*** shows both options.

C - Pads types

C.1 Introduction

The analog library that Synopsys provides allows the user to use different IO types:

- ***"I/O pads"***.

- ***"Power pads usages"***

- ***"Corners pads"***

- ***"Pad filler cells"***

The analog library that Synopsys provides does not allow the user to use different power ***buses*** for the IO ring.

There is 2 ***power buses***:

- ***avdd***: standard power bus that can be used in analog block.

- ***avddo***: the ouput power bus (noisy) that can be used in analog block.

The I/Os of the Synopsys digital libraries use three power buses (***vdd vddo vddq***) There is a patent pending on the IO design that allows to reduce the noise on the noisy power bus. More information, please refer to digital library application note.

Synopsys provides in the analog IO library power pads that allow the power buses to be used only in one way: ***"Power pads usages"***

C.2 I/O pads

The I/O pad, input pad, has to be instantiated with the following syntax (explicit declaration of the port):

apc3d01_s IO(.CIN(OUT),.PAD(PAD_apc3d01_s));

This example connects the pin PAD of the input olny cell supplied by analog power apc3d01_s to the node PAD_apc3d01_s.

There is no issue with the regular IO cells, their usage is the same as any other macro block.

C.3 Power pads usages

C.3.1 Optimal solution

In this library apc3d01_s a cell must be used along with the power pads that are provided in this library , ***apvdi_s, apv0i_s, apvda_s, apv0a_s.***

There are , however, limitations that must be noted when placing these cells in the design.Please refer to Sec.D for detail.

C.4 Corners pads

The ***corners*** pad don't appear in the verilog netlist.

They have to be introduce in the design at the cell instantiation step in Apollo. The Synopsys tools, for instance Apollo, allows to create an instance of a cell that is not in the netlist.

The libraries provide only one corner pad that is used for all 4 corners. If a library include 4 corners they will have the same design unless specified in the datasheet.

C.4.1 Creations

The syntax to create the corners pad is the following:

dbCreateCellInst (geGetEditCell) "<library full path name>" "<name of the cell>" "<name of instance>" "<rotation>" "NO" '(coordonnees XY)

This syntax is also available in the Apollo manual.

The instances usually created are:

dbCreateCellInst (geGetEditCell) "tsl18asio220_6lm_fr" "apfrelr_s.FRAM" "cornerll" "270" "NO" '(10 10)

dbCreateCellInst (geGetEditCell) "tsl18asio220_6lm_fr" "apfrelr_s.FRAM" "cornerlr" "0" "NO" '(10 10)

dbCreateCellInst (geGetEditCell) "tsl18asio220_6lm_fr" "apfrelr_s.FRAM" "cornerul" "180" "NO" '(10 10)

dbCreateCellInst (geGetEditCell) "tsl18asio220_6lm_fr" "apfrelr_s.FRAM" "cornerur" "90" "NO" '(10 10)

Note: It is possible to create only the upper left corner cell, Apollo will manage to use this one in the other corners in the correct orientation.

The create corner operation must be done after the binding of the verilog netlist in the Synopsys library (axgBindNetlist).

The placement of the corners pads can be by hand, or they can be included in the tdf file common to the regular IO.

C.5 Pad filler cells

The filler cells do not appear in the verilog netlist.

The filler cells are instantiated in the Apollo tool (see PostPlace menu).

The filler cells must be specified in Apollo in a list from largest to smaller.

The Synopsys IO library uses IO filler to fill the gaps that may exist between two IOs. This solution is adopted by Synopsys to extend the well and the diffusion between the IOs. In the analog block, the filler cells supplied in tsl18asio220 must be used. The IO ring must not be connected using the Apollo route IO ring command.

The filler cells use a numbered naming convention. This number is relative to the width size of the filler. The size and the number of filler cells are depending on the library technology file.

D - IO placement

We are using the appropriate power signal names for all the cells specification.

AVDD for analog 1.8V power

AVSS for analog VSS

AVDDO for analog 3.3V power

AVSSO for analog VSS

VSS for digital VSS

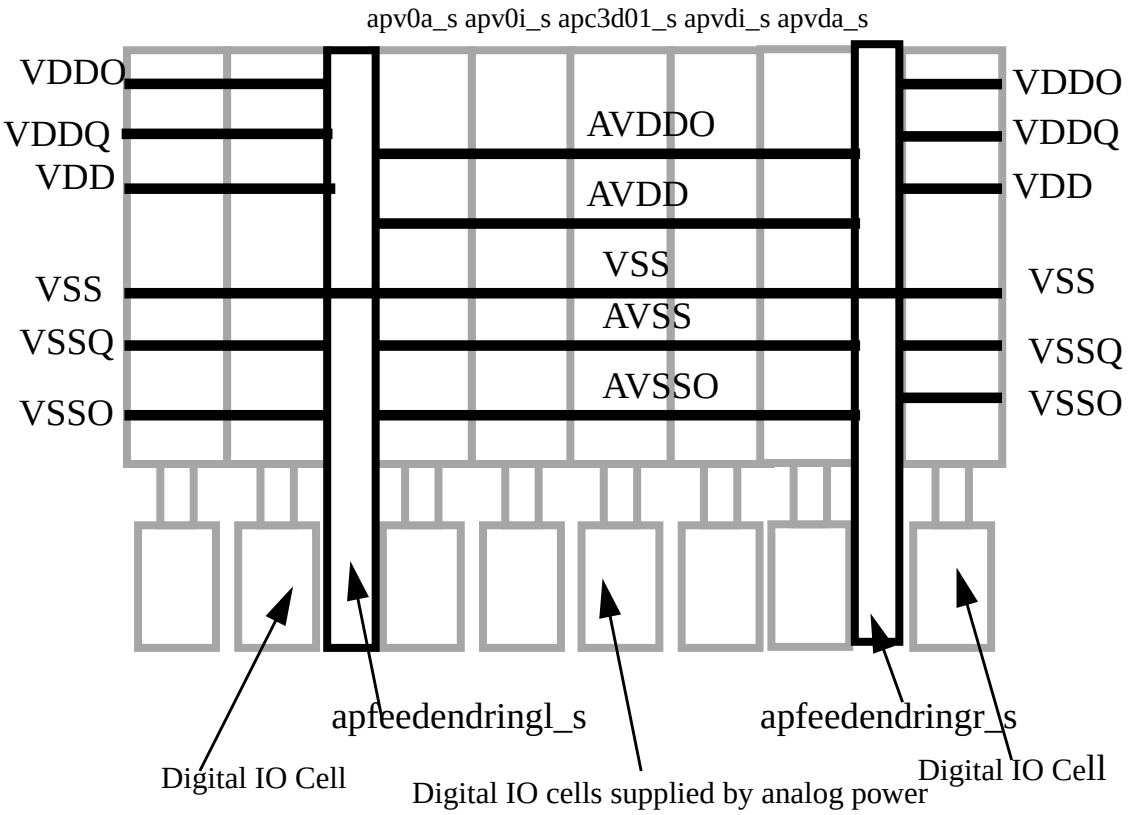
Cut-cells , ***apfeedendringl_s*** and ***apfeedendringr_s*** , are needed in the chip design to buffer the digital section from the analog section as shown in Figure 4.0.0.1,note that the continuous connection of the VSS power rail in the digital as well as the analog section, this configuration is used for good ESD integration.

Configuration in Figure 4.0.0.1 is strongly recommended. Fail to do so might have DRC message during verification process. Please contact Synopsys or refer to sec.D.1 should this DRC error happened.

Synopsys suggests that it is better to put the digital VSS pad (pv0i_s) close enough to the cut-cell.This is for good ESD performance.

All other information about IO placement please refer to the application note of digital IO.

Figure 4.0.0.1:Implementation Proposal



D.1 IO Placement Limitation

In the mix-signal design, digital noise must be isolated from the analog section. This is illustrated in Figure 4.0.0.1. Non-abutting the cut-cell at either side might introduce unwanted noise coupling between the digital and the analog sections for possible design failure. To prevent this ill design from happing , all cells in tsl18asio220 library have used a thin metal2 width of 0.14µ that was built in the cell, thereby, non-abutted side will have DRC for a head up.

Please contact Synopsys should this waving flag is a difficulty for your design.