Number of printed pages 02

Semester VI (B.Tech.)

Er. No.....

Academic Year: 2021-22

Jaypee University of Engineering & Technology, Guna

T-3 (Even Semester 2022)

18B11CI414 – COMPUT. . ORGANIZATION AND ARCHTECTURE

Maximum Duration: 2 Hours

Maximum Marks: 35

Notes:

1. This question paper has **6** questions.
2. Write relevant answers only.
3. Do not write anything on question paper (Except your Er. No.).

			Marks
Q1.	**(a)**	Show that the maximum speed-up factor in ideal pipeline architecture equals to the number of segments of the architecture.	**[02]**
	(b)	Consider four segment pipeline architecture with segment delays of 120, 55, 170 and 60 ns respectively. Registers used between the segments have a delay of 10 ns each. (i) How many instructions can be executed i 0 ms? (ii) What will be the speed-up factor in comparison to non-pipelined architecture? (iii) How can we reduce the total time to about one-third of the time calculated in part (i)?	**[04]**
Q2.	**(a)**	Write at least four differences between HDD and SSD of computer systems.	**[02]**
	(b)	In 80 GB hard disk, there are total of 10 disks with 50 tracks in each disk. How many sectors will be in each track if the storage capacity of a sector is 5 MB? Find the total time to read a file of 6400 MB if rotational speed of disk is 7200 rpm. Consider average seek time 4 ms.	**[04]**
Q3.	**(a)**	Compare SRAM and DRAM with at least four properties.	**[02]**
	(b)	A computer employs RAM chips of size 512 x 16 and ROM chips of size 1024 x 16. The computer system needs total storage capacity of 4KB of RAM and 2KB of ROM. (i) Draw a block diagram of required architecture of memory system. (ii) Find address maps (range) in hexadecimal for RAM and ROM.	**[04]**
Q4.	**(a)**	Show three-level cache memory organization connected with main memory and CPU. Explain working principle of cache memory briefly.	**[02]**
	(b)	Suppose in 5000 memory references, there are 200 misses in L1 cache and 50 misses in L2 cache. If the miss penalty of L2 is 1000 clock cycles, hit time of L1 is 5 clock cycle, and hit time of L2 is 75 clock cycles. Consider system uses clock rate of 2.5 GHz.	**[04]**

(i) Find the average access time of L1 cache.
(ii) Calculate the average access time of L2 cache.
(iii) What will be the overall average cache memory access time?

Q5. (a) Describe the features of various cache memory mappings. [02]

(b) In direct cache memory mapping, 3-bits are in each field of tag bits, block bits, and word bits. If the CPU accesses four physical addresses 001 010 000; 001 010 010; 001 100 010; 001 010 111 sequentially. [04]
(i) Find the number of blocks in main memory and cache memory.
(ii) Which of the blocks of main memory can reside in block-3 of cache memory?
(iii) What will be miss ratio?

Q6. (a) Find the logical (virtual) address to access word number 255 from page number 15 of segment 36. If virtual space contains total of 128 segments, each segment of 32 pages and 4K words in each page. [02]

(b) In a virtual memory system, eight pages are accessed by the CPU sequentially in the order of 2, 1, 2, 0, 3, 6, 4, 5, 3, 0, 7 using least recently used (LRU) algorithm. Assume there are four blocks in the main memory. [03]
(i) Find the total number of page faults.
(ii) What will be the hit ratio?