Semester VI (B.Tech.)

Number of printed pages 2
Er. No. 20.1.B.208...
Academic Year: 2022-23

Jaypee University of Engineering & Technology, Guna

T-3 (Even Semester 2023)

18B11CI414 – COMPUTER ORGANISATION AND ARCHITECTURE

Maximum Duration: 2 Hours **Maximum Marks: 35**

Notes:

1. This question paper has **5** questions.
2. Write relevant answers only.
3. Do not write anything on question paper (Except your Er. No.).

			Marks	**CO No.**
Q1.	**(a)**	Draw space-time diagram for four-segment pipelined and non-pipelined architectures showing the time it takes to process 6 tasks. What will be the speed-up factor for the pipelined architecture with respect to non-pipelined architecture?	**[03]**	**CO2**
	(b)	Consider four segments in a pipelined processor with segment time 55ns, 75ns, 25ns, and 45ns. The interface registers delay is 5ns. a. Calculate the minimum clock cycle time required in the system. b. How long it would take to complete 200 tasks with pipelined processor? c. Calculate speedup of the pipeline for 200 tasks. d. What is the maximum speed-up that can be achieved with four segment pipeline? e. How can we reduce the total time to about one-third of the time calculated in part (b)?	**[05]**	**CO3**
Q2.		Consider a hard disk with 4 surfaces, average seek time of 4 ms, rotational speed of 15000 rpm, 500 sectors per track and each sector of 1k bytes. a. How much time it will take to traverse one track? b. What is the rotational latency? c. Find number of cylinders it takes to store 2MB data stored in total of 2500 sectors? d. How much data it can transfer in a single rotation? e. Estimate the time required to transfer a 2MB file if data is stored in contiguous sectors and tracks? f. What is the data transfer rate in kB/second?	**[06]**	**CO5**
Q3.	**(a)**	A virtual memory system has an address space of 8k words, a memory space of 4k words, and page sizes of 1k words. Find the number of page faults for FIFO and LRU page replacement algorithms with page access sequence of 4 1 0 1 2 6 1 4 0 1 0 2 4 5 7.	**[04]**	**CO4**
	(b)	The memory access time is 2 nsec for a read operation with a hit in cache, 6 nsec for a read operation with a miss in cache, 4 nsec for a write operation with a hit in	**[03]**	

cache, and 10 nsec for a write operation with a miss in cache. The execution of a sequence of instructions involves 1600 instruction fetch operations, 600 memory operand read operations, and 800 memory operand write operations. The cache hit ratio is 0.9. Find the average memory access time (in nanoseconds) in executing the sequence of instructions.

Q4. In direct cache memory mapping, 3-bits are in each field of tag bits, block bits and word bits. If CPU accesses five physical addresses 001 010 000; 001 010 010; 001 100 010; 001 010 111; 001 010 111 sequentially. **[07]** **CO5**

a. Find the number of blocks in main memory.
b. How many total words can be there in cache memory?
c. Which blocks of main memory can reside in block-3 of cache memory?
d. What will be hit ratio?
e. Calculate the hit ratio if cache memory uses fully associative mapping.

Check

Q5. An 8-bit computer employs RAM and ROM chips of size 4096x8 and 1024 x8 respectively. The computer system needs total of 8KB of RAM and 2KB of ROM. **[07]** **CO4**

a. Find the number of RAM and ROM chips is needed in the design?
b. How many lines will be common to RAM and ROM chips?
c. Draw a block diagram of required architecture of memory system.
d. Obtain the address maps (range) in hexadecimal for RAM and ROM chips of the system.
e. How many address maps are possible for RAM and ROM chips?