

**Jaypee University of Engineering & Technology, Guna****T-2 (Odd Semester 2023)****18B11EC311 - Digital Systems and Microprocessor**

Maximum Duration: 1 Hour 30 Minutes

Maximum Marks: 25

Notes:

1. This question paper has five questions.
2. Write relevant answers only in proper order.
3. Do not write anything on question paper (Except your Er. No.).

		Marks	CO Number(s) description
Q1.	Minimize the following and implement the reduced expression using NAND gates. $F(A, B, C, D) = \sum m(1, 3, 4, 6, 8, 9, 11, 13, 15)$ $d(A, B, C, D) = \sum d(0, 2, 14)$	[05]	CO3
Q2.	Explain and draw the following for full adder circuit: (a) Logic circuit and truth table (b) Circuit diagram using two half adders and OR gate	[05]	CO4
Q3.	Design a 3-bit lookahead adder with carry generator circuit. How it speeds up the addition process.	[05]	CO5
Q4. (a)	Design a comparator, which compares the magnitude of two numbers X and Y, each consisting of two bits and giving three outputs $F_1$ , $F_2$ and $F_3$ such that: $F_1 = 1$ , if $X > Y$ $F_2 = 1$ , if $X = Y$ $F_3 = 1$ , if $X < Y$	[03]	CO5
(b)	Design a combinational circuit with three inputs and one output for the condition given as, (a) The output is 1 when the binary value of the inputs is less than or equal to 4. The output is 0 otherwise. (b) The output is 1 when the binary value of the inputs is an even number.	[02]	
Q5. (a)	Construct $F(A, B, C, D) = \sum m(1, 3, 5, 6, 8, 9, 12, 14, 15)$ function using, (a) One 8x1 multiplexer (using A, B, D as select lines) (b) 16x1 multiplexer	[03]	CO2
(b)	Draw a 4-to-16 line decoder using suitable number of 2-to-4 line decoder.	[02]	