Project 4: Full UART
Chip Specification

Version 1.0

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CECS 460

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Version History

Version #	Implemented By	Revision Date	Approved By	Approval Date	Reason
1.0	Vince Nguyen	*5/15/2020*	Vince Nguyen	*5/18/2020*	Initial Design Definition Draft

Table of Contents

1 Introduction

This chip specification template is intended to be the completion of CSULB's senior level final project for CECS 460, assigned for the Spring 2020 semester.

1.1 Purpose

The purpose of this document is to specify the requirements of the communication protocol Universal Asynchronous Receiver Transmitter (UART).

2 Documents

This section describes the principles and strategies to be used as guidelines when designing and implementing the system.

2.1 Applicable External Documents

2.1.1 PicoBlaze 8-bit Embedded Microcontroller User Guide

2.2 Applicable Internal Documents

2.2.1 Programming the TramelBlaze Using Assembly Code

2.2.2 TramelBlaze Assembly Tutorial 2020

3 Requirements

This project shall combine the full UART with the TramelBlaze processor. When working, the project shall follow the following special requests:

- A <CR> shall send the cursor to the start of the next line and should refresh the prompt.
- A <BS> shall erase the character in front of the cursor.
- An “*” shall result in the displaying of my hometown “Costa Mesa, CA”, followed by a new line and a prompt.
- An “@” will result in outputting of the number of characters received followed by a new line and a prompt.
- If a character is entered and doesn't follow the following requirements, it shall be echoed up to 40 times.

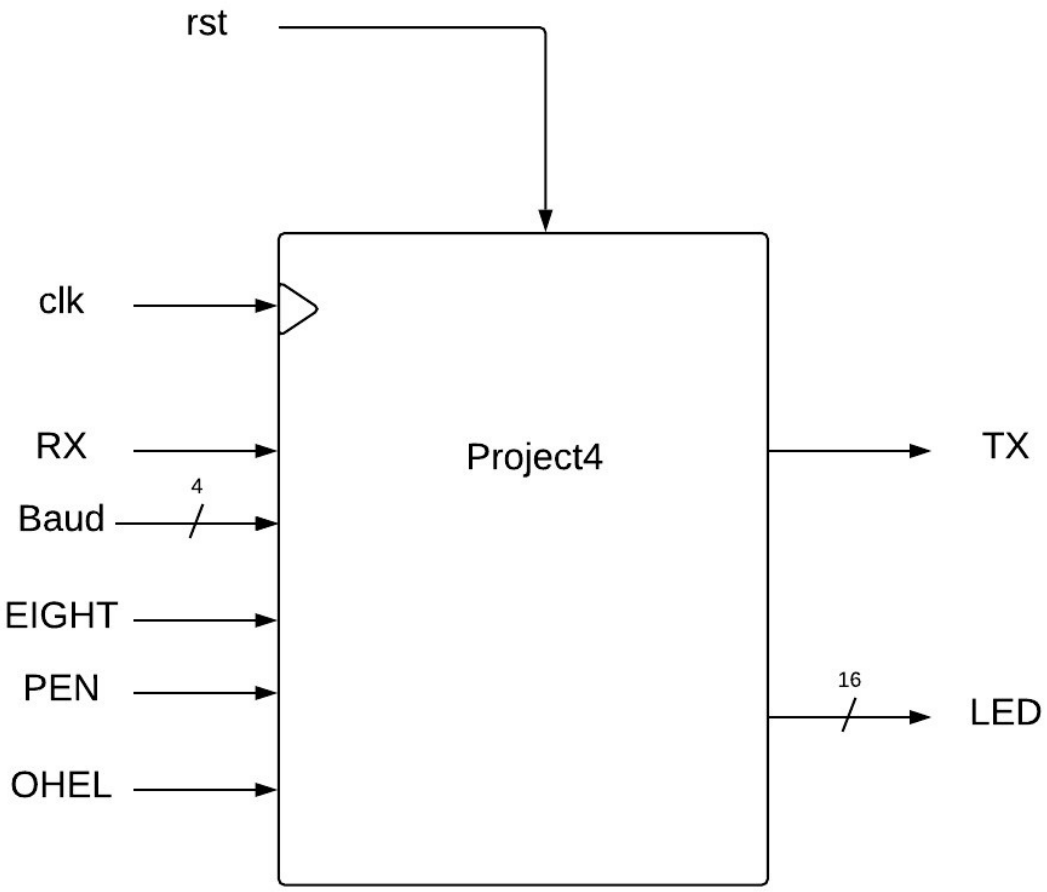
4 Top Level Design

4.1 Description

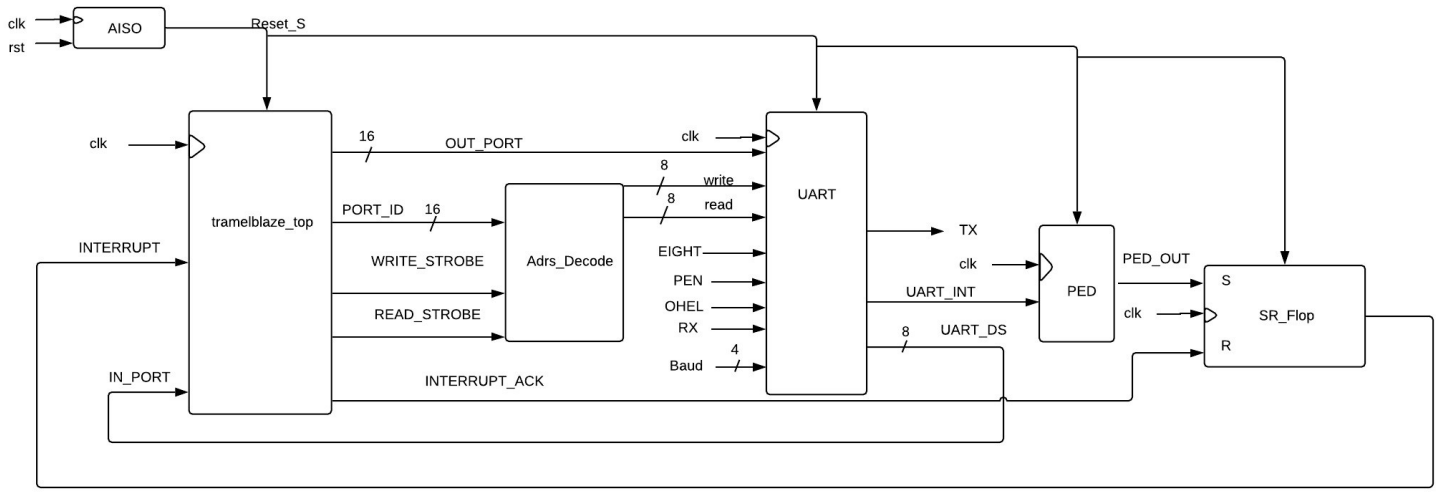
The top level is designed with six blocks, including the TramelBlaze processor and the UART block.

4.2 Block Diagrams

4.2.1 Top Block Diagram



4.2.2 Top Level Schematic



4.3 Data Flow Description

All sequential blocks receive the same clock signal of 100MHz. When a reset is asserted, the output of AISO will synchronously send out a reset signal to all other sequential blocks. The system will start with the execution of Assembly code within the TramelBlaze processor. Based on the output of the TramelBlaze processor, the Adrs_Decode block will determine the actions of the UART. The switches are distributed amongst the Baud decode inputs, EIGHT, PEN, and OHEL.

4.4 I/O

4.4.1 Signal Names

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator
Rst (reset)	1	Input	Brings all signals to a known state. Driven by onboard push button.
EIGHT	1	Input	Determine the number of bits that will be transmitted from the Transmit Engine. Driven by onboard switch.
PEN	1	Input	Determines if a parity bit will be sent along with the data from the Transmit Engine to the Receive Engine. Driven by onboard switch.
OHEL	1	Input	Determine the state of the parity bit that will be transmitted from the Transmit Engine and received from the Receive Engine. Driven by onboard switch.
RX	1	Input	Signal sent in from pin C4 on the board
Baud	4	Input	Determines the frequency at which data is transferred. Driven by onboard switches.
TX	1	Output	Data that is being sent out bit by bit. Determined by the least significant bit in the shift register.
LED	16	Output	Shows data from the TramelBlaze to give a visual to the user that indicates that there is data being transferred.

4.4 I/O

4.4.2 Pin Assignments

Inputs:

Name	Pin Assignment
Clk	E3
Rst	M18
EIGHT	R15
PEN	M13
OHEL	L16
RX	C4
Baud[3]	R13
Baud[2]	U18
Baud[1]	T18
Baud[0]	R17

Outputs:

Name	Pin Assignment
TX	D4
LED[15]	V11
LED[14]	V12
LED[13]	V14
LED[12]	V15
LED[11]	T16
LED[10]	U14
LED[9]	T15
LED[8]	V16
LED[7]	U16
LED[6]	U17
LED[5]	V17
LED[4]	R18
LED[3]	N14
LED[2]	J13
LED[1]	K15
LED[0]	H17

4.4.3 Electrical Characteristics

N/A

4.5 Clocks

The only clock used for the project is the 100MHZ clock (pin E3) on the Nexys 4 DDR FPGA board.

4.6 Resets

The reset button is located at the “up” button (pin M18) on the board.

4.7 Software

Software was written in Verilog using the Xilinx Vivado 2019.1. The logic for the TramelBlaze processor was written in Verilog. The .coe file used for the processor was generated using the .tba Assembly file.

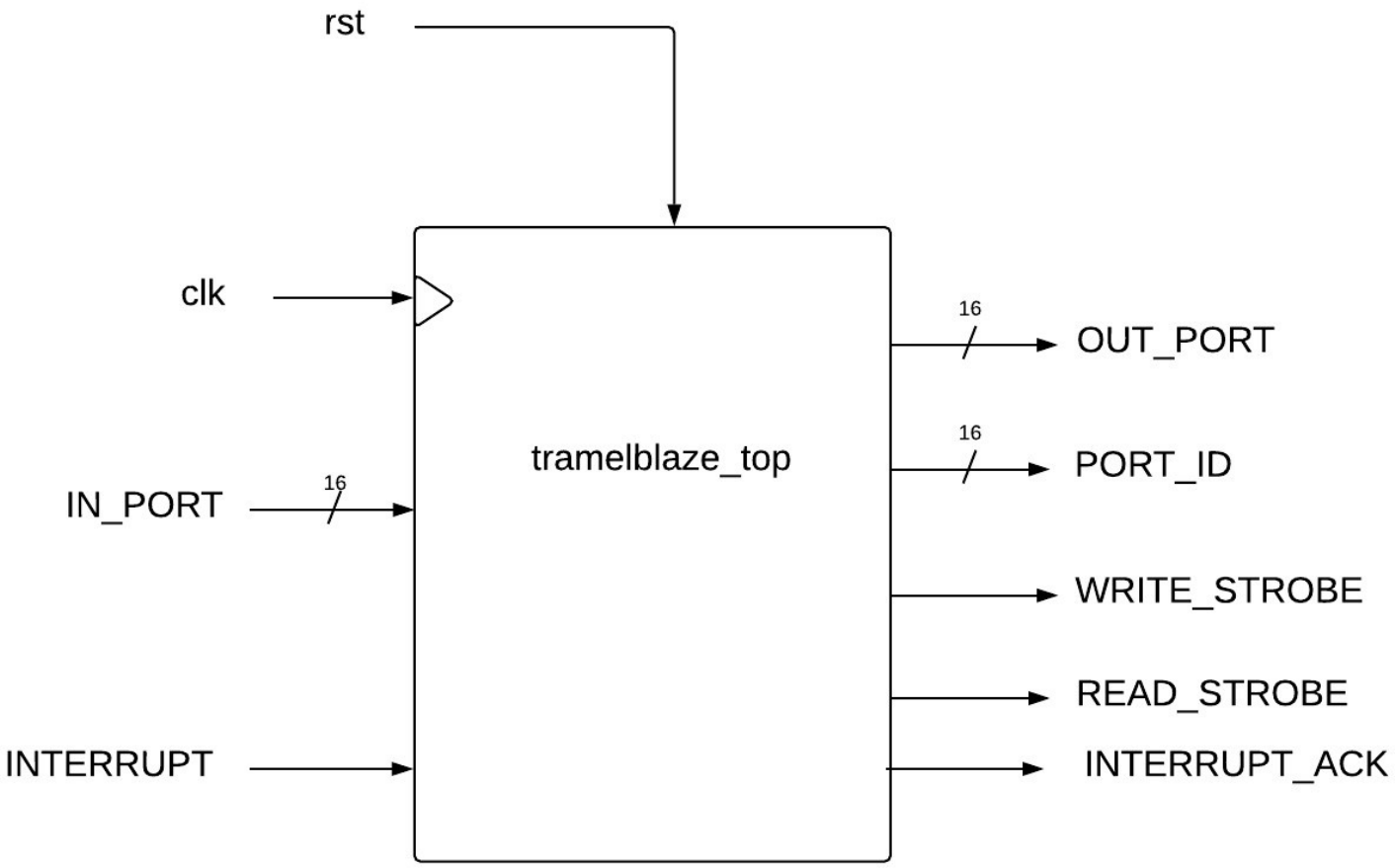
5 Externally Developed Blocks

5.1 TramelBlaze Top Module (tramelblaze_top.v)

5.1.1 Description

The TramelBlaze Top module instantiates the TramelBlaze processor.

5.1.2 Block Diagram



5.1.3 I/O

Signal Name	Bit Size	Input/Output	Description
CLK(clock)	1	Input	Driven by 100MHz crystal oscillator
RESET	1	Input	Brings all signals to a known state. Driven by onboard push button.
IN_PORT	16	Input	Inputs the data that is being read by the
INTERRUPT	1	Input	Tells the TramelBlaze to execute the Interrupt
OUT_PORT	16	Output	Outputs the data that is to be written from the TramelBlaze.
PORT_ID	16	Output	Outputs the address location at which the data is to
READ_STROBE	1	Output	Signals when the TramelBlaze should read data from
WRITE_STROBE	1	Output	Signals when the TramelBlaze should write data to a
INTERRUPT_ACK	1	Output	Signals when the TramelBlaze has received an

5.1.4 Register Map

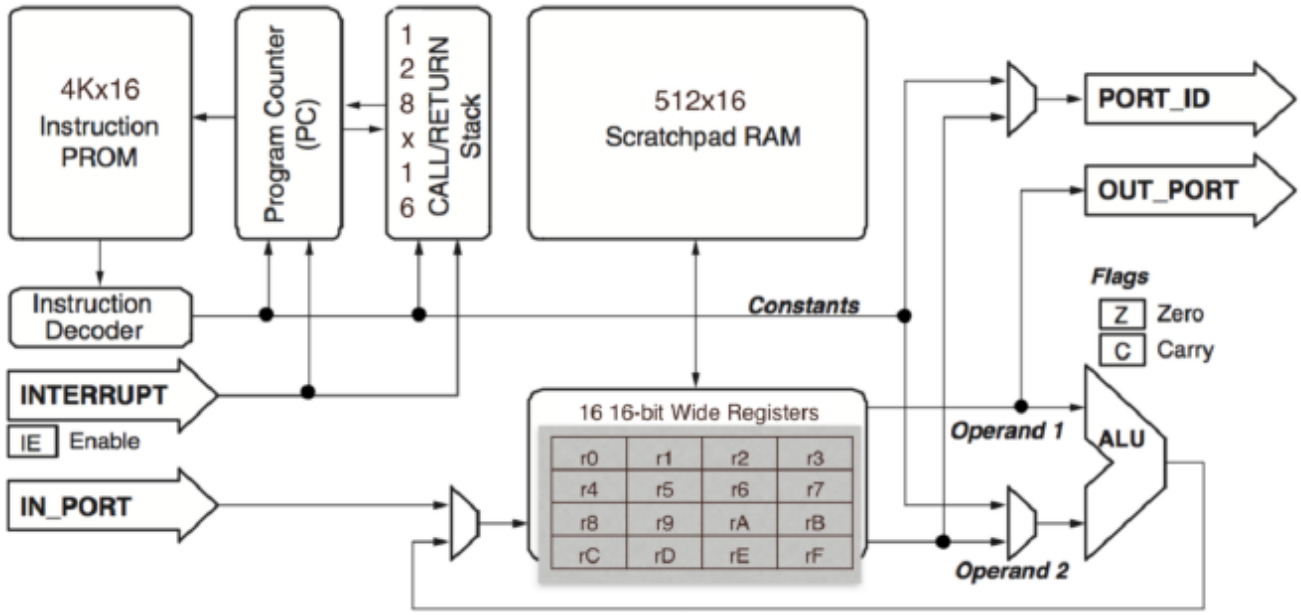
N/A

5.2 TramelBlaze Processor (tramelblaze.v)

5.2.1 Description

The TramelBlaze processor is a sixteen-bit soft core processor designed to emulate the eight-bit PicoBlaze open core from Xilinx.

5.2.2 Block Diagram



5.2.3 I/O

Signal Name	Bit Size	Input/Output	Description
CLK(clock)	1	Input	Driven by 100MHz crystal oscillator
RESET	1	Input	Brings all signals to a known state. Driven by onboard push button.
IN_PORT	16	Input	Inputs the data that is being read by the TramelBlaze.
INTERRUPT	1	Input	Tells the TramelBlaze to execute the Interrupt Service Routine (ISR).
OUT_PORT	16	Output	Outputs the data that is to be written from the TramelBlaze.
PORT_ID	16	Output	Outputs the address location at which the data is to be either input or output.
READ_STROBE	1	Output	Signals when the TramelBlaze should read data from a location.
WRITE_STROBE	1	Output	Signals when the TramelBlaze should write data to a location.
INTERRUPT_ACK	1	Output	Signals when the TramelBlaze has received an Interrupt.
ADDRESS	12	Output	Address to instruction memory (ROM).
INSTRUCTION	16	Input	Executable directives from instruction memory (ROM).

5.2.4 Register Map

Register Name	Purpose	Description
R0-RF	Hold user data from IN_PORT	Sixteen 16-bit registers that hold data to be used for operations and outputting data.
Z	Flags if value is zero	One-bit flag
C	Flags if there is a carry	One-bit flag
IE	Flags if interrupt is enabled	One-bit flag

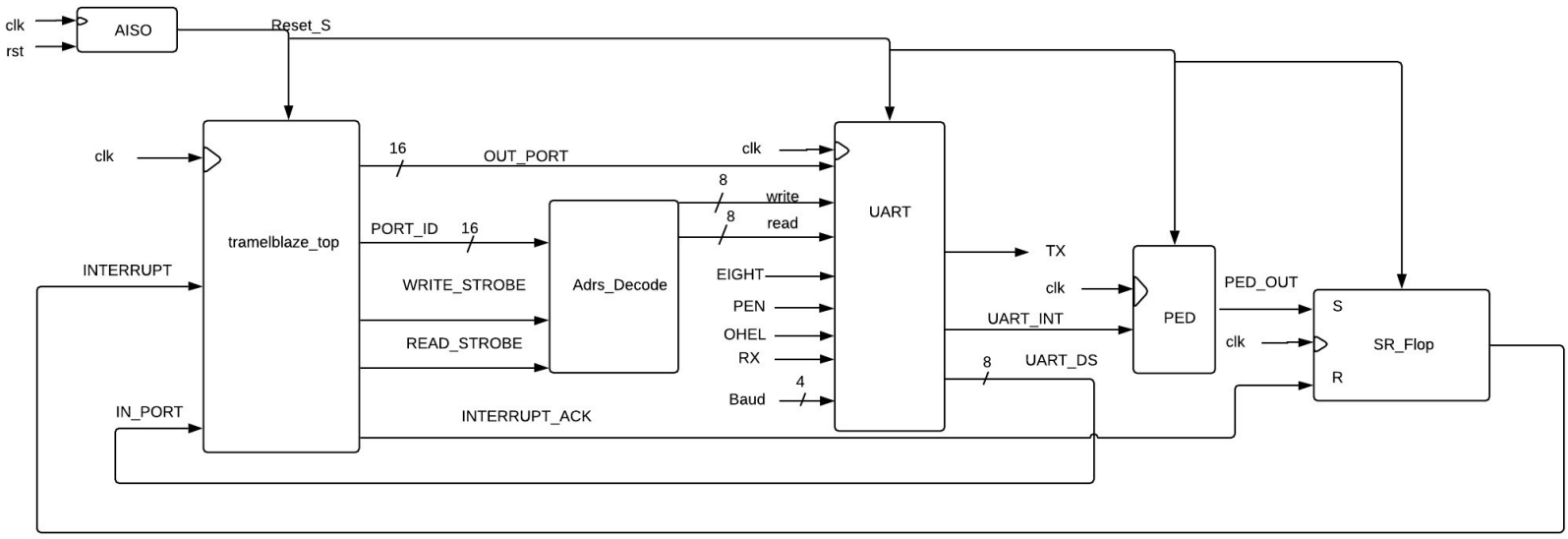
6 Internally Developed Blocks

6.1 Top Level Module (project4.v)

6.1.1 Description

The Top Level Module instantiates all the necessary components needed for interactions between the TramelBlaze processor and the UART. This module will be used for implementation onto the Nexys 4 DDR FPGA board.

6.1.2 Block Diagram



6.1.3 I/O

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator
Rst (reset)	1	Input	Brings all signals to a known state. Driven by onboard push button.
EIGHT	1	Input	Determine the number of bits that will be transmitted from the Transmit Engine. Driven by onboard switch.
PEN	1	Input	Determines if a parity bit will be sent along with the data from the Transmit Engine to the Receive Engine. Driven by onboard switch.
OHEL	1	Input	Determine the state of the parity bit that will be transmitted from the Transmit Engine and received from the Receive Engine. Driven by onboard switch.
RX	1	Input	Signal sent in from pin C4 on the board
Baud	4	Input	Determines the frequency at which data is transferred. Driven by onboard switches.
TX	1	Output	Data that is being sent out bit by bit. Determined by the least significant bit in the shift register.
LED	16	Output	Writes data sent from the TramelBlaze processor. Written to address 0002.

6.1.4 State Machines

N/A

6.1.5 Register Map

Register Name	Purpose	Description
LED	Holds data written to address 0002 from TramelBlaze Processor.	Holds data when address 0002 is written to.

6.1.6 Verification

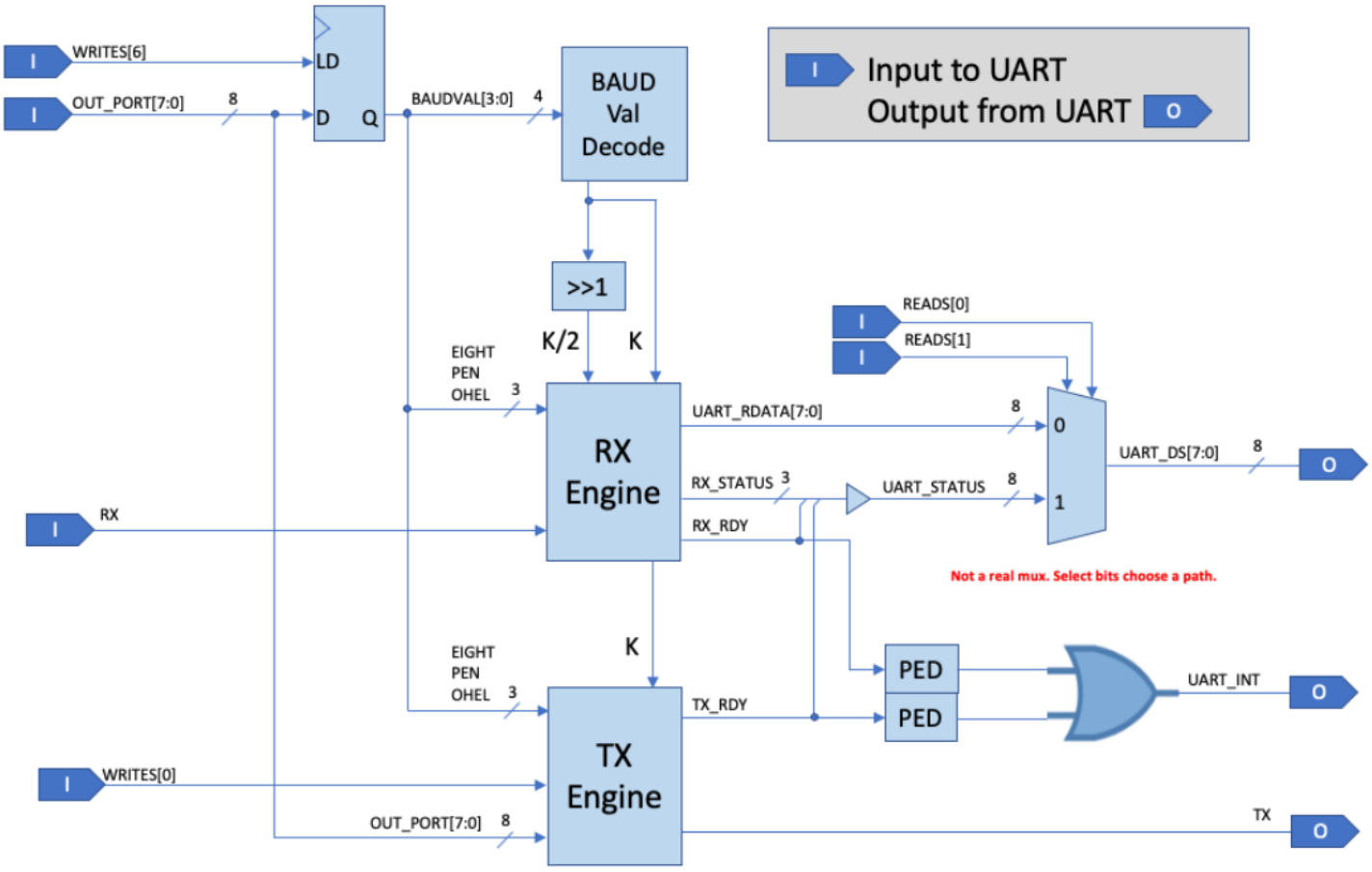
N/A

6.2 UART (UART.v)

6.2.1 Description

The Universal Asynchronous Receiver Transmitter (UART) is designed to take onboard switch inputs and generate data and interrupts to be sent to the INTERRUPT port on the TramelBlaze Processor.

6.2.2 Block Diagram



6.2.3 I/O

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator
Rst (reset)	1	Input	Brings all signals to a known state. Driven by onboard push button.
EIGHT	1	Input	Determine the number of bits that will be transmitted from the Transmit Engine. Driven by onboard switch.
PEN	1	Input	Determines if a parity bit will be sent along with the data from the Transmit Engine to the Receive Engine. Driven by onboard switch.
OHEL	1	Input	Determine the state of the parity bit that will be transmitted from the Transmit Engine and received from the Receive Engine. Driven by onboard switch.
RX	1	Input	Signal sent in from pin C4 on the board
Baud	4	Input	Determines the frequency at which data is
Write	1	Input	Sent into the Tx Engine acting as a load signal.
Read	2	Input	Used to determine status of UART_DS. Read[0] is sent into the RX Datapath to determine status flags.
OUT_PORT	16	Input	Data to be transmitted out via the shift register.
TX	1	Output	Data that is being sent out bit by bit. Determined
UART_INT	1	Output	Sends an interrupt signal to the TramelBlaze. Determined by a logic OR gate with the inputs of
UART_DS	8	Output	Data/Status. Determined by a multiplexor depending on the read inputs.

6.2.4 State Machines

N/A

6.2.5 Register Map

Register Name	Purpose	Description
UART_DS	Holds either data or status to be displayed	Eight-bit register that holds data if read[0] signal is high or if read [1] signal is high. Holds zero value otherwise.

6.2.6 Verification

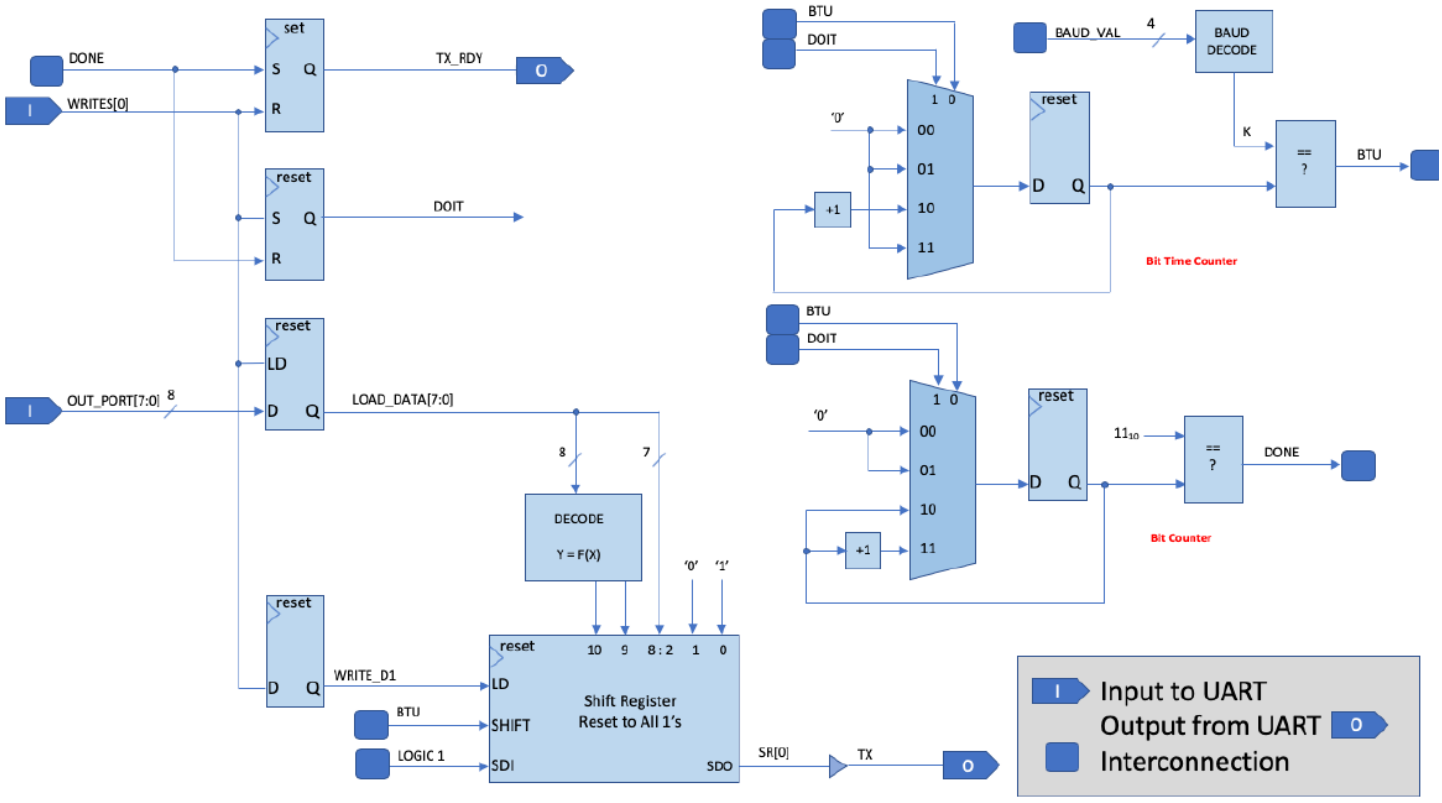
N/A

6.3 Transmit Engine (Tx_Engine.v)

6.3.1 Description

The Transmit Engine is a block in the UART designed to transmit data that is generated by the TramelBlaze. It outputs a one-bit wide signal based on the TramelBlaze data. Data is sent out via a shift register that outputs start, data (starting with the least significant bit first), the parity bit (if PEN is high), stop bit, and the mark bits.

6.3.2 Block Diagram



6.3.3 I/O

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator
Rst (reset)	1	Input	Brings all signals to a known state. Driven by onboard push button.
EIGHT	1	Input	Determine the number of bits that will be transmitted from the Transmit Engine. Driven by onboard switch.
PEN	1	Input	Determines if a parity bit will be sent along with the data from the Transmit Engine to the Receive Engine. Driven by onboard switch.
OHEL	1	Input	Determine the state of the parity bit that will be transmitted from the Transmit Engine and received from the Receive Engine. Driven by onboard switch.
Baud	4	Input	Determines the frequency at which data is transferred. Driven by onboard switches.
Write	1	Input	Determines state of TXRDY and LD.
OUT_PORT	16	Input	Data to be transmitted out via the shift register.
TX	1	Output	Data that is being sent out bit by bit. Determined by the least significant bit in the shift register.
TXRDY	1	Output	Signals when the Transmit Engine is ready to transmit data. Determined by the status of Write

6.3.4 State Machines

N/A

6.3.5 Register Map

Register Name	Purpose	Description
TXRDY	Holds status flag of TX	SR flop that is high if reset or DONE are high, low if Write is high.
Do_it	Holds value for doit signal	SR flop that is high if Write is high, low if rst or DONE is high.
Out_port	Holds value for data	Eight-bit D flop that holds data from OUT_PORT.
Flipflop	Holds value for LD	One-bit flop that gets the value of Write.

6.3.6 Verification

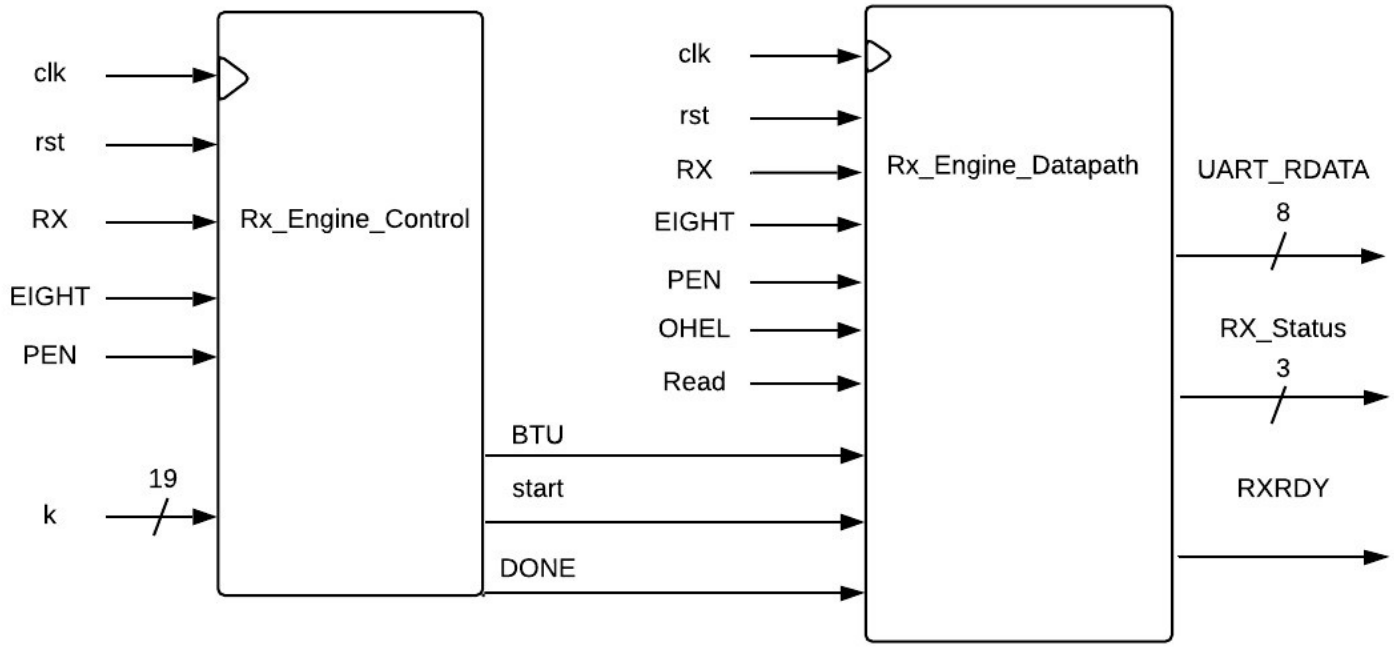
N/A

6.4 Receive Engine (Rx_Engine.v)

6.4.1 Description

The Receive (Rx) Engine is a block in the UART designed to receive data that is generated by the TramelBlaze and sent by the Transmit Engine. The Rx block combines the Rx Engine Control and the Rx Engine Datapath.

6.4.2 Block Diagram



6.4.3 I/O

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator
Rst (reset)	1	Input	Brings all signals to a known state. Driven by onboard push button.
EIGHT	1	Input	Determine the number of bits that will be transmitted from the Transmit Engine. Driven by onboard switch.
PEN	1	Input	Determines if a parity bit will be sent along with the data from the Transmit Engine to the Receive Engine. Driven by onboard switch.
OHEL	1	Input	Determine the state of the parity bit that will be transmitted from the Transmit Engine and received from the Receive Engine. Driven by onboard switch.
RX	1	Input	Data sent into the shift register. Driven by pin C4.
Baud	4	Input	Determines the frequency at which data is transferred. Driven by onboard switches.
Read	1	Input	Data sent into the four SR flops in the Rx Engine Datapath determined by the address decoder in the top module.
UART_RDATA	8	Output	Data that is being sent out bit by bit. Determined by the least significant bit in the shift register.
RX_Status	5	Output	Data that is being sent out bit by bit. Determined by the least significant bit in the shift register.
RXRDY	1	Output	Signals when the Rx Engine is ready to receive data. Determined by the status of BTU, doit, EIGHT, and PEN.

6.4.4 State Machines

N/A

6.4.5 Register Map

N/A

6.4.6 Verification

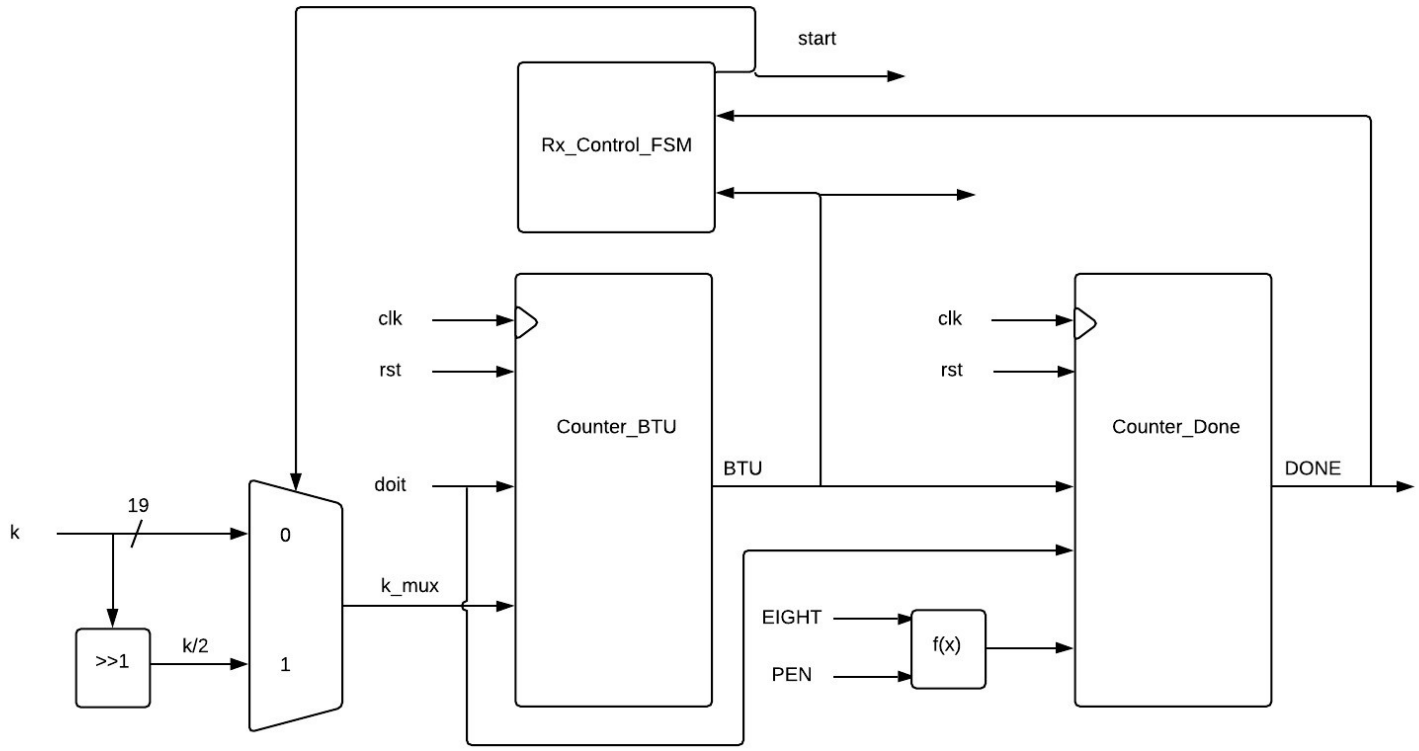
N/A

6.5 Receive Engine Control (Rx_Engine_Control.v)

6.5.1 Description

The Receive Engine Control is comprised of 3 main blocks: BTU counter, Done counter, and the finite state machine. The purpose of this module is to generate a start, BTU, and DONE signals. These signals will then be used in the rest of the design.

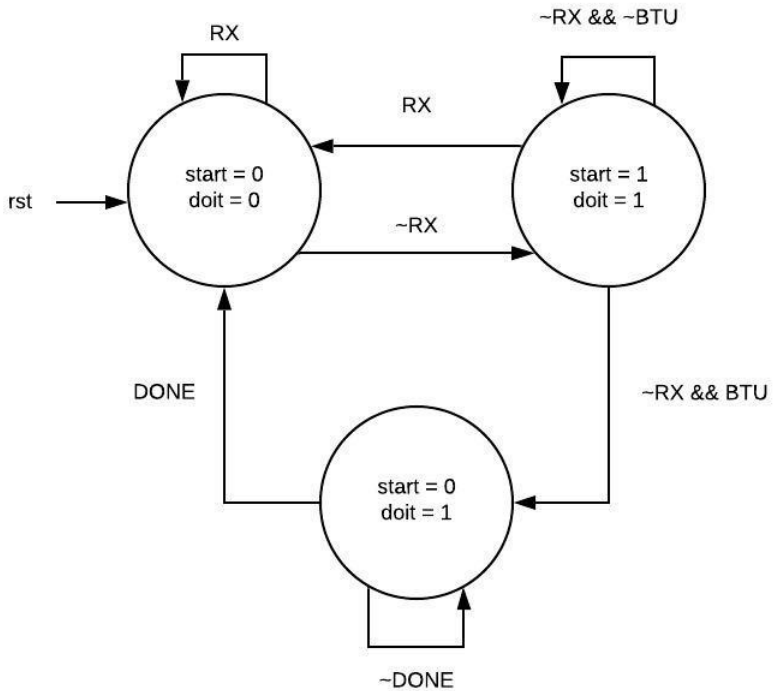
6.5.2 Block Diagram



6.5.3 I/O

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator
Rst (reset)	1	Input	Brings all signals to a known state. Driven by onboard push button.
EIGHT	1	Input	Determine the number of bits that will be transmitted from the Transmit Engine. Driven by onboard switch.
PEN	1	Input	Determines if a parity bit will be sent along with the data from the Transmit Engine to the Receive Engine. Driven by onboard switch.
k	19	Input	The frequency at which data is transferred. Driven by onboard switches from Baud decoder module.
BTU	1	Output	Signals when a bit has been active as long as the bit is specified to be.
start	1	Output	Signals when the Rx Engine Control is ready to start processing data.
DONE	1	Output	Signals when the Rx Engine Control is finished processing data.

6.5.4 State Machines



6.5.5 Register Map

Register Name	Purpose	Description
state	Holds status of which state the Finite State Machine is currently residing in.	Finite State Machine location that determines the next outputs based on the current state.
start	Holds value for start signal	Finite State Machine output based on the current state.
doit	Holds value for doit signal.	Finite State Machine output based on the current state.

6.5.6 Verification

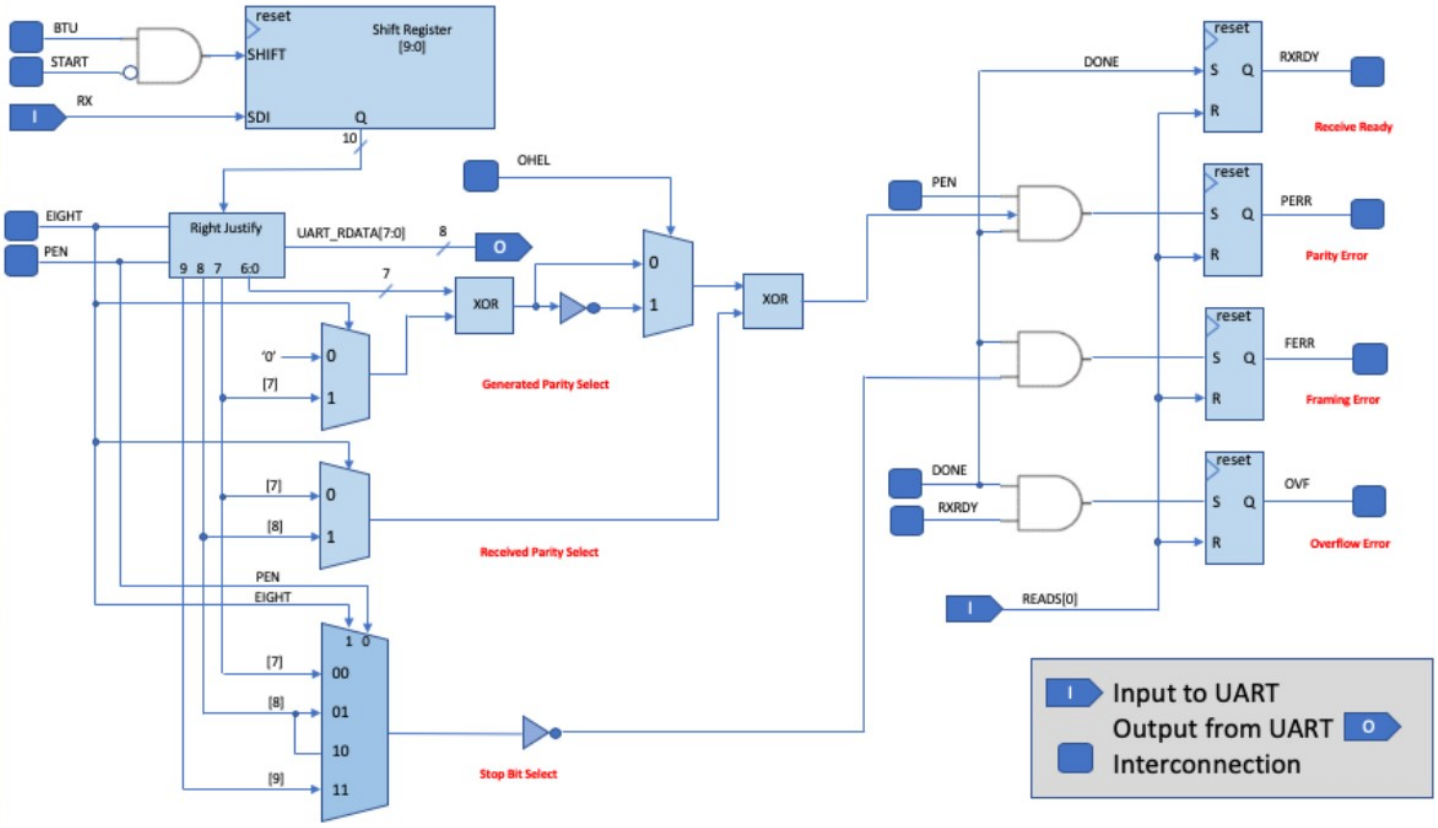
N/A

6.6 Receive Engine Datapath (Rx_Engine_Datapath.v)

6.6.1 Description

The Receive Engine Datapath creates the layout for where the received data signal will go. The received data will be displayed on a terminal. The received data will also determine the status flags for the UART.

6.6.2 Block Diagram



6.6.3 I/O

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator
Rst (reset)	1	Input	Brings all signals to a known state. Driven by onboard push button.
EIGHT	1	Input	Determine the number of bits that will be transmitted from the Transmit Engine. Driven by onboard switch.
PEN	1	Input	Determines if a parity bit will be sent along with the data from the Transmit Engine to the Receive Engine. Driven by onboard switch.
OHEL	1	Input	Determine the state of the parity bit that will be transmitted from the Transmit Engine and received from the Receive Engine. Driven by onboard switch.
RX	1	Input	Data being brought in and sent into the shift register. Driven by pin C4.
BTU	1	Input	Signals when a bit has been active as long as the bit is specified to be.
start	1	Input	Signals when the Rx Engine Datapath has no data to be processed. Signal is low active in this
Read	1	Input	Determining factor in the status of RXRDY, PERR, FERR, and OVF registers.
DONE	1	Input	Determining factor in the status of RXRDY, PERR, FERR, and OVF registers.
RXRDY	1	Output	Signals when the Rx Engine is ready to receive data.
PERR	1	Output	Signals when the Rx Engine has received incorrect data based on the internally generated parity and the parity sent to it.
FERR	1	Output	Signals when the Rx Engine does not receive a stop bit during the expected stop bit time.
OVF	1	Output	Signals when the Rx Engine is receiving new data before the previous data has been processed.
UART_RDATA	8	Output	The data that is being received, sent from the Tx Engine.

6.6.4 State Machines

N/A

6.6.5 Register Map

Register Name	Purpose	Description
RXRDY	Holds status flag of RX.	SR flop that is high if done is high, low if reset or Read is high.
PERR	Holds value for a parity error signal.	SR flop that is high if there is a parity error, low if reset or Read is high.
FERR	Holds value for a framing error signal.	SR flop that is high if a stop bit is not detected when it is expected, low if reset or Read is high.
OVF	Holds value for a overflow error signal.	SR flop that is high if DONE and RXRDY are high, low if reset or Read is high.

6.6.6 Verification

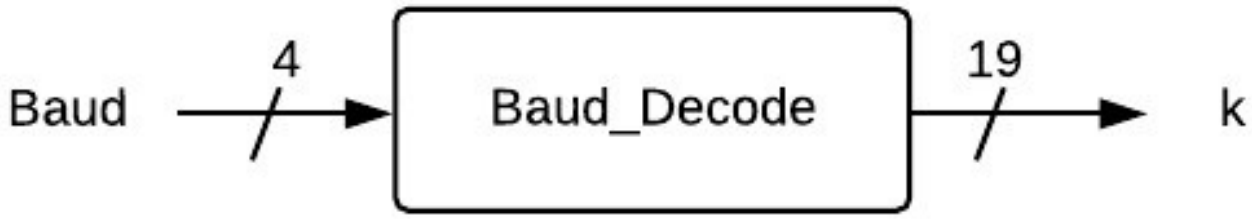
N/A

6.7 Baud Decoder (Baud_Decode.v)

6.7.1 Description

The Baud decoder takes a four bit input and outputs a nineteen bit number. This number acts as the number of clock ticks needed before a data bit can be transferred and received.

6.7.2 Block Diagram



6.7.3 I/O

Signal Name	Bit Size	Input/Output	Description
Baud	4	Input	Determines the baud rate. Driven by onboard
k	19	Output	Holds the value for the number of clock ticks needed before a bit can be transferred and

6.7.4 State Machines

N/A

6.7.5 Register Map

N/A

6.7.6 Verification

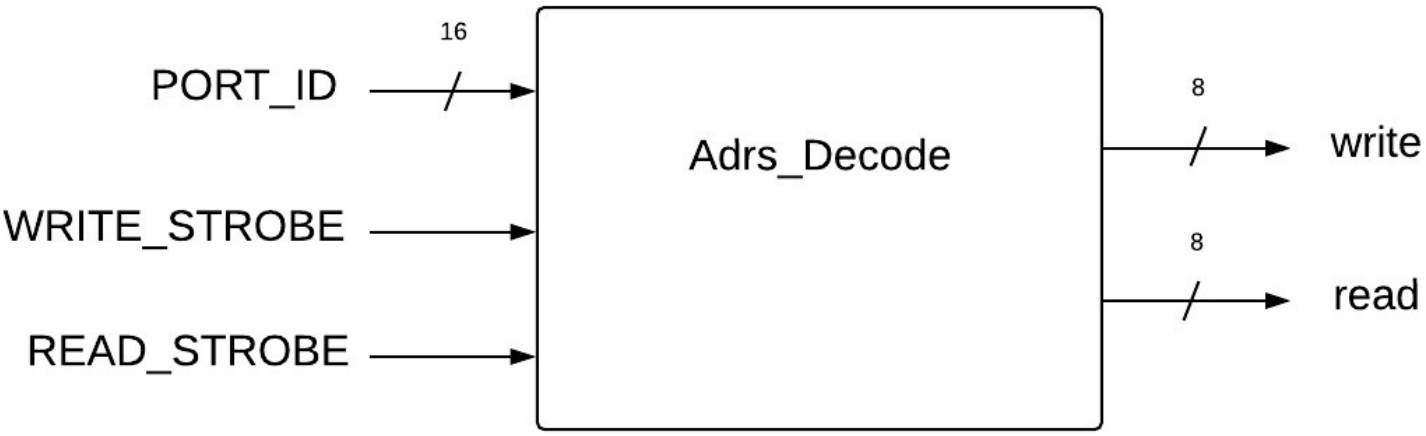
N/A

6.8 Address Decoder (Adrs_Decode.v)

6.8.1 Description

The address decoder determines which action will be executed and at a specific memory address based on the outputs of the TramelBlaze.

6.8.2 Block Diagram



6.8.3 I/O

Signal Name	Bit Size	Input/Output	Description
PORT_ID	16	Input	Outputs the address location at which the data is to be either input or output.
READ_STROBE	1	Input	Signals when the TramelBlaze should read data from a location.
WRITE_STROBE	1	Input	Signals when the TramelBlaze should write data to a location.
Write	8	Output	Determines if UART data or the LEDs will be written.
Read	8	Output	Determines if the UART status flags or data received will be displayed.

6.8.4 State Machines

N/A

6.8.5 Register Map

N/A

6.8.6 Verification

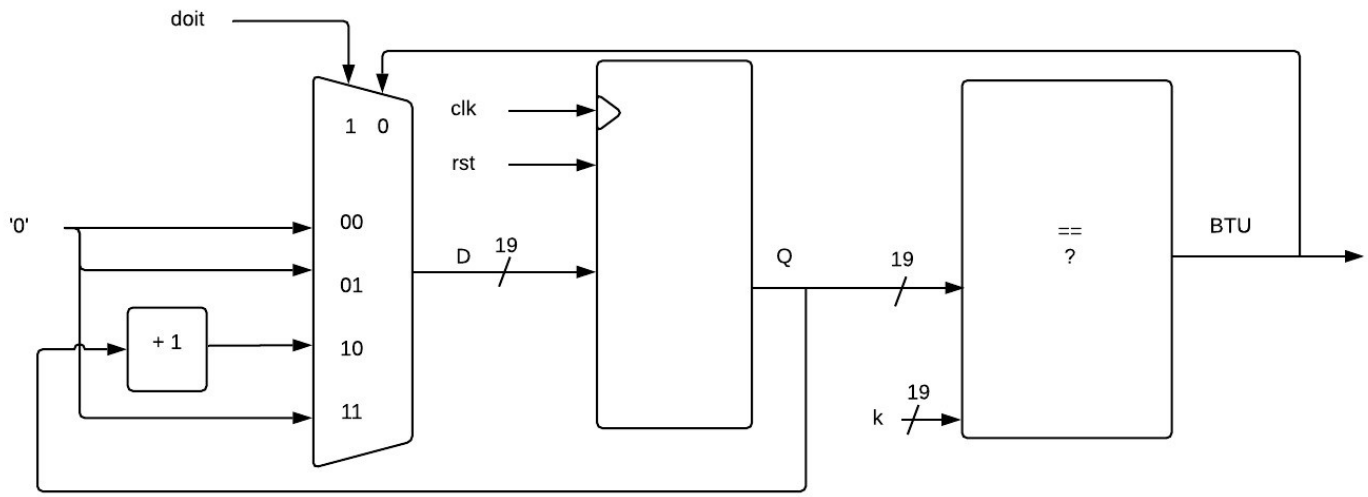
N/A

6.9 Bit Time Up Counter (Counter_BTU.v)

6.9.1 Description

The bit time up counter keeps count of how many clock ticks are needed before UART data can be shifted bit by bit for both the Transmit and Receive engines. The number of clock tics needed is determined by the Baud decoder.

6.9.2 Block Diagram



6.9.3 I/O

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator
Rst (reset)	1	Input	Brings all signals to a known state. Driven by onboard push button.
k	19	Input	Holds the value for the number of clock ticks needed before a bit can be transferred and received.
doit	1	Input	Determines value of the multiplexor, which is sent to a flop to hold the current count value.
BTU	1	Output	Signals when the data bit can be transferred.

6.9.4 State Machines

N/A

6.9.5 Register Map

Register Name	Purpose	Description
Q	Holds the value of the counter, which will be compared to the baud rate.	D flop that is compared to the baud rate.

6.9.6 Verification

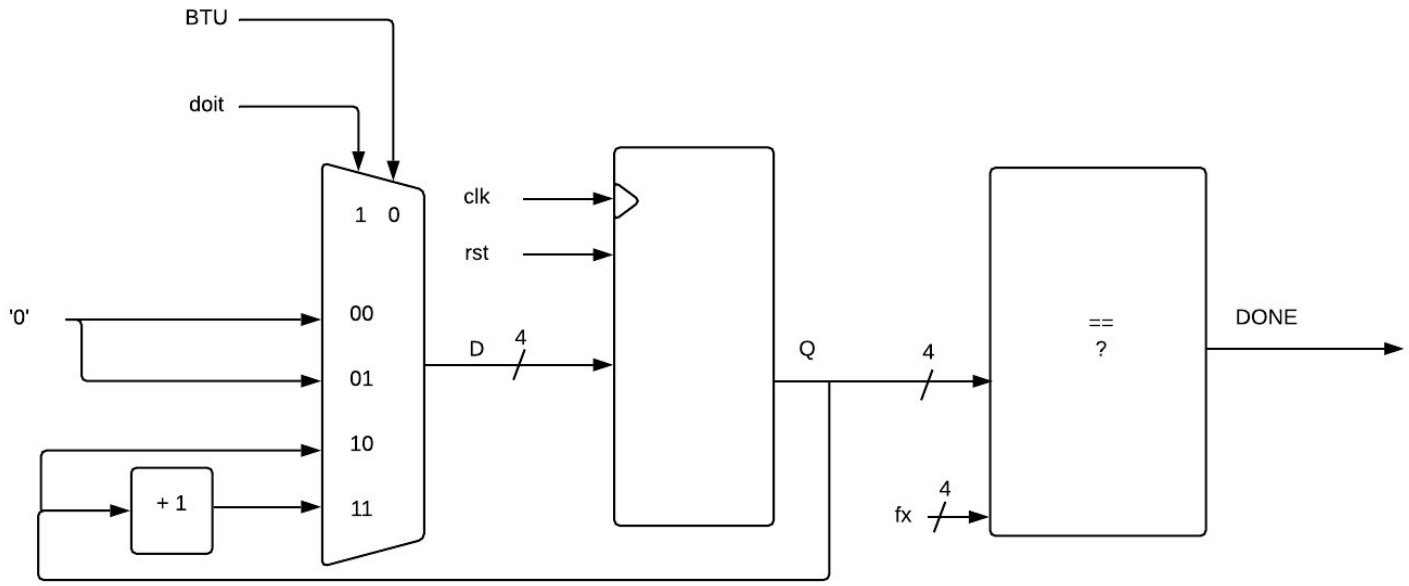
N/A

6.10 Bit Done Counter (Counter_Done.v)

6.10.1 Description

The bit done counter keeps track of the number of bits that have been transmitted or received. In the Tx Engine, the counter is always compared to 11 bits. In the Rx Engine, the comparison number is determined by EIGHT and PEN.

6.10.2 Block Diagram



6.10.3 I/O

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator
Rst (reset)	1	Input	Brings all signals to a known state. Driven by onboard
fx	4	Input	Holds the value for the number of bits that will be written or received.
doit	1	Input	Determines value of the multiplexor, which is sent to a
BTU	1	Input	Signals when the data bit has been transferred.
DONE	1	Output	Signals when all necessary data bits have been transferred.

6.10.4 State Machines

N/A

6.10.5 Register Map

Register Name	Purpose	Description
Q	Holds the value of the counter, which will be compared to fx.	D flop that is compared to fx.

6.10.6 Verification

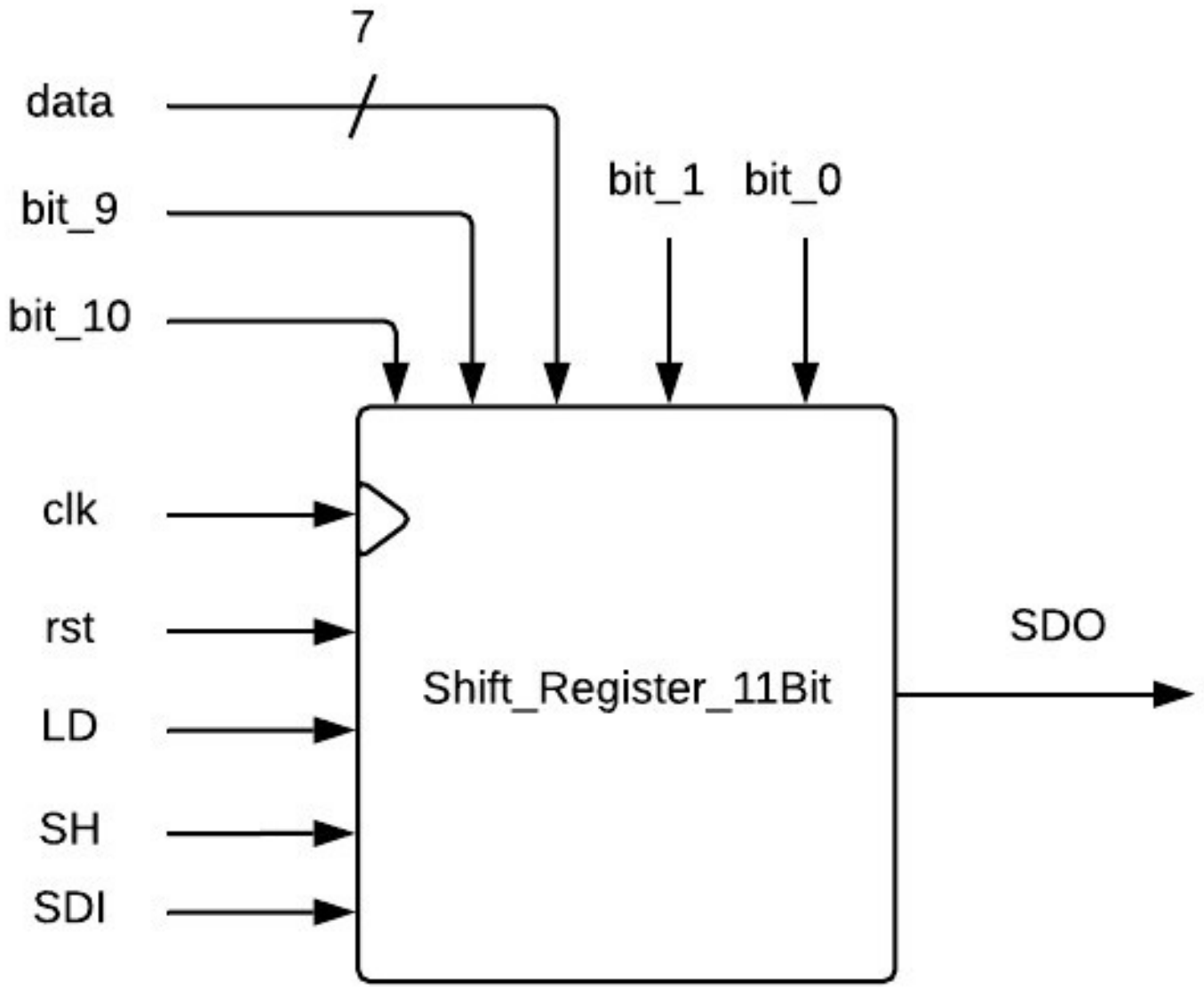
N/A

6.11 11 Bit Shift Register (Shift_Register_11Bit.v)

6.11.1 Description

The 11 bit shift register takes in data to be written, and outputs the data bit by bit.

6.11.2 Block Diagram



6.11.3 I/O

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator
Rst (reset)	1	Input	Brings all signals to a known state. Driven by
LD	1	Input	Allows module to accept data bits when signal is high.
SH	1	Input	Signals when the data should be shifted.
SDI	1	Input	Constant “1” bit used for shifting.
Bit_10	1	Input	Eleventh bit of data to be shifted.
Bit_9	1	Input	Tenth bit of data to be shifted.
data	7	Input	Data to be loaded when LD signal is high.
Bit_1	1	Input	Constant ‘0’ that will be the second bit to be shifted.
Bit_0	1	Input	Constant ‘1’ that will be the first bit to be shifted.
SDO	1	Output	Data that will be sent out of the Tx Engine bit by bit.

6.10.4 State Machines

N/A

6.10.5 Register Map

Register Name	Purpose	Description
Store	Stores the data that has been shifted within the shift register.	Holds data used for shifting. Register is filled with ‘1’ when reset is high.

6.10.6 Verification

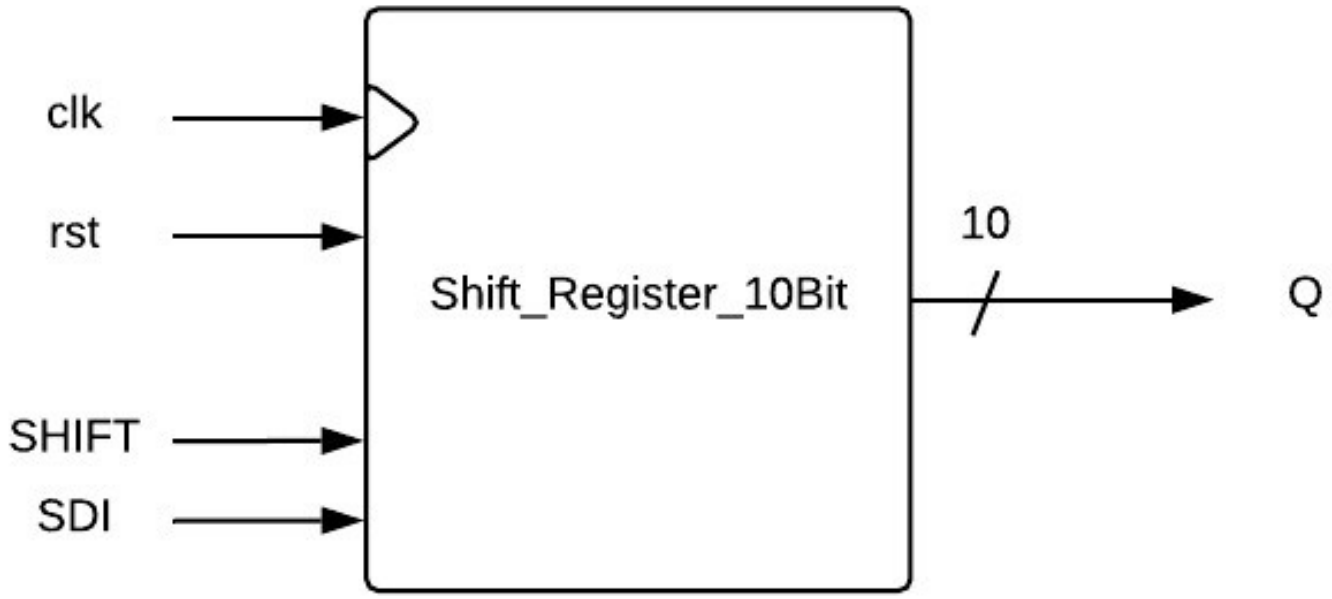
N/A

6.12 10 Bit Shift Register (Shift_Register_10Bit.v)

6.12.1 Description

The 10 bit shift register takes in data that is received bit by bit, and outputs the data as one whole value.

6.12.2 Block Diagram



6.12.3 I/O

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator
Rst (reset)	1	Input	Brings all signals to a known state. Driven by
SHIFT	1	Input	Signals when the data should be shifted.
SDI	1	Input	Data that is received bit by bit from the Tx Engine.
Q	10	Output	Data that will be sent out of the shift register and into other modules.

6.12.4 State Machines

N/A

6.12.5 Register Map

Register Name	Purpose	Description
Q	Stores the data that has been shifted within the shift register.	Holds data used for shifting. Register is filled with ‘0’ when reset is high.

6.12.6 Verification

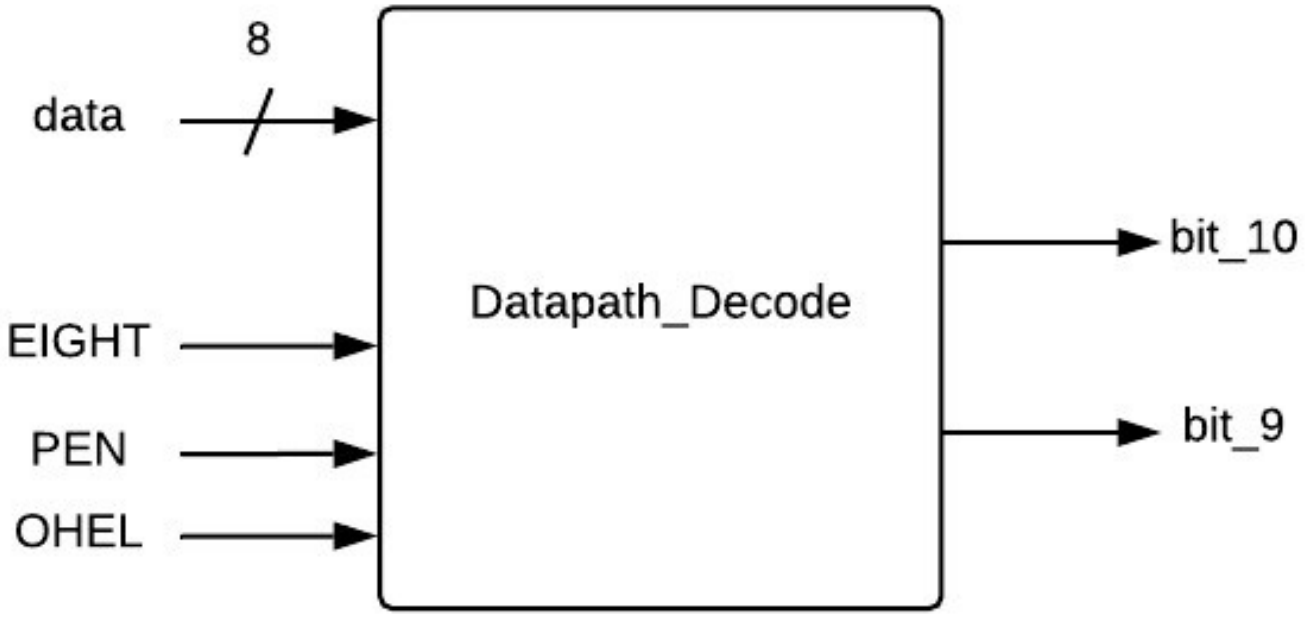
N/A

6.13 Transmit Datapath Decoder (Datapath_Decode.v)

6.13.1 Description

The Tx Engine's datapath decoder uses three inputs to determine the most significant bits to be transmitted out of the Tx Engine.

6.13.2 Block Diagram



6.13.3 I/O

Signal Name	Bit Size	Input/Output	Description
EIGHT	1	Input	Determine the number of bits that will be transmitted from the Transmit Engine.
PEN	1	Input	Determines if a parity bit will be sent along with the data from the Transmit Engine.
OHEL	1	Input	Determine the state of the parity bit that will be transmitted from the Transmit Engine.
data	8	Input	Main portion of UART data to be written.
Bit_10	1	Output	Eleventh bit of data to be shifted.
Bit_9	1	Output	Tenth bit of data to be shifted.

6.13.4 State Machines

N/A

6.13.5 Register Map

N/A

6.13.6 Verification

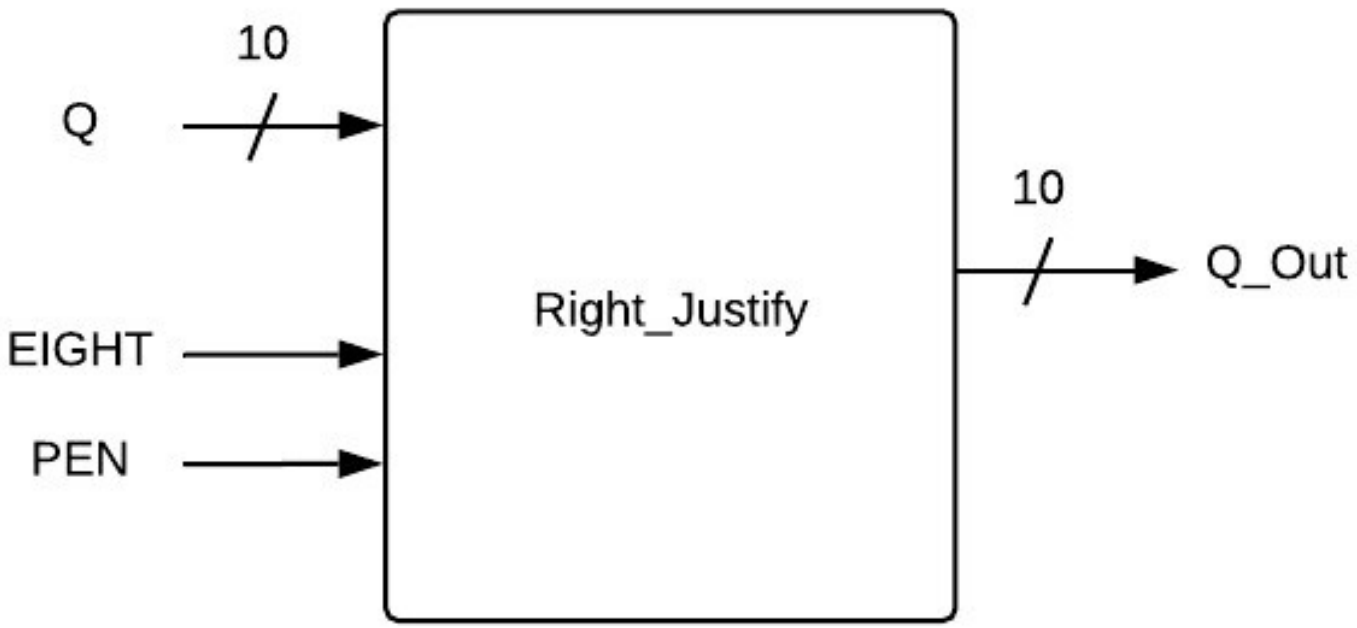
N/A

6.14 Right Justify (Right_Justify.v)

6.14.1 Description

This module puts the starting bit ‘0’ in the proper position once the proper number of data bits has been received.

6.14.2 Block Diagram



6.14.3 I/O

Signal Name	Bit Size	Input/Output	Description
EIGHT	1	Input	Determine the number of bits that will be transmitted from the Transmit Engine.
PEN	1	Input	Determines if a parity bit will be sent along with the data from the Transmit Engine.
Q	10	Input	The complete data received from the shift register.
Q_Out	10	Output	The complete data after being right justified.

6.14.4 State Machines

N/A

6.14.5 Register Map

N/A

6.14.6 Verification

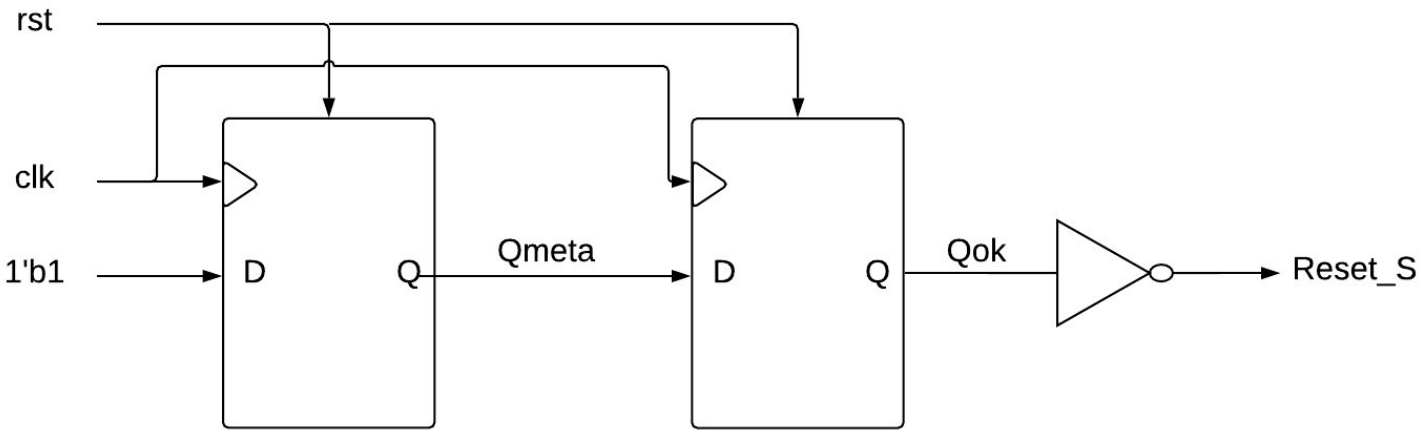
N/A

6.15 Asynchronous In Synchronous Out (AISO.v)

6.15.1 Description

Asynchronous In Synchronous Out (AISO) module is designed to take the input of a push button at any time and release a single output to multiple modules at the same time.

6.15.2 Block Diagram



6.15.3 I/O

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator
Rst (reset)	1	Input	Brings all signals to a known state. Driven by onboard push button.
Reset_S	1	Output	Outputs a synchronized signal to multiple modules to prevent metastability.

6.15.4 State Machines

N/A

6.15.5 Register Map

Register Name	Purpose	Description
Qmeta	Holds a value of 1 until reset is asserted.	Sets state to be changed only by reset
Qok	Holds output signal from Qmeta to prevent metastability.	Signal is received from Qmeta and changed when reset is asserted.

6.15.6 Verification

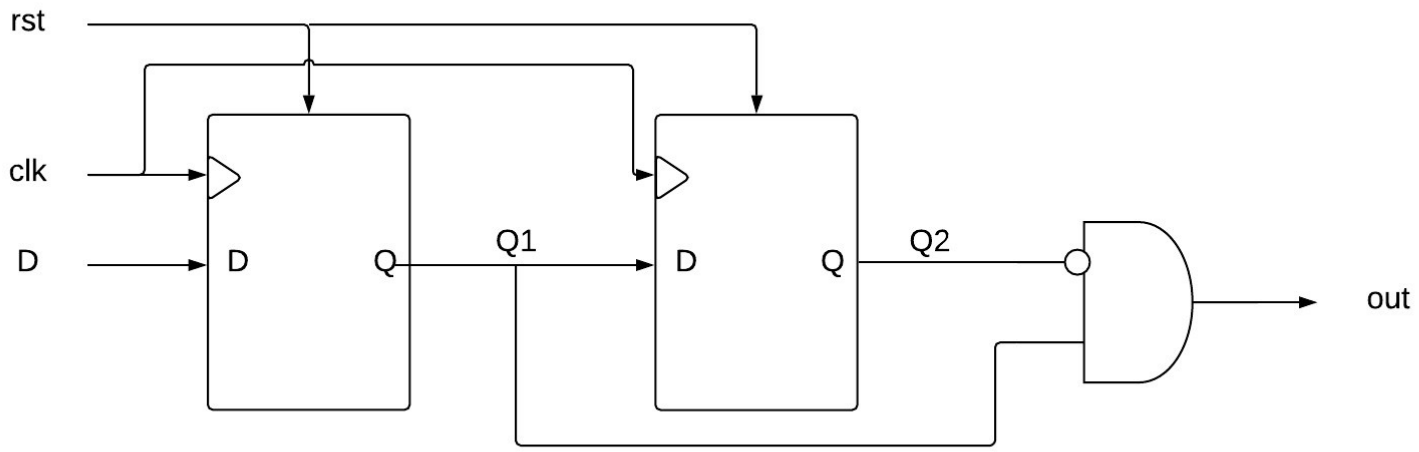
N/A

6.16 Positive Edge Detect (PED.v)

6.16.1 Description

Positive Edge Detect (PED) outputs a one clock wide high active pulse when the module receives a high signal. The output signal goes low after the pulse for the duration the input signal is high.

6.16.2 Block Diagram



6.16.3 I/O

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator
Rst (reset)	1	Input	Brings all signals to a known state. Driven by
D	1	Input	The main data signal of focus.
out	1	Output	Outputs a one clock wide high active signal and goes for the duration the input signal is high.

6.16.4 State Machines

N/A

6.16.5 Register Map

Register Name	Purpose	Description
Q1	Holds the input signal for the module.	Used as a high active input for AND gate.
Q2	Holds the output signal from Q1.	Used as a low active input for AND gate.

6.16.6 Verification

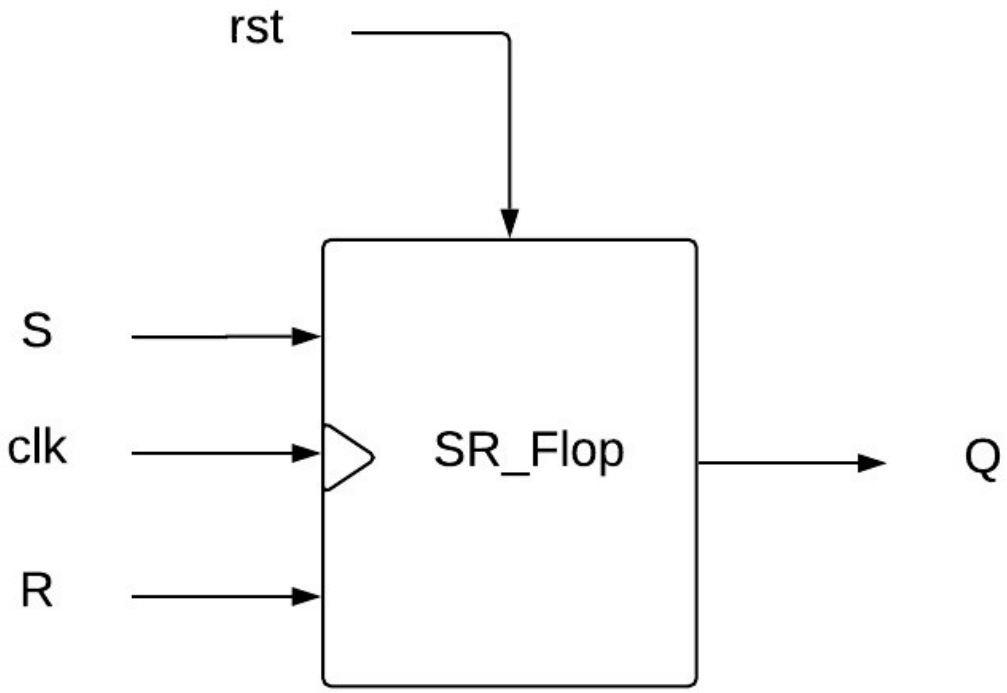
N/A

6.17 Set Reset Flop (SR_Flop.v)

6.17.1 Description

The Set Reset Flop (SR Flop) is used to set and reset a value depending on the two inputs. For this particular chip specification, high signals from Set will have priority.

6.17.2 Block Diagram



6.17.3 I/O

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator.
Rst (reset)	1	Input	Brings all signals to a known state. Driven by onboard push button.
S	1	Input	Signal for Set.
R	1	Input	Signal for Reset (not to be confused with rst).
Q	1	Output	Output of SR Flop.

6.17.4 State Machines

N/A

6.17.5 Register Map

Register Name	Purpose	Description
Q	Holds the output for SR Flop.	Output is high when set is high. Output is low when rst is asserted or Reset is high. Output is retained if no input signals are high.

6.17.6 Verification

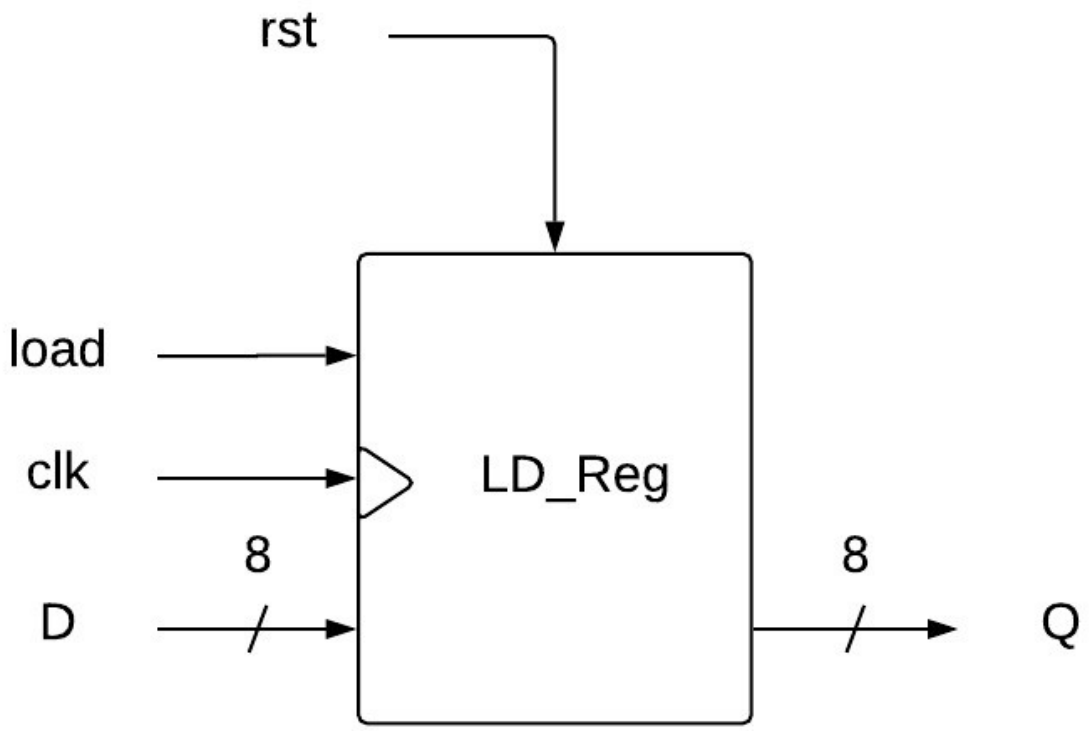
N/A

6.18 Loadable Register (LD_Reg.v)

6.18.1 Description

A loadable register that reads the new data input when the load signal is high and retains the current data output when the load signal is low. For this particular chip specification, the register will be eight bits wide.

6.18.2 Block Diagram



6.18.3 I/O

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator.
Rst (reset)	1	Input	Brings all signals to a known state. Driven by onboard push button.
load	1	Input	Determines if the module will read the main data input signal or retain the current data output signal.
D	8	Input	The main data input signal.
Q	8	Output	The data output signal.

6.18.4 State Machines

N/A

6.18.5 Register Map

Register Name	Purpose	Description
Q	Holds the output for the LD Flop.	If load is active, D gets Q. Else, Q gets Q.

6.18.6 Verification

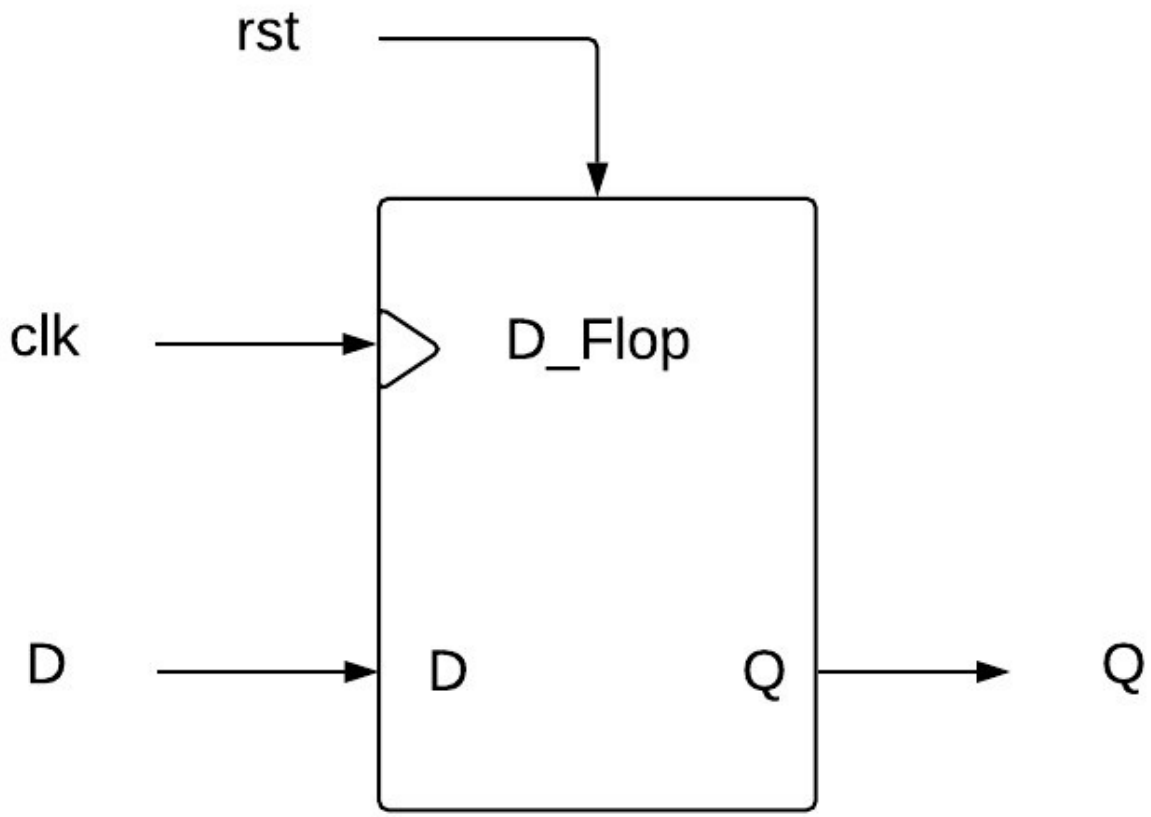
N/A

6.19 D Flip Flop (D_Flop.v)

6.19.1 Description

A one bit wide register. This is the fundamental building block that is used to hold data values. At the active edge of the clock, the value of D gets copied to Q.

6.19.2 Block Diagram



6.19.3 I/O

Signal Name	Bit Size	Input/Output	Description
Clk (clock)	1	Input	Driven by 100MHZ crystal oscillator.
Rst (reset)	1	Input	Brings all signals to a known state. Driven by onboard push button.
D	1	Input	The data input signal.
Q	1	Output	The data output signal.

6.19.4 State Machines

N/A

6.19.5 Register Map

Register Name	Purpose	Description
Q	Holds the output for the D Flop.	At the active edge of the clock, the value of D gets copied to Q.

6.19.6 Verification

N/A

7 Chip Level Verification

N/A

8 Chip Level Test

N/A

9 Modules and Software

9.1 Assembly Code (.tba files)

9.1.1 transmit.tba

This file shall be used to verify the functions of the Transmit Engine for the UART.

9.1.2 receive.tba

This file shall be used to verify the functions of the Receive Engine for the UART.

9.2 Assembler Code

9.2.1 trambler.py

Use this file to create instructions for the TramelBlaze processor. The assembler accepts files ending with .tba.

9.3 Externally Developed Verilog Modules (.v files)

9.3.1 tramelblaze_top.v

9.3.2 tramelblaze.v

9.4 Internally Developed Verilog Modules (.v files)

9.4.1 Adrs_Decode.v

9.4.2 AlSO.v

9.4.3 Baud_Decode.v

9.4.4 Counter_BTU.v

9.4.5 Counter_Done.v

9.4.6 D_Flop.v

9.4.7 Datapath_Decode.v

9.4.8 LD_Reg.v

9.4.9 PED.v

9.4.10 Project4.v

9.4.11 Right_Justify.v

9.4.12 Rx_Engine.v

9.4.13 Rx_Engine_Control.v

9.4.14 Rx_Engine_Datapath.v

9.4.15 Shift_Register_10Bit.v

9.4.16 Shift_Register_11Bit.v

9.4.17 SR_Flop.v

9.4.18 Tx_Engine.v

9.4.19 UART.v