VINCENT CAUQUIL

Apprentice Research Engineer | Physics & Microelectronics Systems

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Apprentice Research Engineer with hands-on experience in **Cryogenic Electronics (4K)** and **Mixed-Signal IC Design**. Skilled in thermal budgeting for quantum setups and semiconductor physics. Seeking a PhD opportunity to advance **Computing Architectures** and develop **robust, high-speed acquisition interfaces** for quantum or constrained applications.

EXPERIENCE

Apprentice Research Engineer
CEA-Leti | Quantum Devices Laboratory

📅 Sept 2023 – Sept 2026   📍 Grenoble, France

Focus: Characterization and hardware development for quantum devices (FD-SOI & Cryogenics).

- **Cryogenic Circuit Design (4K): Currently designing** a multiplexing and amplification circuit (cryogenic I/V converters) managing 50 I/Os, targeting high-speed signal integrity and thermal compliance.
- **Device Physics: Characterizing** FD-SOI substrate polarization effects (body factor) at room temperature to model transistor behavior.
- **Process Optimization: Developed** an automated dicing method for 300mm wafers, aiming to increase yield and speed compared to manual cleaving.

Research Intern
Institute of Science Tokyo

📅 July 2025 – Sept 2025   📍 Tokyo, Japan

Subject: Cryogenic packaging and high-density interconnects.

- Designed an architecture using **off-the-shelf components** to enable the **sequential testing** of multiple quantum chips within a single cooling cycle.
- Addressed strict **thermal dissipation** and spatial constraints specific to cryogenic systems (cryostat).

EDUCATION

Engineering Degree
Physics & Microelectronic Systems (PSM)
CPE Lyon – Class Valedictorian 🏆

📅 Sept 2023 – Sept 2026   📍 Villeurbanne, France

- **Electronics & IC Design:** Analog/Mixed-Signal & **RF Circuits**, simple ASIC Design, Sensors & PCB Design.
- **Digital & Computing:** FPGA Architecture, HDL (Verilog/VHDL), RISC-V (LiteX), **AI for Integrated Design** (ML/RL for EDA).
- **Physics & Signal:** Semiconductor Device Physics, **Quantum Mechanics** & Computing, Digital Signal Processing.
- **Research Initiation:** Seminars by **Centrale Lyon** researchers & drafting of an IEEE review paper on **Neuromorphic Processors** (🔗 Read).

Intensive Undergraduate Program
Mathematics & Physics (CPGE PSI)
Institution des Chartreux

📅 Sept 2021 – Sept 2023   📍 Lyon, France

Two-year intensive preparation for the highly competitive entrance exams to French "Grandes Écoles". Focus on rigorous analytical reasoning and physics modelling.

LANGUAGES

French: Native   **English:** Professional (C1)
Spanish: Elementary   **Japanese:** Elementary

SOFT SKILLS & INTERESTS

- **Leadership & Open-mindedness:** 👥 *Rep. & Project Lead* Developed autonomy & coordination.
- **Creativity & Precision:** 🌙 *Astronomy* (Imagination & Problem-solving) 📷 *Photography* (Rigor).
- **Discipline & Strategy:** 🏊 *Swimming* (Perseverance) 🏸 *Badminton* (Adaptability).

ACADEMIC PROJECTS

- **Smart Modular Parking (IoT/FPGA/Power):** **Led** the technical development and full system integration. Engineered the **RISC-V SoC** (LiteX/Custom Linux) on FPGA and full **BMS** architecture (RP2350/TI BQ IC's). ○ Repository

  🏆 *Best Technical Project **Awarded** at 2025 CPE Lyon Majors Competition*

- **Mixed-Signal IC Design (Cadence):** Full design of a **2nd Order CT** $\Sigma\Delta$ **ADC** (50dB SNR, 64 OSR) and a 4-bit R-2R DAC. Validated via Monte-Carlo & Corner analysis.

- **AI Optimization for Standard Cells (Sky130):** Developed a Reinforcement Learning tool to optimize logic cells' **PPA metrics** via automated SPICE/DRC loops. ○ Repository

  ❝ *See detailed schematics, layouts, code and more project in my ○ **portfolio*** ❞

TECHNICAL SKILLS

Physics & Cryogenics:

Cryogenics (4K/Dilution)

Semiconductor Physics   RF Concepts

Thermal Budgeting   Quantum Devices

EDA & Instrumentation:

Cadence Virtuoso   Spectre / SPICE

KiCad   Xilinx Vivado   LabVIEW   LTspice

Programming:

Python 🐍   OpenCV PyTorch   MATLAB

Verilog/VHDL   HTML/CSS   C/C++

Assembly   🐧 Linux/Bash   MS365 📄📊📑