NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2017-2018

CE1006/CZ1006 – COMPUTER ORGANIZATION AND ARCHITECTURE

Apr/May 2018 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 7 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.
5. The VIP Instruction Set Summary Chart is provided in Appendix 1 on page 7.

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1. Figure Q1a shows the hexadecimal contents of several registers in the VIP processor and a section of its memory.

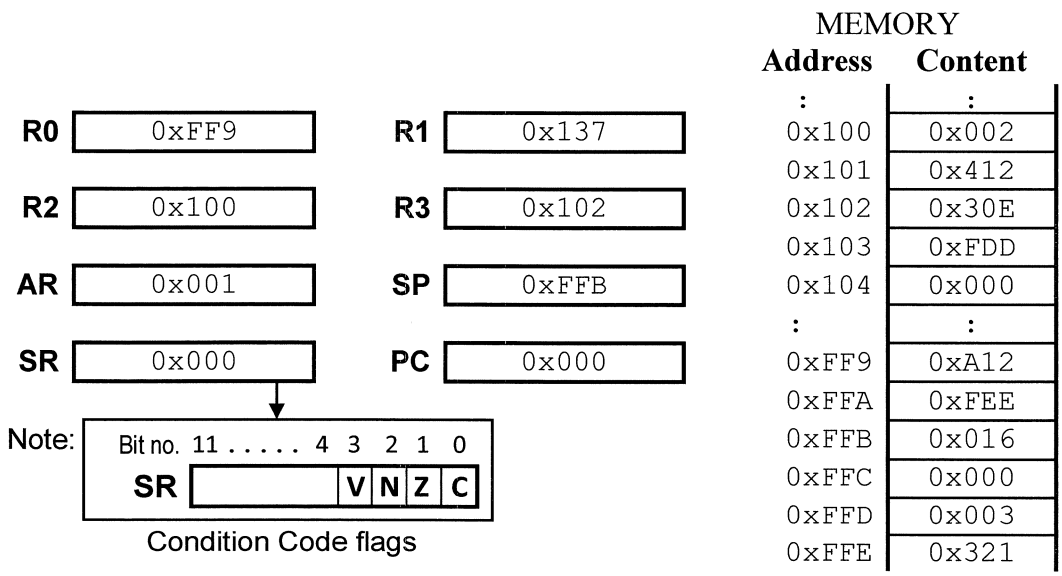

Figure Q1a

Note: Question No. 1 continues on Page 2

(a) Give (*in hexadecimal*) the 12-bit contents in the two registers **R1** and **SR**, immediately after the execution of each instruction given below.

Note: Instructions (i) to (v) are **not consecutive instructions**. You must use the initial conditions shown in Figure Q1a to derive your answer for each of the instructions given below.

(i) `MOV R1,R0`

(ii) `MOV R1,[R3+2]`

(iii) `EOR R1,[SP]`

(iv) `SUB R1,#0x8C4`

(v) `ROR R1`

(10 marks)

(b) Rewrite the VIP assembly language code segment given in Figure Q1b to optimize its execution speed. Your optimized code must produce the same results in the data registers and memory locations as the original code. More marks will be given for a more optimized code.

(7 marks)

```
START   PSH  R0
        PSH  R1
        PSH  R3
        MOV  R0,#0
        MOV  R1,#20
        MOV  R3,[0x100]
LOOP    ADD  R0,[0x100]
        ADD  R1,#0xFFF
        CMP  R1,#0
        JGE  LOOP
FINISH  ADD  R0,[0x100]
```

Figure Q1b

(c) With initial conditions shown in Figure Q1a, give the value in register **R0** when execution ends **after** label **FINISH** for the code segment in Figure Q1b. Assume execution begins at **START**.

(3 marks)

(d) Rewrite the VIP code segment in Figure Q1b so that it will be position-independent. State any assumptions you have made in deriving your answer.

(5 marks)

2. A VIP assembly language program and the contents of several memory variables are given in Figure Q2.

(a) Describe clearly the purposes of the **two instructions** at (**a1**) and give the instructions needed to achieve the requirements stated in the comments at (**b1**) and (**b2**).

(8 marks)

(b) Give the instructions required at (**c1**) and (**d1**) to ensure subroutine **SubA** returns correctly and the stack parameters are removed.

(6 marks)

```
Strt   PSH   [0x100]
       PSH   #0x101
       CALL  SubA
         ?                ; remove parameters from the stack          (d1)
         :
SubA   PSH   R2           ;
       SUB   SP,#3        ;  }(a1)
         ?                ; get the contents of Var_N on the stack into R2   (b1)
       MOV   [SP],R2
         ?                ; get the address of Var_X on the stack into R2    (b2)
       MOV   [SP+2],#0
       MOV   [SP+1],#0
Loop   CMP   [R2],#0
       JPL   Skip
       INV   [R2+0]
       INV   [R2+1]
       ADD   [R2+1],#1
Skip   ADD   [SP+2],[R2+1]
       ADDC  [SP+1],[R2+0]
       SUB   [SP],#1
       JEQ   Done
       ADD   R2,#2
       JMP   Loop
Done   MOV   [R2+0],[SP+1]
       MOV   [R2+1],[SP+2]
         ?               ;
         ?               ;  }(c1)
         ?               ;
```

Address	Contents
Var_N 0x100	0x003
Var_X 0x101	0x111
0x102	0xFFF
Var_Y 0x103	0x9FF
0x104	0xFFE
Var_Z 0x105	0x100
0x106	0x222

Memory Map

Figure Q2

(c) The values in the memory map shown in Figure Q2 are initial values before execution. Redraw the memory map with its new contents immediately after returning from the subroutine **SubA**. You may assume that the program execution begins at the label **Strt**.

(7 marks)

(d) Describe the function of subroutine **SubA** by giving details of how the parameters passed in affect its operation and state clearly how memory variables **Var_X**, **Var_Y** and **Var_Z** are interpreted.

(4 marks)

3. (a) Determine the most suitable memory to be used for each requirement listed in Table Q3a below and give explanation for your choice. The memory types available are: SRAM, DRAM, EEPROM, NAND Flash, NOR Flash and Magnetic HDD. Note that each memory type may be used more than once if deemed most suitable.

(6 marks)

Table Q3a

Requirements	Memory Type
Robust portable 256Gbyte external storage. Needs to retain data when powered off and immune to excessive vibration during operation.	
Memory to store 100 sets of user configuration data. Each set of data is <64bytes in size and can be erased without affecting other sets of user configuration. User configuration needs to be retained when changing batteries.	
Main storage memory of an 8-TeraByte home-based Network Attached Storage system.	

(b) You are tasked to design a wired transmission channel between two sets of equipment. The channel requirement is as shown below

- Length of channel = 20 meter (The length is considered long, in case you are wondering)
- The highest data transfer rate possible under the given condition
- Channel will pass through an electrically noisy environment

Select your choice of interface design with respect to each of the options given below and explain clearly why you choose those designs.

- Serial vs Parallel
- Asynchronous vs Synchronous
- Single-ended vs Differential signaling

(9 marks)

Note: Question No. 3 continues on Page 5

(c) Two computer systems, COMP-A and COMP-B are connected via a UART link. Table Q3b shows the UART configuration for COMP-A and COMP-B.

Table Q3b

COMP-A UART	COMP-B UART
1 Start, 8 Data, 1 Stop Bit	1 Start, 8 Data, 1 Stop Bit
No Parity Scheme	No Parity Scheme
Baud rate = 115200 bps	Baud rate = Unknown
Allowable baud rate: 115200, 57600, 38400, 28800, 19200, 14400, 9600, 4800, 2400.	

Given that COMP-B transmits a value of 0x0D and COMP-A receives 0x00. What is/are the possible baud rate(s) that COMP-B is transmitting at? Illustrate your answer clearly with the UART timing diagram.

(6 marks)

(d) Describe clearly two advantages that the Sold State Drive has over the Hard Disk Drive.

(4 marks)

4. (a) Describe the write-through and write-back cache write policy. Which write policy would you choose for a system with limited system bus bandwidth? Give one reason to justify your choice.

(5 marks)

(b) Consider a system with the following characteristics.

- Direct mapped cache of 16 cache blocks and block size 16 bytes
- Cache uses Physical Address for address mapping
- Virtual Memory page size 1024bytes
- Virtual Memory size 1Mbyte. Physical Memory size 64 KByte
- Extracts of Page Table (valid entries)
  - Virtual Page 0 → Physical Frame 2
  - Virtual Page 1 → Physical Frame 5
  - Virtual Page 2 → Physical Frame 8
  - Virtual Page 9 → Physical Frame 3

From which cache block would the CPU retrieve the data for a virtual address 0x00911? What is the corresponding tag value of the cache block if it is a cache hit?

(8 marks)

Note: Question No. 4 continues on Page 6

(c) What is the difference between carry and overflow? Describe the functions of the carry bit and overflow bit in computer arithmetic operations.

(4 marks)

(d) Consider a processor with 4 pipeline stages: Fetch Instruction (F), Decode (D), Execute (E) and Store (S). Assume that

- Branch target address is calculated at the execute stage
- Instruction length for every instruction is one word long
- Each pipeline stage takes 1 cycle to complete
- No resource conflicts
- This processor is not the VIP processor

(i) Describe and illustrate with a pipeline diagram the pipeline conflict created by a branch instruction.

(4 marks)

(ii) Given that delayed branching is NOT enabled, identify ALL pipeline conflicts the code in Figure Q4 has when run in the pipeline processor above. Marks will be deducted for wrongly identified conflicts.

```
      MOV   R3, #0x400 ; I1
      MOV   R1, #0x200 ; I2
      ADD   [R3], R1   ; I3
Loop  SUB   [R1], R3   ; I4
      INC   R3         ; I5
      DEC   R1         ; I6
      JNE   Loop       ; I7
      MOV   R2, [R1]   ; I8
      MOV   [R3], [R2] ; I9
```

Figure Q4

(4 marks)

Appendix 1

VIP Instruction Set Summary Chart

VIP Instruction Encoding – Opcode Formats

11	10	9	8	7	6	5	4	3	2	1	0
0-7	Dual operand			d				s			
8	Short Move			d				n			
9-A	Unary/Control			op-code				operand = s, d or n			
B-F	JMP			2's complement -128 to +127 *relative*							

Group 1 – Dual-Operand Instructions (Opcode: 000 to 8FF)

Bits 8-11	Name	Bits 4-7	Bits 0-3	Operation	Flags
0	MOV	d	s	d ← s	NZ
1	AND	d	s	d ← d .AND. s	NZ
2	OR	d	s	d ← d .OR. s	NZ
3	EOR	d	s	d ← d .EOR. s	NZ
4	ADD	d	s	d ← d + s	VNZC
5	ADDC	d	s	d ← d + s + carry	VNZC
6	SUB	d	s	d ← d + (.NOT. s) + 1	VNZC
7	CMP	d	s	d + (.NOT. s) + 1	VNZC
8	MOVS	d	n	d ← n	

Group 2 – Unary and Control Instructions (Opcode: 900 to 9FF)

Bits 4-7	Name	Bit 0-3	Operation	Flags
0	INC	d	d ← d + 1	C
1	DEC	d	d ← d + 0xFFF	NZC
2	ROR	d	Rotate d right : msb ← lsb; and C ← lsb	NZC
3	ROL	d	Rotate d left : lsb ← msb; and C ← msb	NZC
4	RRC	d	Rotate d right including carry	NZC
5	RLC	d	Rotate d left including carry	NZC
6	RAR	d	Rotate d 'arithmetic' right preserving msb	NZC
7	PRSG	d	Left shift lsb from EOR (bits 11,5,3,0)	NZC
8	INV	d	d ← .NOT. d	NZ
9	NEG	d	d ← (.NOT. d) + 1	NZC
A	DADD	s	AR ← AR + s + carry (as 3 BCD digits)	ZC
B	UMUL	s	R1:R0 ← unsigned R0 times unsigned s	Z
C	TST	s	s + 0	NZ
D	EXEC	s	Execute s as an instruction	implied
E	BCSR	n	SR (bits 3-0) ← SR .AND. (.NOT. n)	explicit
F	BSSR	n	SR (bits 3-0) ← SR .OR. n	explicit

Group 3 – Unary and Control Instructions (Opcode: A00 to AFF)

Bits 4-7	Name	Bits 0-3	Operation	Flags
0	PSH	s	SP ← SP-1; (SP) ← s	
1	POP	d	d ← (SP); SP ← SP+1	explicit if d=SR
2	PSHM	3:2:1:0	Push R3:2:1:0 to stack, R3 first	
3	POPM	3:2:1:0	Pop R3:2:1:0 from stack, R3 last	
4	CALL	s	SP ← SP-1; (SP) ← Return Address PC ← Effective address	
5	RET	n	PC ← (SP) + n; SP ← SP+1	
6			See subgroup 3a	
7	RCN	n	Count for next rotate instruction. if n=0 use bits 3:2:1:0 of AR	
8	JDAR	±n	AR ← AR-1, if AR != 0, PC ← PC ± n	
9	JPE	±n	If parity of AR is even, PC ← PC ± n	
A	JPL	±n	If N = 0, PC ← PC ± n	
B	JVC	±n	If V = 0, PC ← PC ± n	
C	JGE	±n	If N = V, PC ← PC ± n	
D	JLT	±n	If N != V, PC ← PC ± n	
E	JGT	±n	If Z = 0 and N = V, PC ← PC ± n	
F	JLE	±n	If Z = 1 or N != V, PC ← PC ± n	

Group 1 – Jump Instructions (8-bit Range) (Opcode: B00 to FFF)

Bits 8-11	Name	n = Bits 0 to 7	Operation
B	JMP = BRA	-128 to +127	PC ← PC ± n
C	JEQ = JZ	-128 to +127	If Z=1, PC ← PC ± n
D	JNE = JNZ	-128 to +127	If Z=0, PC ← PC ± n
E	JHS = JC	-128 to +127	If C=1, PC ← PC ± n
F	JLO = JNC	-128 to +127	If C=0, PC ← PC ± n

Group 3a – Control Instructions (Opcode: A60 to A6F)

Bits 4-7	Name	Bits 0-3	Operation
6	RETI	0	SR ← (SP); SP ← SP+1; PC ← (SP); SP ← SP+1
6	SWI	1	SP ← SP-1; (SP) ← PC; SP ← SP-1; (SP) ← SR; PC ← (0x009)
6	WAIT	2	IE ← 1; Execution resumes after interrupt signal
6	HALT	3	Stop execution. Non-maskable interrupt or hardware reset to exit.
6	STOP	4	Stop execution. Reset to exit.
6	SYNC	8	Pulse SYNC output pin high for 1 clock cycle
6	NOP	9	No operation
6	LOCK	A	Block interrupts and bus sharing
6	UNLK	B	Allow interrupts and bus sharing
6	MSS	C to F	Memory Space Select override

Addressing Modes

Hex	Symbol	Location of Data	Availability
0	R0	Register R0	Both d and s
1	R1	Register R1	Both d and s
2	R2	Register R2	Both d and s
3	R3	Register R3	Both d and s
4	[R0]	Register R0 indirect	Both d and s
5	[R1]	Register R1 indirect	Both d and s
6	[R2+n]	Register R2 with offset indirect	Both d and s
7	[R3+n]	Register R3 with offset indirect	Both d and s
8	AR	Data is in Auxiliary Register	Both d and s
9	SR	Status Register	Both d and s
A	SP	Stack Pointer	Both d and s
B	PC	Program Counter	Both d and s
C	#n	Immediate, (or just n for CALL)	s only
D	[n]	Absolute (code space for CALL)	Both d and s
E	[SP+n]	SP with offset indirect	Both d and s
F	[PC+n]	PC with offset indirect (CALL is relative with PC+n)	Both d and s

Notation: d = destination; s = source

Description of bits in Status Register

SR	F	R	Description
11-8	*	*	Reserved
7-4	*	*	Defined but not described here
3	V	0	Set if 2's complement sign is incorrect
2	N	0	Is most significant bit of result
1	Z	0	1 if result is zero, otherwise 0
0	C	0	1 if carry out, otherwise 0

Notation: SR=Bits in register; F=Name of flag; R=Value after reset

END OF PAPER

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