Assignment 6 (Due on June 2, 2023)

1. This Exercise examines the single error correcting (SEC) Hamming code.
   I. What is the minimum number of parity bits required to protect a 64-bit word using the SEC/DED code? (10 pts)
   7 (64 = 2^6, 6 + 1 = 7)

   II. Consider a SEC code that protects 8 bit words with 4 parity bits. If we read the value 0x375, is there an error? If so, correct the error. (10 pts)
   (Please show detailed process or your will get 0 point)

   0x375 = 0011 0111 0101

   P1 = 0 ⊕ 1 ⊕ 0 ⊕ 1 ⊕ 0 ⊕ 0 = 0

   P2 = 0 ⊕ 1 ⊕ 1 ⊕ 1 ⊕ 1 ⊕ 0 = 0

   P3 = 1 ⊕ 0 ⊕ 1 ⊕ 1 ⊕ 1 = 0

   P4 = 1 ⊕ 0 ⊕ 1 ⊕ 0 ⊕ 1 = 1

2. Mean Time Between Failures (MTBF), Mean Time To Replacement (MTTR), and Mean Time To Failure (MTTF) are useful metrics for evaluating the reliability and availability of a storage resource. Explore these concepts by answering the questions about devices with the following metrics.

MTTF	MTTR
3 Years	1 Day

   I. Calculate the MTBF for each of the devices in the table (10 pts)
   (Please answer how many days or your will get 0 point).

   MTBF = MTTF = MTTR = 365 x 3 + 1 = 1096 days

   II. Calculate the availability for each of the devices in the table (10 pts)
   (Round your answer to 4 decimal places or you will get 0 point).

   Availability = MTTF / MTBF = 325 x 3 / 1096 = 0.9991

3. In this exercise, we will look at the different ways capacity affects overall performance. In general, cache access time is proportional to capacity. Assume that main memory accesses take 70 ns and that memory accesses are 36% of all instructions. The following table shows data for L1 caches attached to each of two processors, P1 and P2.

	L1 size	**L1 Miss Rate**	**L1 Hit Time**
P1	2KiB	8.0%	0.66ns

P2	4KiB	6.0%	0.90ns

Note: please use round to 2 decimal places to calculate all the following problem, or you will get 0 points.

I. Assuming that the L1 hit time determines the cycle times for P1 and P2, what are their respective clock rates? (6 pts)

i. P1 : 1 / (0.66 x 10 ^ (-9)) = 1.52 (6Hz)

ii. P2 : 1 / (0.9 x 10 ^ (-9)) = 1.11 (6Hz)

II. What is the Average Memory Access Time for P1 and P2? (7 pts)

i. P1 : 0.66 + 70 x 0.08 = 6.26 (ns)

ii. P2 : 0.9 + 70 x 0.06 = 5.1 (ns)

III. Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 and P2? Which processor is faster? (7 pts)

i. P1 : miss penalty = 70 / 0.66 = 106.06

miss cycles = 1.36 x 0.08 x 106.06 = 11.54

CPI = 1 + 11.54 = 12.54

ii. P2 : miss penalty = 70 / 0.9 = 77.78

miss cycles = 1.36 x 0.06 x 77.78 = 6.35

CPI = 1 + 6.35 = 7.35

12.54 / 1.52 > 7.35 / 1.11 so P2 is faster

4. Following the previous question, we will consider the addition of an L2 cache to P1 to presumably make up for its limited L1 cache capacity for the next three problems. Use the L1 cache capacities and hit times from the previous table when solving these problems. The L2 miss rate indicated is its local miss rate.

L2 Size	L2 Miss Rate	L2 Hit Time
1 MiB	95%	5.62 ns

I. What is the AMAT for P1 with the addition of an L2 cache? Is the AMAT better or worse with the L2 cache? (6 pts)

AMAT with L2 : 0.66 + 0.08 x (5.62 + 0.95 x 70) = 6.43 > 6.26 so worse

II. Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 with the addition of an L2 cache? (7 pts)

Miss penalty : (5.62 + 0.95 x 70) / 0.66 = 109.27

Miss cycles : 1.36 x 0.08 x 190.27 = 11.89

CPI = 1 + 11.89 = 12.89

III. Which processor is faster, now that P1 has an L2 cache? If P1 is faster, what miss rate would P2 need in its L1 cache to match P1's performance? If P2 is faster, what miss rate would P1 need in its L1 cache to match P2's performance? (7 pts) **(Round your answer to 3 decimal places or you will get 0 point).**

12.89 / 1.52 > 7.35 / 1.11 so P2 is faster.

Now let the new miss rate of P1 = r

We get (1 + 1.36 x r x 109.27) x 0.66 = 7.35 x 0.9

⇨ r = 0.061

5. You are using a 2-way set-associative L1 cache with a capacity of 8KB and cache lines consisting of 4 words. The L2 cache has a latency of 10 cycles for both read and write operations. Here is the sequence of write operations performed on the cache, with each entry representing a 32-bit address in hexadecimal format:

0x1000, 0x1004, 0x1010, 0x11c0, 0x2000, 0x21c0, 0x3400, 0x3404, 0x3f00, 0x2004, 0x1004

I. How many cache misses occur if an LRU policy is implemented? (6 pts)

7

II. If the cache size remains the same but is changed to a direct-mapped configuration, would the miss-rate increase or decrease? Explain why? (7 pts)

Cache live 總數一樣且沒有 replace 發生，因此兩者的 miss rate 一樣。

III. What is the time duration for a read-miss eviction in a write-back, write-allocate cache? And how about for a write-miss? (Assuming the cache line is dirty) (7 pts)

Read-miss : write to L2 (10) + read from L2 (10) = 20 cycles

Write-miss : write to L2 (10) + read from L2 (10) = 20 cycles

4 words = 16 bytes

Offset : 4 bits

Index : 2^13 / (2^4 x 2) = 2^8, log_2 2^8 = 8 bits

Tag : 32 – 4 – 8 = 20 bits

Address	Index	Tag	Access type

0x1000	0x00	0x1	CM
0x1004	0x00	0x1	H
0x1010	0x01	0x1	CM
0x11c0	0x1x	0x1	CM
0x2000	0x00	0x2	CM
0x21c0	0x1c	0x2	CM
0x3400	0x40	0x3	CM
0x3404	0x40	0x3	H
0x3f00	0xf0	0x3	CM
0x2004	0x00	0x2	H
0x1004	0x00	0x1	H