數位系統設計實習
Final Project

指導老師：陳勇志 教授

Schedule

Week	Day	Lecture	Content	Note
1	02/18	1	Introduction, Verilog HDL (Gate level)	
2	02/25	2	Verilog HDL (Date flow level)	
3	03/04	3	Verilog HDL (Behavior level)	
4	03/11	4	Sequential logic, Latch and Flip-Flop	
5	03/18	5	Counter	
6	03/25	6	Shift Register, Johnson Counter	
7	04/01	7	FSM, Seven segment display, Binary to BCD	
8	04/08	8	SMIMS Development Board, LFSR	
9	04/15	9	LCD module	
10	04/22	10	Key Pad module	
11	04/29		Final project	
12	05/06		Final project	
13	05/13		Final project	
14	05/20		Final project	
15	05/27		Final project demo	Project deadline
16	06/03		Final exam	

Final Project Demo

- One person per group
- 6-min in-class presentation (Week 15: 5/27)
  - 3-min slide presentation
  - 3-min pre-recorded video demonstration

Deliveries

- **Fill in the name of the game (Week 13: 5/13)**
  - https://docs.google.com/spreadsheets/d/1kFLfzbB0kP9whGDRE7HFJoAW1_KgHK_pah_5zDKxfNs/edit?usp=sharing

Deliveries

- **Complete all the submissions by the end of class (Week 15: 5/27)**
  - .dkp, .rbf, and presentation slide
    - Tar/zip them into a single file and submit it to Moodle
    - File name: Bxxxxxxxx_DEMO
  - Quartus project
    - Tar/zip the project into a single file and submit it to Moodle
    - File name: Bxxxxxxxx_林小明_Project
  - Demonstration video
    - Upload it to the following google drive
      - https://drive.google.com/drive/folders/1UT76Q_QeroiUTdGvIRVURJPFH8mWM5wq?usp=sharing
      - File name:數位系統設計實習小影片_final_project_Bxxxxxxxx_林小明

Requires

- **Use the following components to get basic points**