數位系統設計實習

Lecture 8

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實習課助教:鍾兆鋐

Outline

- Introduction of FPGA & VeriLite (SMIMS)
- Quartus II FPGA Setting
- VeriLite board and Instrument Setting
- VeriInstrument usage
- LAB 8-1、8-2

Chapter

- Introduction of FPGA & VeriLite (SMIMS)
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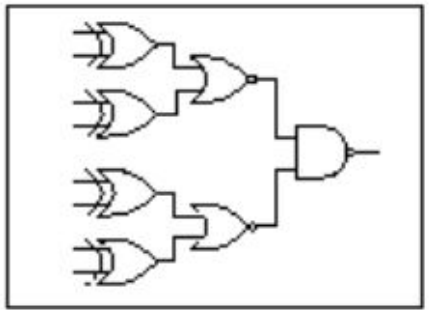
Introduction of FPGA

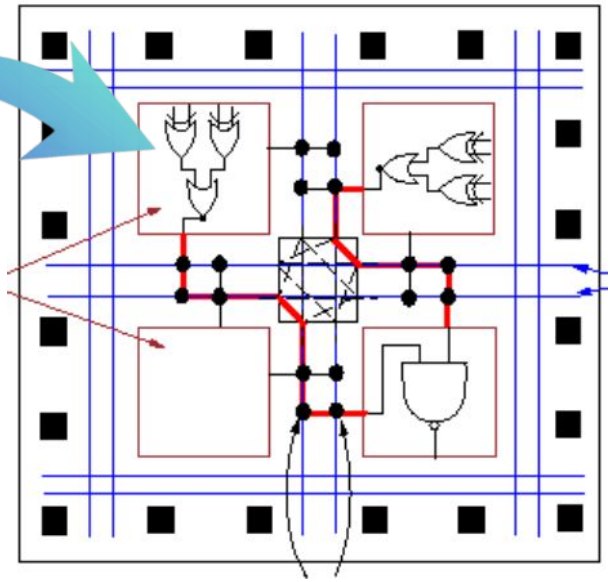
- 硬體描述語言(Verilog)描述之電路功能，可在經過邏輯合成自動化工具轉成邏輯網表(Netlist)後，燒錄至FPGA上進行電路功能測試，靈活且快速的特性，在積體電路設計前段驗證有很大的幫助。
- FPGA內部含有許多可程式化邏輯元件可被用來實現一些基本的邏輯閘數位電路(AND OR NOT XOR...)，燒錄設計好的電路功能，就能夠模擬實際生產運作的晶片。

```
module LEC9_1(a,b,out);
 input [1:0] a, b;
 output out;
 wire w1;

 assign w1=(a[0]^b[0])+(a[0]^b[1]);
 assign out=w1+(a[1]^b[0])+(a[1]^b[1]);

 endmodule
```

VHDL code



Gate-level (Netlist)



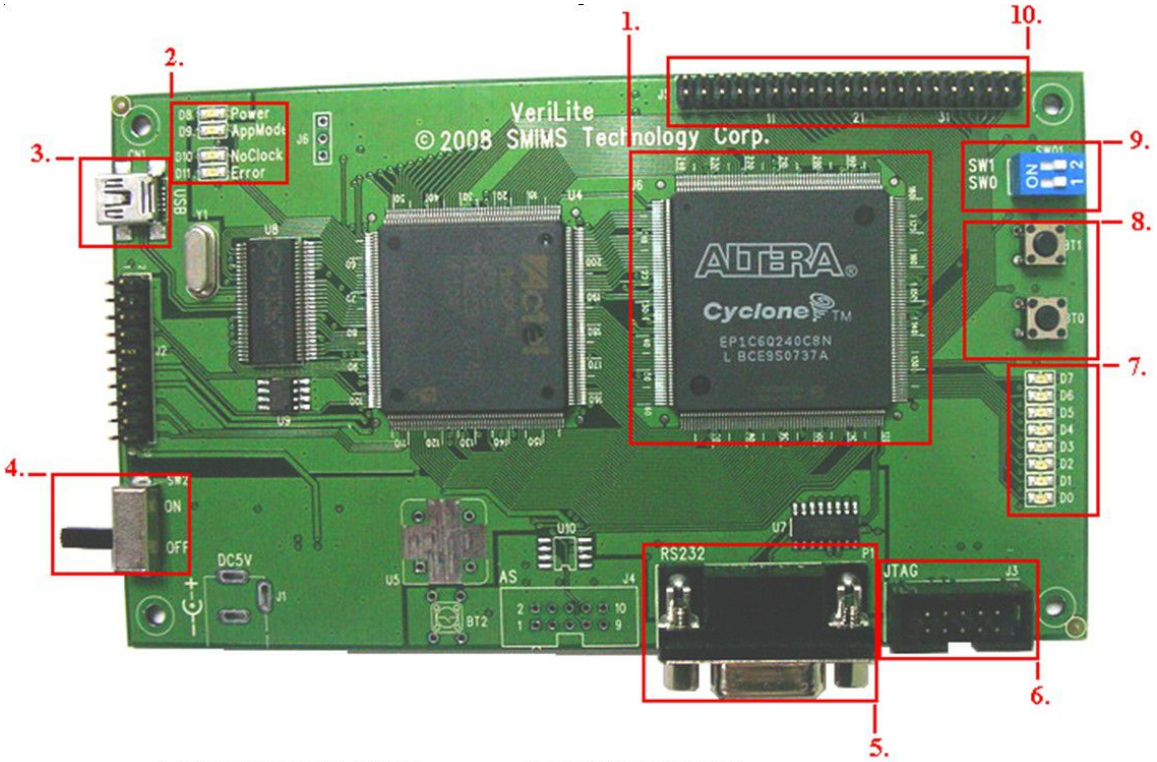
FPGA simulation

Introduction of SMIMS VeriLite

- VeriLite實驗板, 由 北瀚科技(SMIMS) 公司所出產, 其中 FPGA 芯片元件是 Cyclone EP1C(XX)Q240C(X)N (每位同學的板號不同), 其中包含12,060個可程式　化邏輯閘及239,616的on-chip memory。

- 詳細說明可參考moodle LAB_9資料。

Introduction of SMIMS VeriLite



1. Altera Cyclone FPGA
2. LED indicateor light
3. USB 2.0 Interface
4. FPGA power switch
5. RS232 interface
6. JTAG pin header
7. User define LED
8. User define Push Button
9. User define Dip Switch
10. General IO

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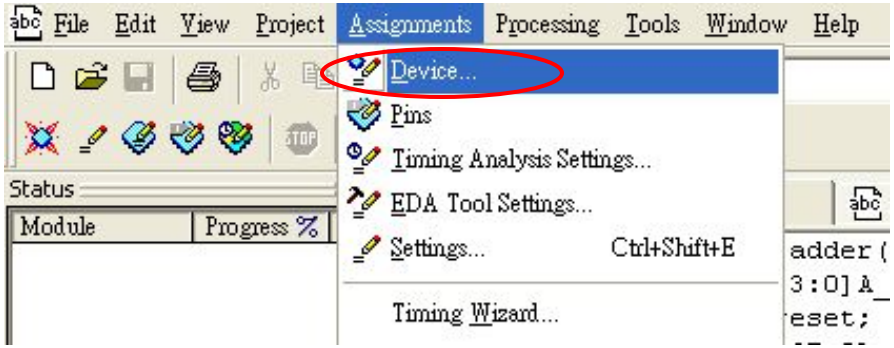
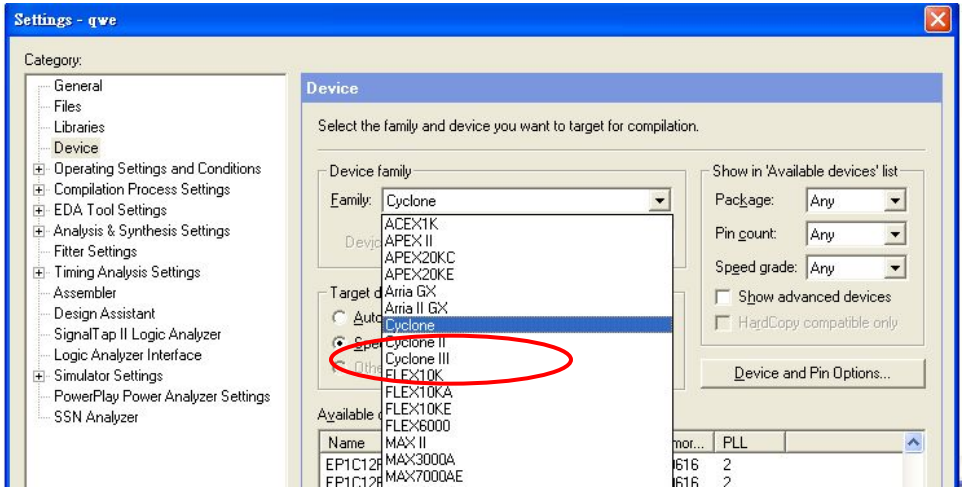
Quartus II FPGA Setting

- Choose Assignments → Device。

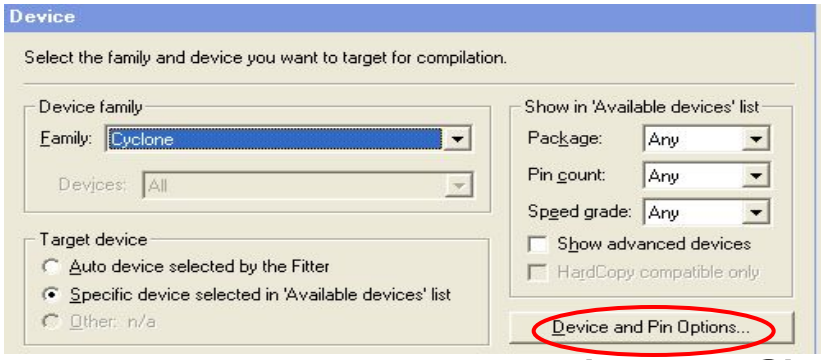


- In Family ,Choose cyclone Family Chips。

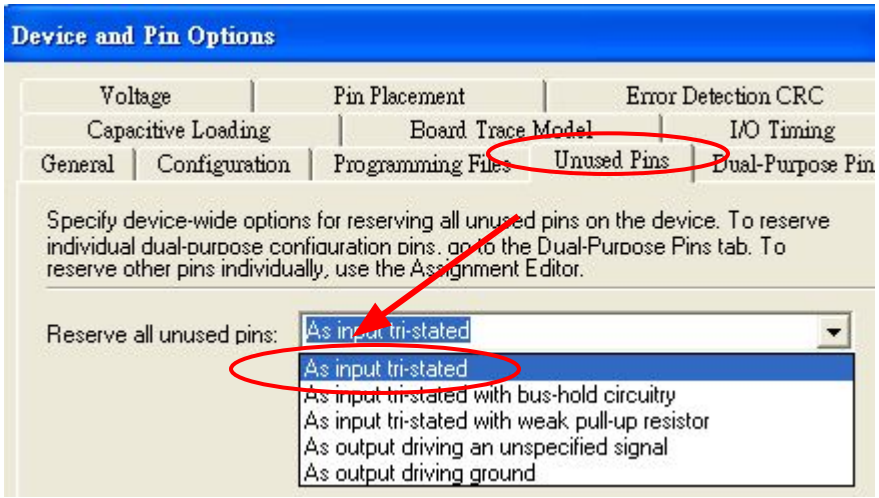


Quartus II FPGA Setting

- *Click Device & Pin Option*

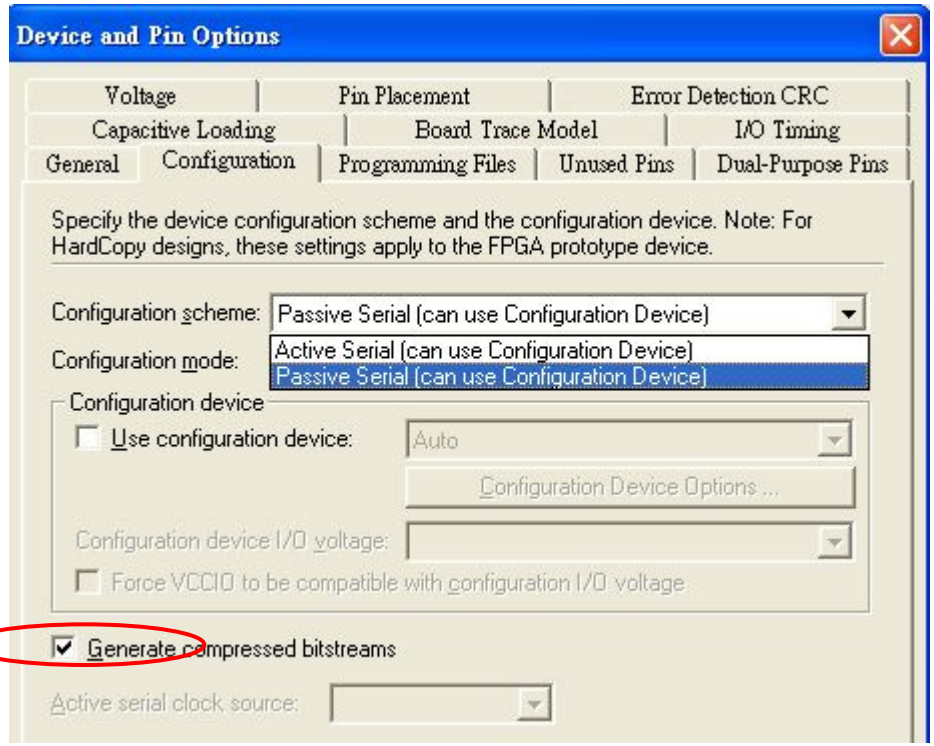


- Click Unused Pins, In Reserve all unused pins ,Choose As inputs tri-stated。



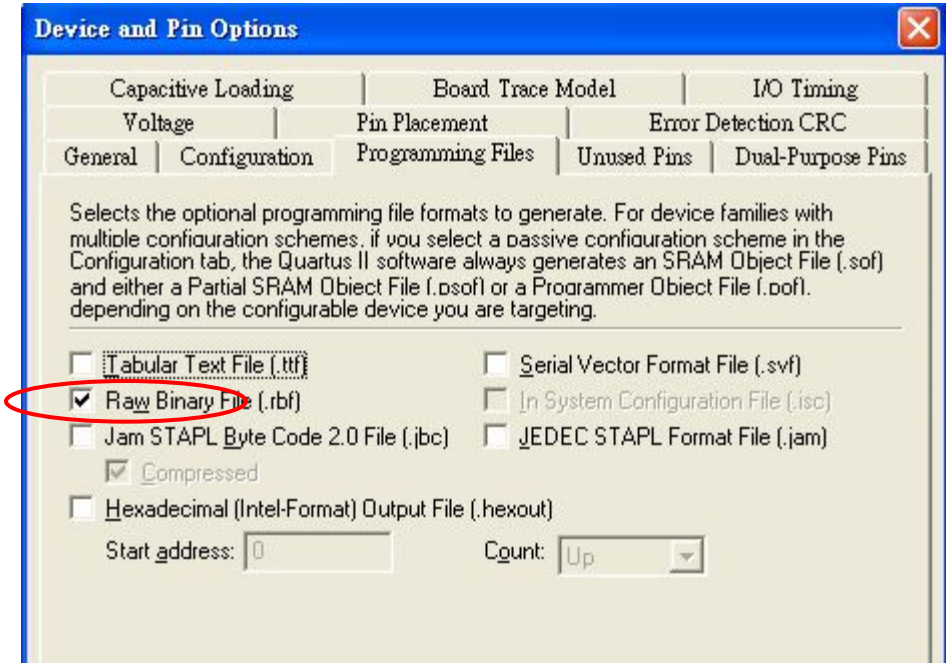
Quartus II FPGA Setting

- In the “Device & Pin Options” window, choose the “Configuration” tab. For “Configuration scheme”, select “Passive Serial ”. As well, check the “Generate compressed bitstreams” box as shown below.



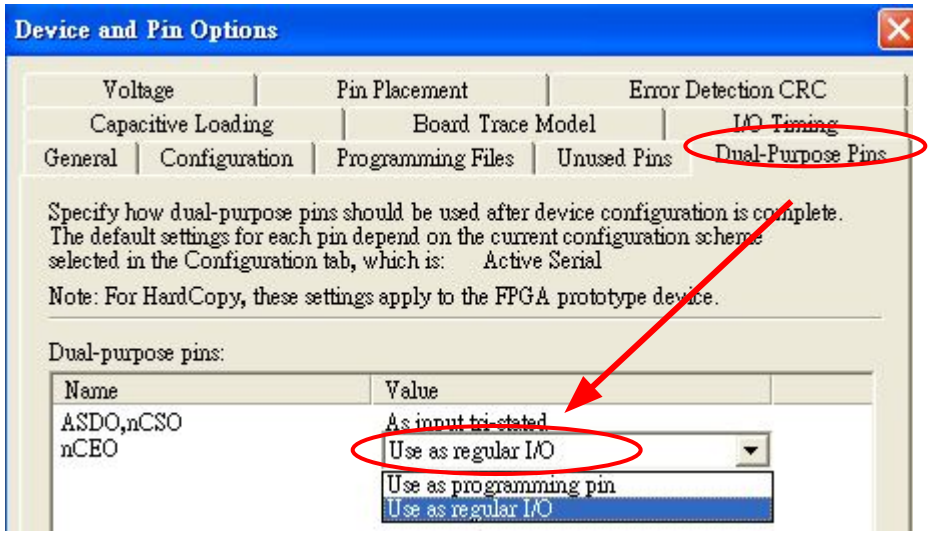
Quartus II FPGA Setting

- In the “Device & Pin Options” window, choose the “Programming Files” tab. Check the “Raw Binary File(.rbf)” box as shown below.



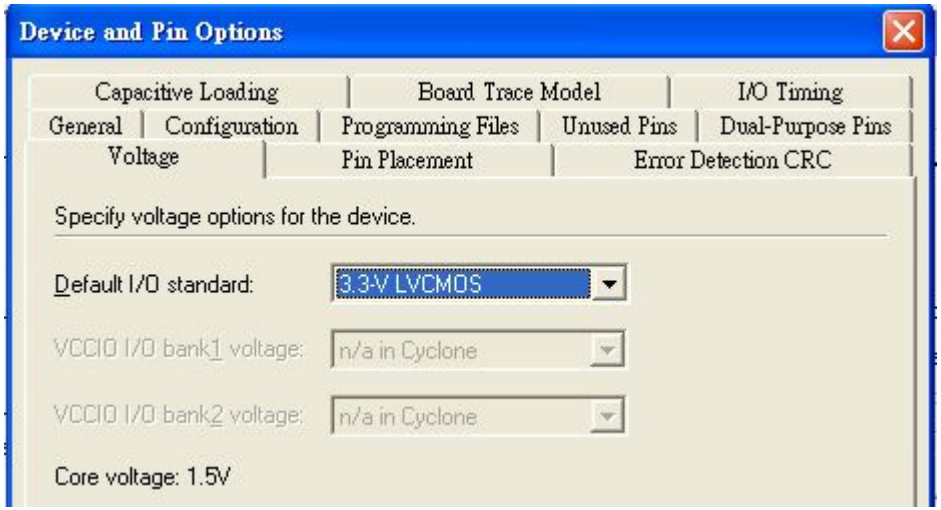
Quartus II FPGA Setting

- *Click Dual-Purpose Pins, In nCEO ,Choose Use as regular I/O。*



Quartus II FPGA Setting

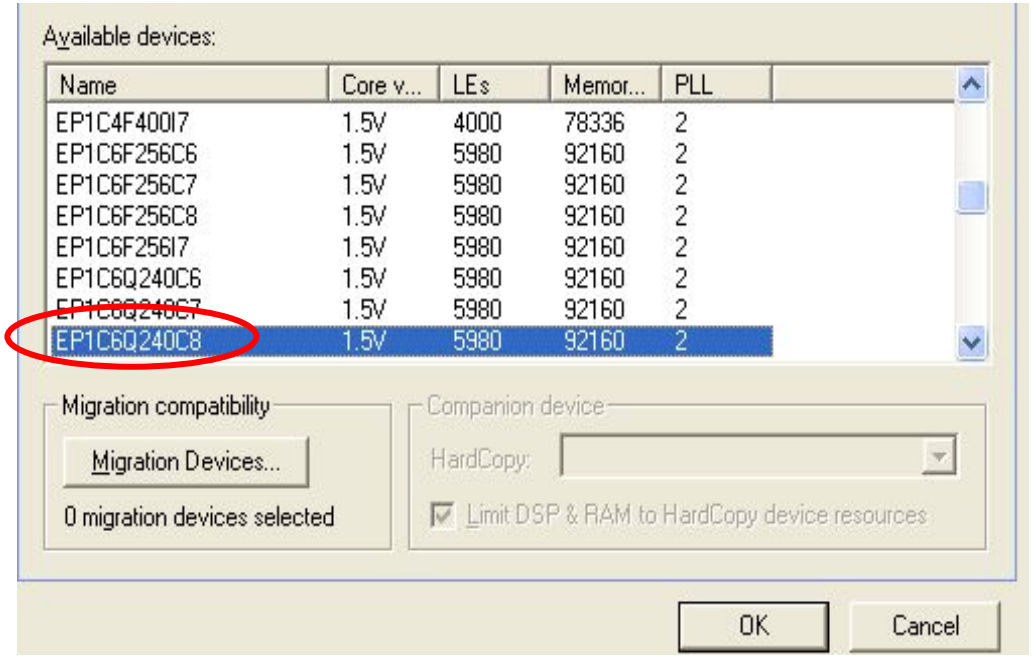
- In the “Device & Pin Options” window, choose the “Voltage” tab. For “I/O standard”, select “3.3-V LVCOMS” as shown below.



Quartus II FPGA Setting

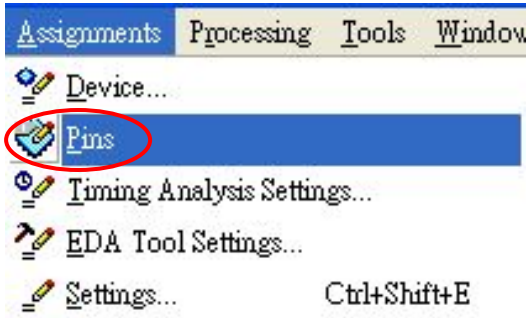
- Choose the ID of your FPGA Chip, click OK

Check your own FPGA Chip ID

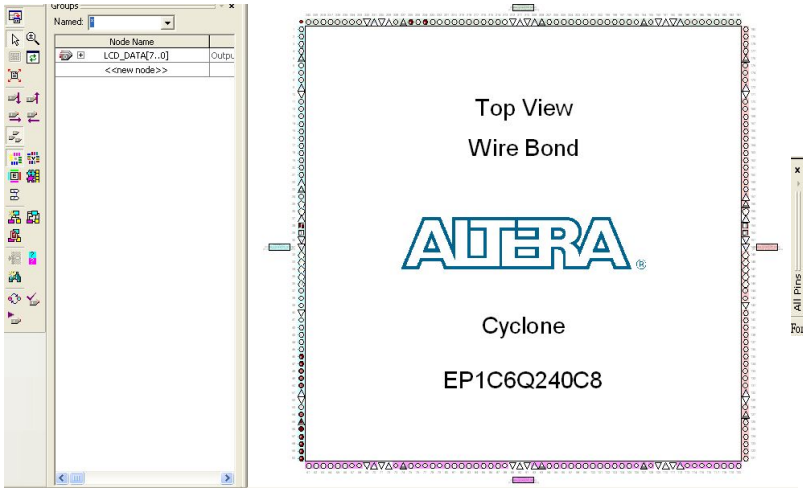


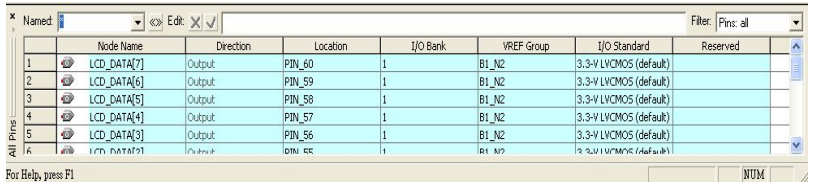
Quartus II FPGA Setting

- We've done setting Device, next we need to assign Pin location, Choose *Assignments* → *Pins*。



- You can see the pin planning window.

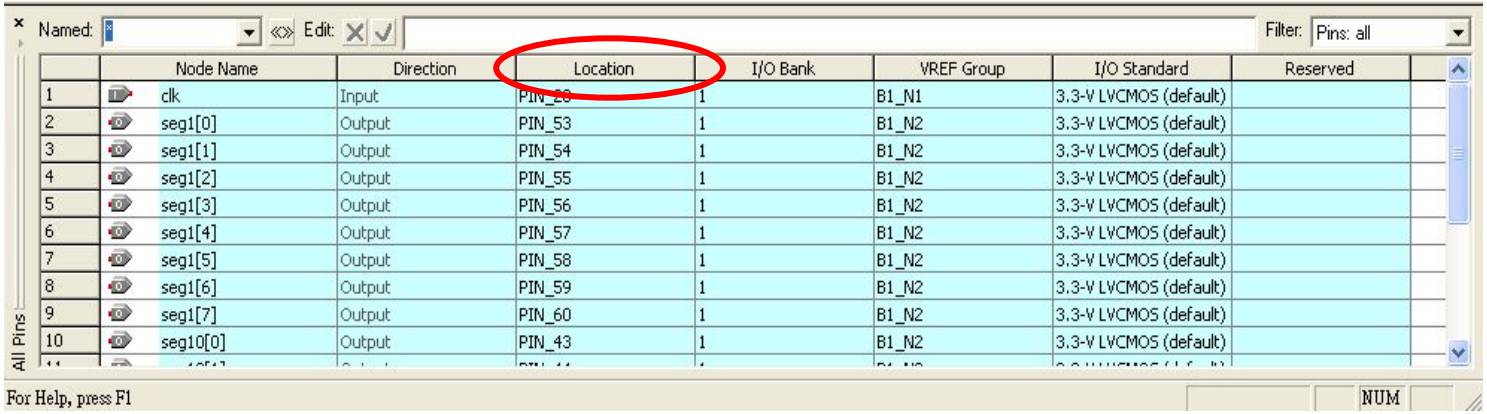




Quartus II FPGA Setting

- Pin腳設定內容請參考moodle LAB_9資料。

- Lecture 9 SMIMS_VLA_USB_Install_Manual_v3.1_EN.pdf 12-16頁。



	Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
1	clk	Input	PIN_28	1	B1_N1	3.3-V LVCMOS (default)	
2	seg1[0]	Output	PIN_53	1	B1_N2	3.3-V LVCMOS (default)	
3	seg1[1]	Output	PIN_54	1	B1_N2	3.3-V LVCMOS (default)	
4	seg1[2]	Output	PIN_55	1	B1_N2	3.3-V LVCMOS (default)	
5	seg1[3]	Output	PIN_56	1	B1_N2	3.3-V LVCMOS (default)	
6	seg1[4]	Output	PIN_57	1	B1_N2	3.3-V LVCMOS (default)	
7	seg1[5]	Output	PIN_58	1	B1_N2	3.3-V LVCMOS (default)	
8	seg1[6]	Output	PIN_59	1	B1_N2	3.3-V LVCMOS (default)	
9	seg1[7]	Output	PIN_60	1	B1_N2	3.3-V LVCMOS (default)	
10	seg10[0]	Output	PIN_43	1	B1_N2	3.3-V LVCMOS (default)	

Assign I/O PIN by clicking Location slot

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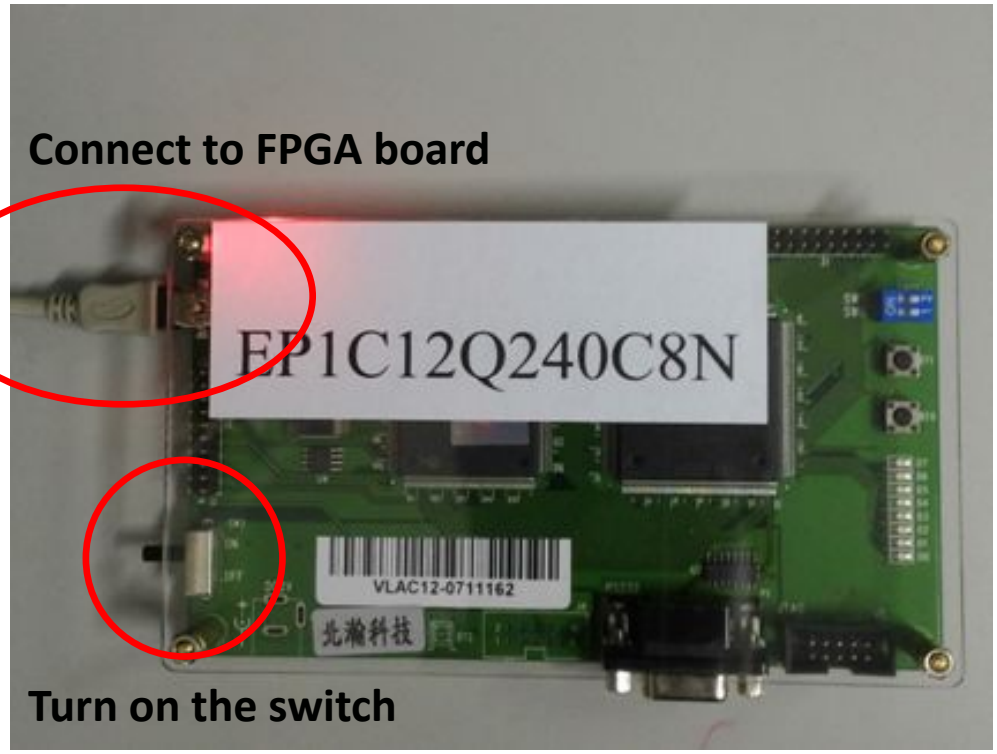
VeriLite board Setting

- Before programming your design to VeriLite Board, you have to connect VeriLite Board to PC first.

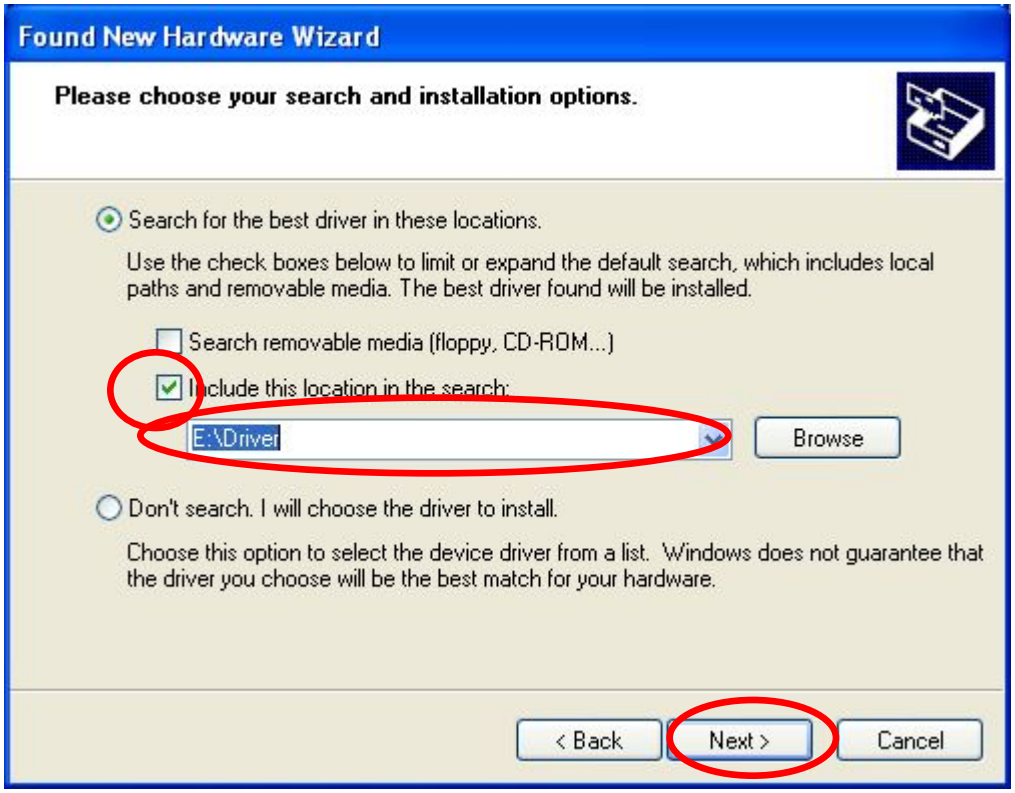


VeriLite board Setting

- Driver info will arise as board connection is triggered.
- If not, it means that your environment already has the driver.

VeriLite board Setting

- Choose “Include this location in the search”, Path is in PC’s “ CD-ROM driver”.

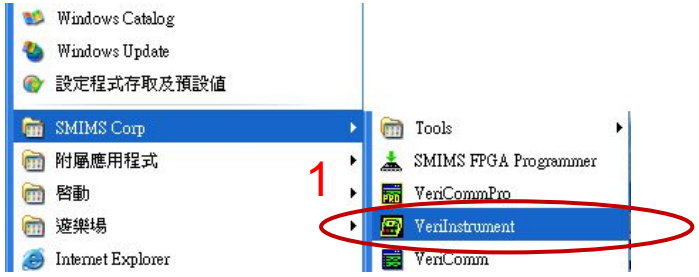


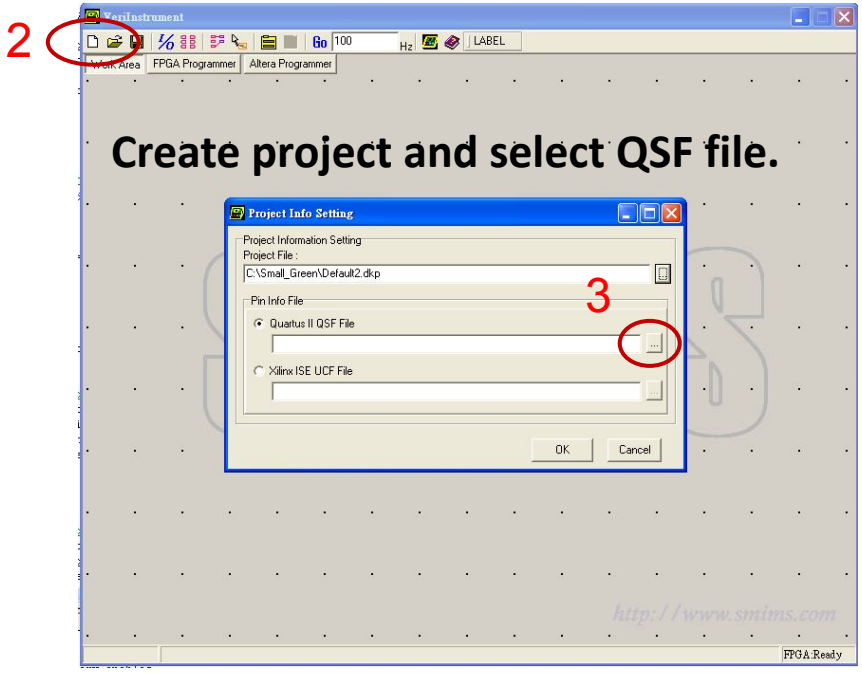
VeriLite board Setting

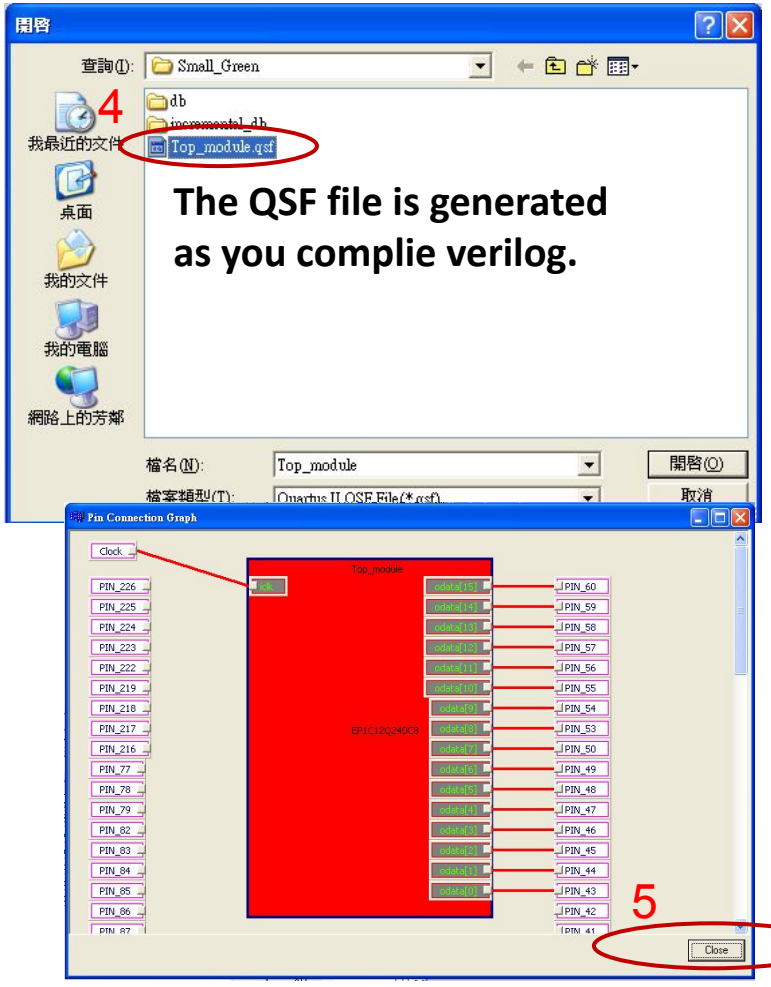
- Installed successfully。

VeriLite board Setting

- Open VeriLite Instrument (VeriInstrument) to place components.

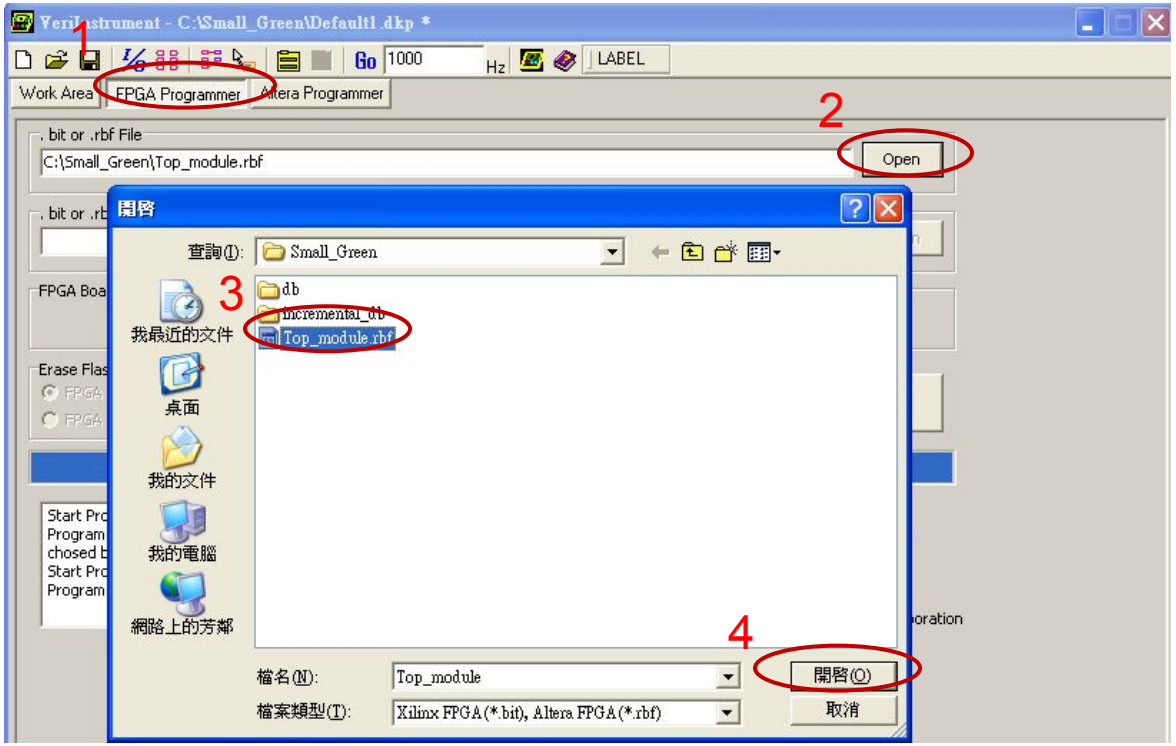






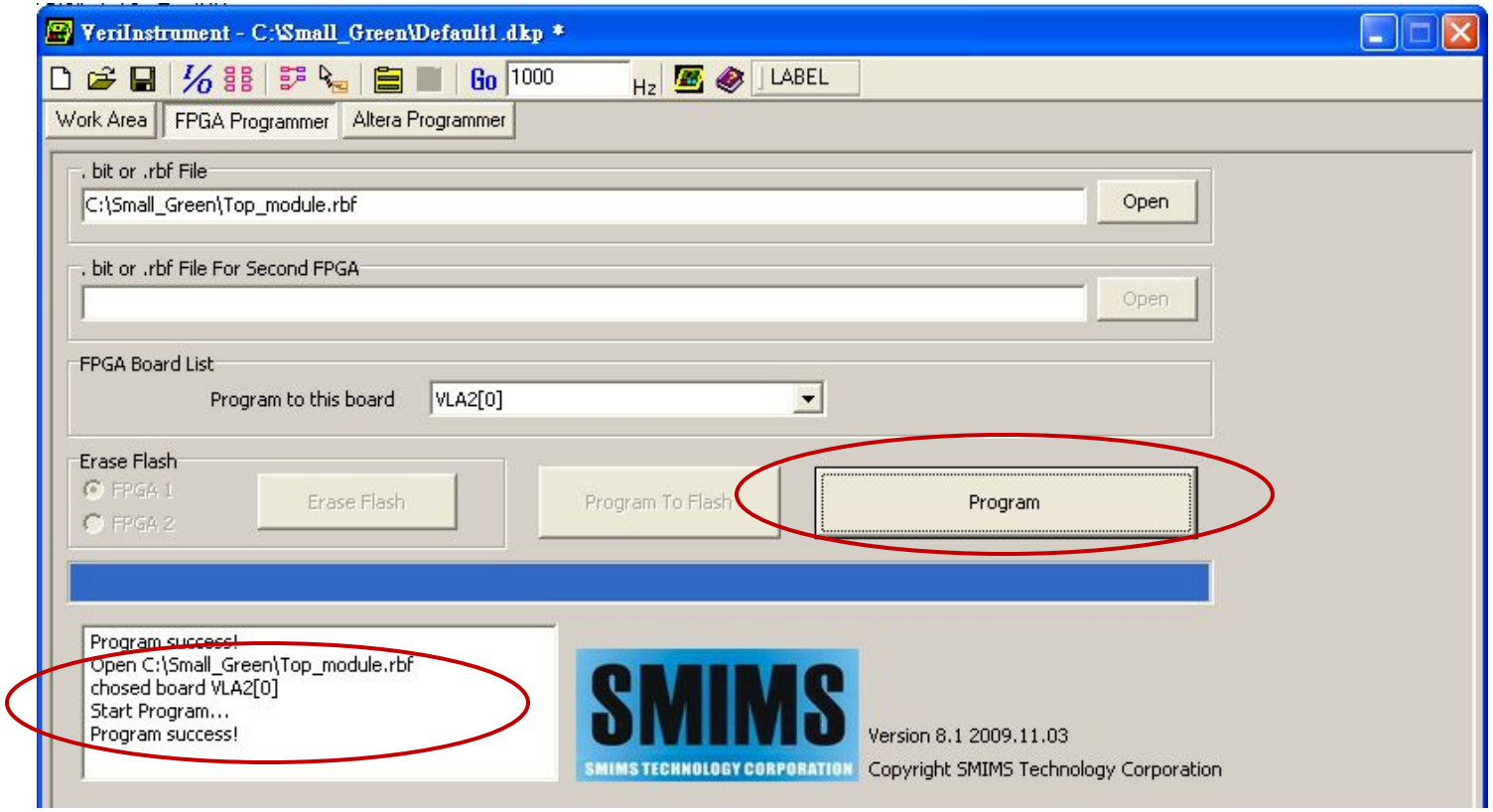
VeriLite board Setting

- Set FPGA Programmer as follow.



VeriLite board Setting

- Click program then check the result messenge.



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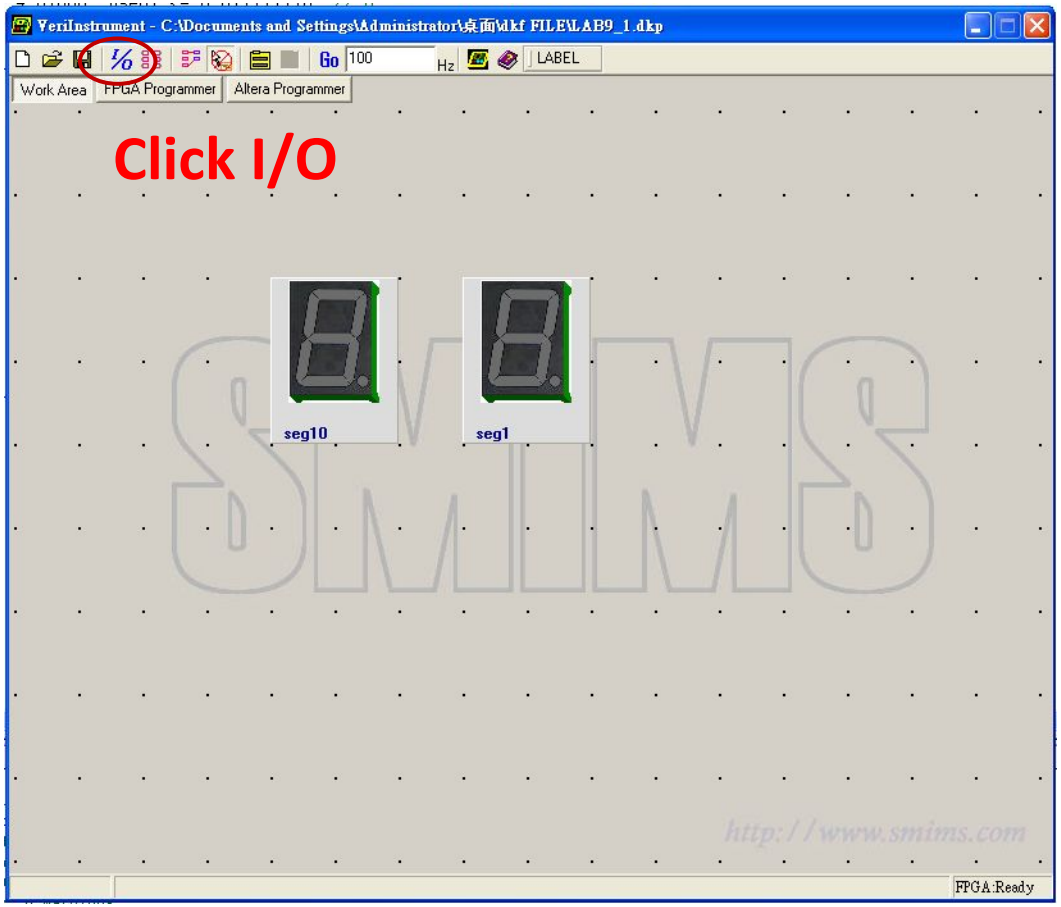
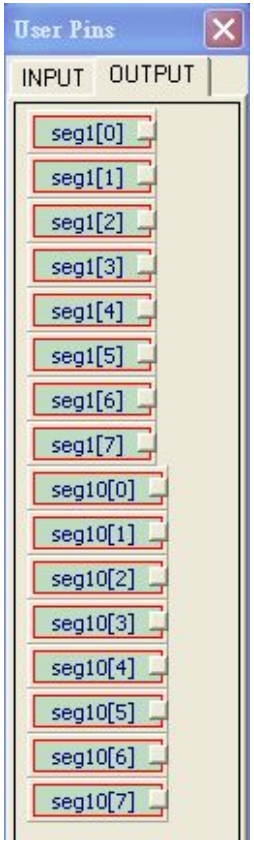
VeriInstrument usage

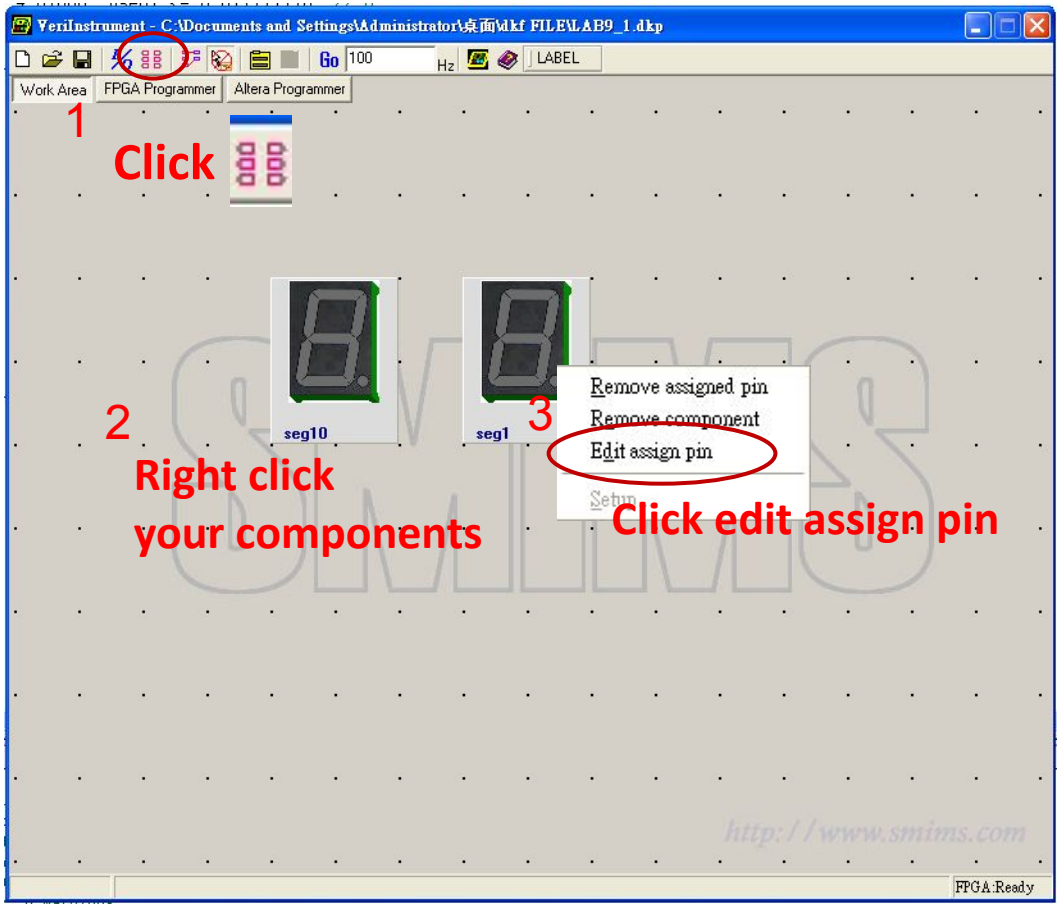
- Click I/O, you can place any components you need.



VeriInstrument usage

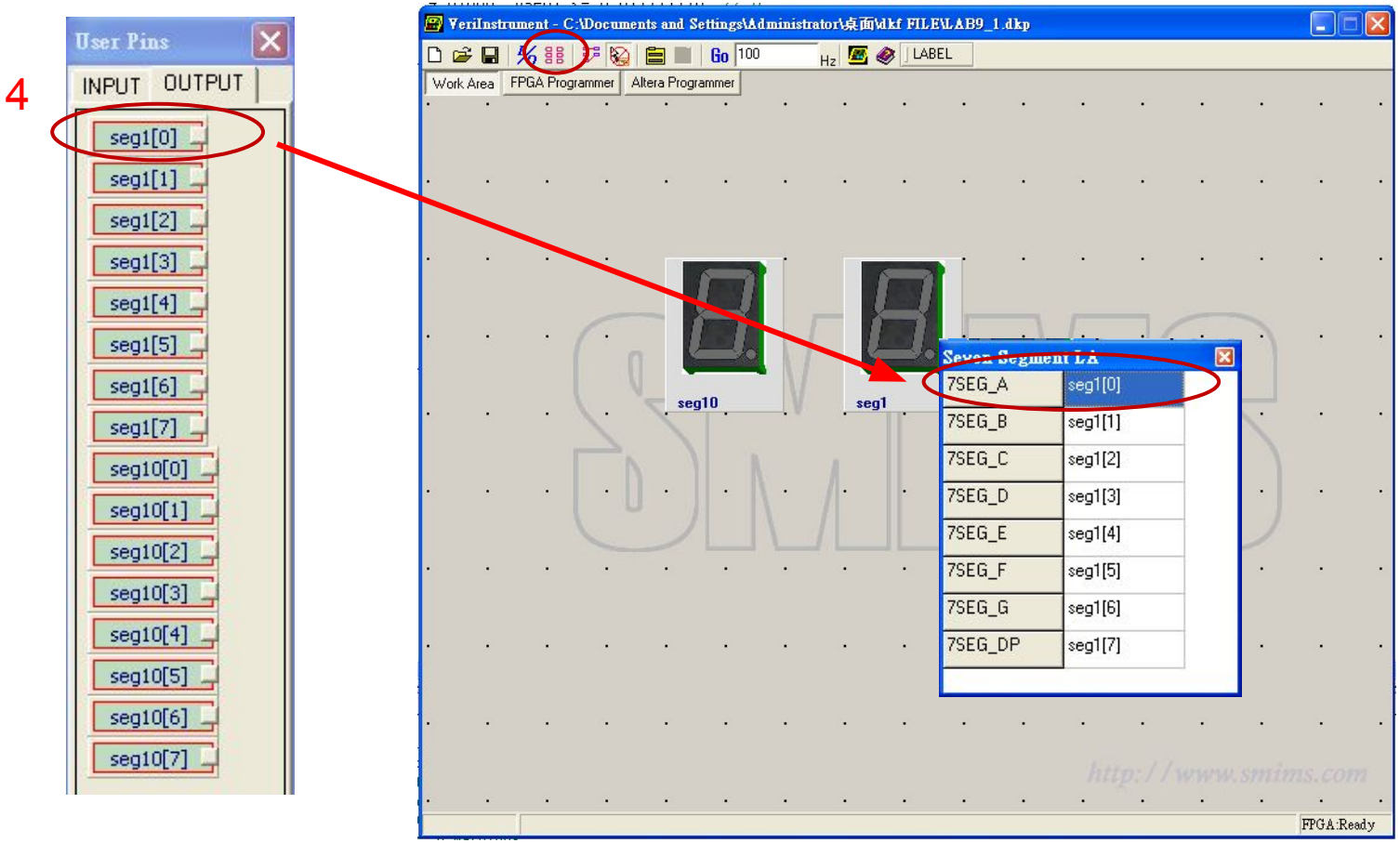
- Assign pin to your components.





VeriInstrument usage

- Drag the pin to the slot.



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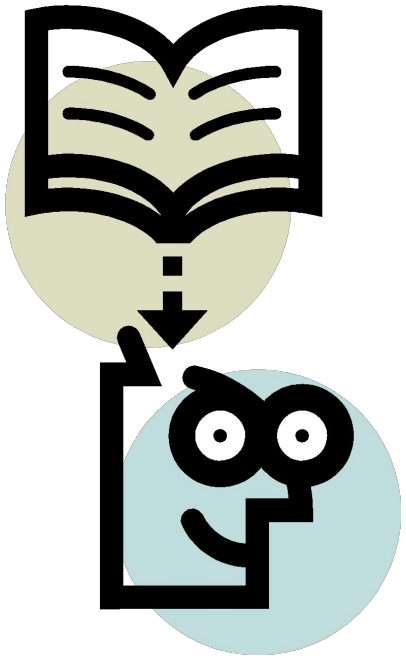
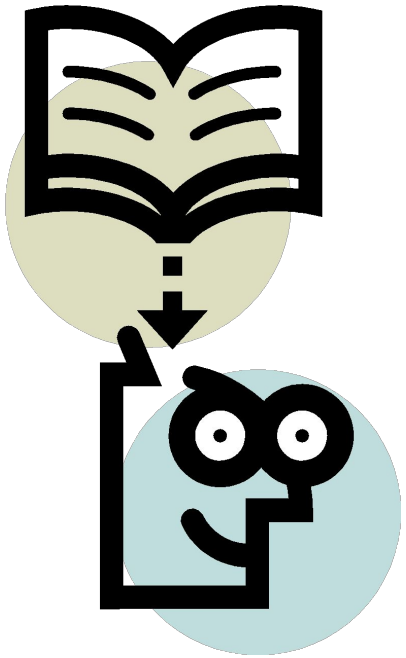
LAB 8-1

- 程式燒錄與測試。
- 輸入:按鈕開關(板子上)
- 輸出:Led(軟體上)
- 按鈕開關按下時，Led亮;
  按鈕開關放開時，Led滅。

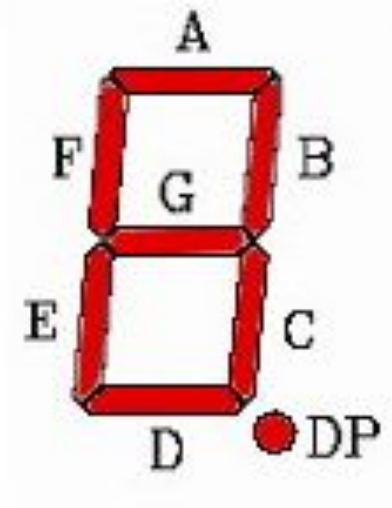


LAB 8-2

- 請設計一個計數器包含以下功能:
- 輸入:加1、加10、減1、減10
- 輸出:七段顯示器(2顆)
- 數值:0~99



七段顯示器(共陽極)



資料	DP	G	F	E	D	C	B	A	16進制
0	1	1	0	0	0	0	0	0	C0
1	1	1	1	1	1	0	0	1	F9
2	1	0	1	0	0	1	0	0	A4
3	1	0	1	1	0	0	0	0	B0
4	1	0	0	1	1	0	0	1	99
5	1	0	0	1	0	0	1	0	92
6	1	0	0	0	0	0	1	0	82
7	1	1	1	1	1	0	0	0	F8
8	1	0	0	0	0	0	0	0	80
9	1	0	0	1	0	0	0	0	90

LAB 8

下課前繳交至moodle：

上傳verilog.v

波形截圖