**Contrôleur**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Instruction** | **Op5:0** | **RegWrite** | **RegDst** | **AluSrc** | **Branch** | **MemWrite** | **MemtoReg** | **ALUOp1:0** | **Jump** |
| **R-type** | **000000** | **1** | **1** | **0** | **0** | **0** | **0** | **10** | **0** |
| **lw** | **100011** | **1** | **0** | **1** | **0** | **0** | **1** | **00** | **0** |
| **sw** | **101011** | **0** | **X** | **1** | **0** | **1** | **X** | **00** | **0** |
| **beq** | **000100** | **0** | **X** | **0** | **1** | **0** | **X** | **01** | **0** |
| **addi** | **001000** | **1** | **0** | **1** | **0** | **0** | **0** | **00** | **0** |
| **j** | **000100** | **0** | **X** | **X** | **0** | **0** | **X** | **XX** | **1** |
| **andi** | **001100 (12)** | **1** | **0** |  | **0** | **0** | **0** | **100100 (and)** | **0** |
|  |  |  |  |  |  |  |  |  |  |