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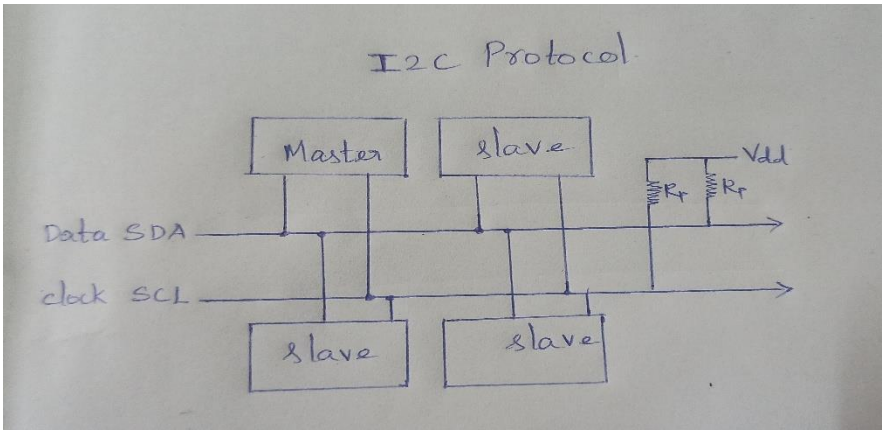
1.Write a brief summary about I2C protocol?

The I2C stands for “Inter Integrated Circuit”. It was first introduced by the Philips semiconductors in 1982. The I2C bus consists of three data transfer speeds such as standard, fast-mode and high-speed-mode. The I2C bus supports 7-bit and 10-bit address space device and its operation differ with low voltages.The I2C protocol operates three modes such as: fast mode, high-speed mode and standard mode wherein the standard mode data speed ranges 0Hz to 100Hz, and the fast mode data can transfer with 0Hz to 400 KHz speed and the high speed mode with 10 KHz to 100KHz. The 9-bit data is sent for each transfer wherein 8-bits are sent by the transmitter MSB to LSB, and the 9th bit is an acknowledgement bit sent by the receiver.

Terminology Used in I2C Protocols

Transmitter: The device that sends data to the bus is called transmitter.
Receiver: The device that receives data from the bus is called a receiver.
Master: The device that initiates transfers to generate a clock signals and terminate a transfer is called a master.
Slave: The device addressed by a master is called a slave.
Multimaster: More than one master can attempt to control the bus at the same time without corrupting the message is called a Multimaster.
Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus – only one is allowed to do so; the winning message is not corrupted.
Synchronization: Procedure to synchronize the clock singles of two or more devices is called synchronization.
The Data Read Format
Start: Primarily, the data transfer sequence is initiated by the master generating the start condition.
7-bit Address: After that the master sends the slave address in two 8-bit formats instead of a single 16-bit address.
R/W: If the read and write bit is low, then the read operation is performed.
ACK: If the write operation is performed in the slave device, then the receiver sends the 1-bit ACK to the microcontroller.
Stop: After completion of the write operation in the slave device, the microcontroller sends the stop condition to the slave device.



2. Write short text about, pull up resistor, pull down resistor, open drain, active low, active High?

Pull up resistor:

It is the most common method of ensuring that the inputs of digital logic gates and circuits can not self-bias and float about is to either connect the unused pins directly to ground (0V) for a constant low “0” input, (OR and NOR gates) or directly to Vcc (+5V) for a constant high “1” input (AND and NAND gates).

Pull down resistor:

A Pull-down resistor works in the same way as the previous pull-up resistor, except this time the logic gates input is tied to ground, logic level “0” (LOW) or it may go HIGH by the operation of a mechanical switch. This pull-down resistor configuration is particularly useful for digital circuits like latches, counters and flip-flops that require a positive one-shot trigger when a switch is momentarily closed to cause a state change.

Open Drain:

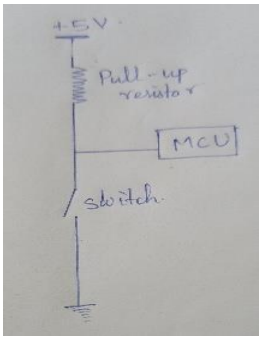
An open-drain or open-collector output pin is driven by a single transistor, which pulls the pin to only one voltage (generally, to ground). When the output device is off, the pin is left floating (open, or hi-z). Open-drain outputs are useful when multiple gates or pins are connected together, such as with the I2C bus. When a device is not using the bus, the open-drain output is in high-impedance mode and the voltage level is pulled high by the pull-up resistor. When a device drives the output low, all connected lines will go low, as they are tied together.

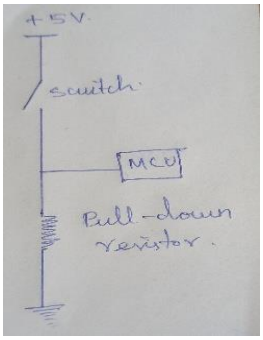
Active High:

If the signal's meaning is considered active or asserted when the input voltage is above the minimum high threshold voltage of the receiver, then it is called active high. An active high clock enable means the clock is enabled when the input is high.

Active Low:

If the signal's meaning is considered active or asserted when the input voltage is below the maximum low threshold voltage of the receiver, then it is called active low. An active low reset means the circuit is reset when the input is driven low.





3. Short text about Linux booting process and the role of Kernel?

1. BIOS

BIOS stands for Basic Input/Output System. In simple terms, the BIOS loads and executes the Master Boot Record (MBR) boot loader.When you first turn on your computer, the BIOS first performs some integrity checks of the HDD or SSD.

2.MBR

MBR stands for Master Boot Record, and is responsible for loading and executing the GRUB boot loader.The MBR is located in the 1st sector of the bootable disk, which is typically /dev/hda, or /dev/sda.

3.GRUB

The GRUB splash screen is often the first thing you see when you boot your computer. It has a simple menu where you can select some options. If you have multiple kernel images installed, you can use your keyboard to select the one you want your system to boot with. By default, the latest kernel image is selected.

4.KERNAL

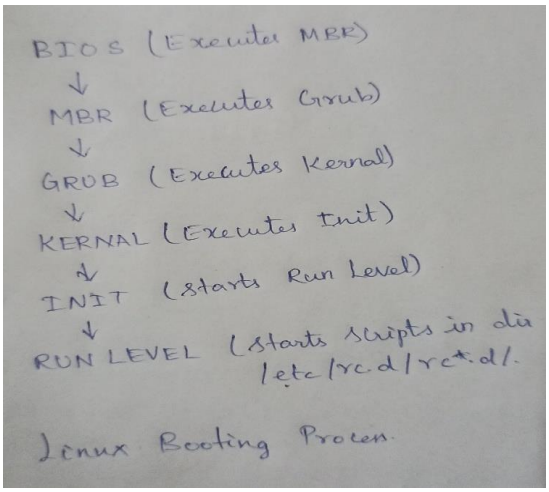
The kernel is often referred to as the core of any operating system, Linux included. It has complete control over everything in your system.In this stage of the boot process, the kernel that was selected by GRUB first mounts the root file system that's specified in the grub.config file. Then it executes the /sbin/init program, which is always the first program to be executed.

5.INIT

At this point, your system executes runlevel programs. At one point it would look for an init file, usually found at /etc/inittab to decide the Linux run level.

6.RUNLEVEL PROGRAMS

Depending on which Linux distribution you have installed, you may be able to see different services getting started.



4.Text about first impression on Zephyr RTOS?

- Optimized for low-powered, small memory footprint devices
- Build applications to target different boards, and even architectures via Device Tree.
- The Zephyr Project provides developers with feature-rich software optimized for memory constrained devices.
- Runs on systems as small as 8 kB of memory but scales up to systems with megabytes or even gigabytes of memory.
- Advanced memory management
- Long term support (LTS) with security updates
- Free to use in commercial and non-commercial solutions.
- Developed with security in mind