Task 5: Operational Amplifiers: Feedback and Stability

Optical Uplink

Joseph Arsenault
Ryan Dufour
Phil Robb

Abstract

The design, simulation and construction of a differential amplifier circuit (developed in task 4) with feedback is described. In this task a multistage op-amp with a class B output amplifier will be developed, simulated and constructed. The required differential voltage gain for this circuit is 200 $\frac{V}{V}$ while driving the smallest load possible. The uncompensated unity gain is required to be larger than 150 kHz. The gain was measured at 63.3 dB while unloaded. The smallest value for the load resistor which caused a 3 dB drop in gain was found to be 900 Ω, with a gain measured at 61.3 dB. The unity gain uncompensated unity gain frequency was measured at 2 MHz.

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1 Introduction

This report describes the design, construction, and analysis of negative feedback for an operational amplifier. This is achieved using capacitors and resistors attached to and across certain nodes in the op amp **??**

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Operational amplifiers serve an integral building block for modern electronics. Op amps provide large gain with various configuration schema. This allows the circuit designer to use the op amp in different topologies and achieve different results, all without modifying the op amp circuit itself. In addition, an op amp provides significant gain while maintaining stability, this is where the output stage comes in. The output stage allows design to accommodate for non-controllable factors such as transistor mismatch and temperature variation. The objective of this lab is to apply feedback to the op amp so that the op amp achieves the specifications as seen in Table **??**

Section 2 of this report describes the design, and when relevant, the simulations of the experiments. Experimental results and implementation are addressed in Section 3, including reasoning as to why a different circuit than the one outlined previously was constructed. A discussion of the results, sources of error, and areas of possible improvement are outlined in Section 4. Section 5 concludes this report.

2 Circuit Development

This section covers the design choices associated with the actively loaded differential amplifier with cascoded current mirror and a class B amplifier for an output stage. Frequency compensation will also be considered in the development to ensure stability.

The circuit that was developed in task 4 will be used for the purposes of this circuit development section. The output stage will be added in this task which will be a class B amplifier. The class B amplifier will consist of a 2n3904 NPN BJT and a 2n3906 PNP BJT. The simulations were conducted in Microcap 10. As these schematics are difficult to read, a set of schematics with identical values and components were created in Eagle by Autodesk. The simulated schematic can be seen in Figure 1 below.

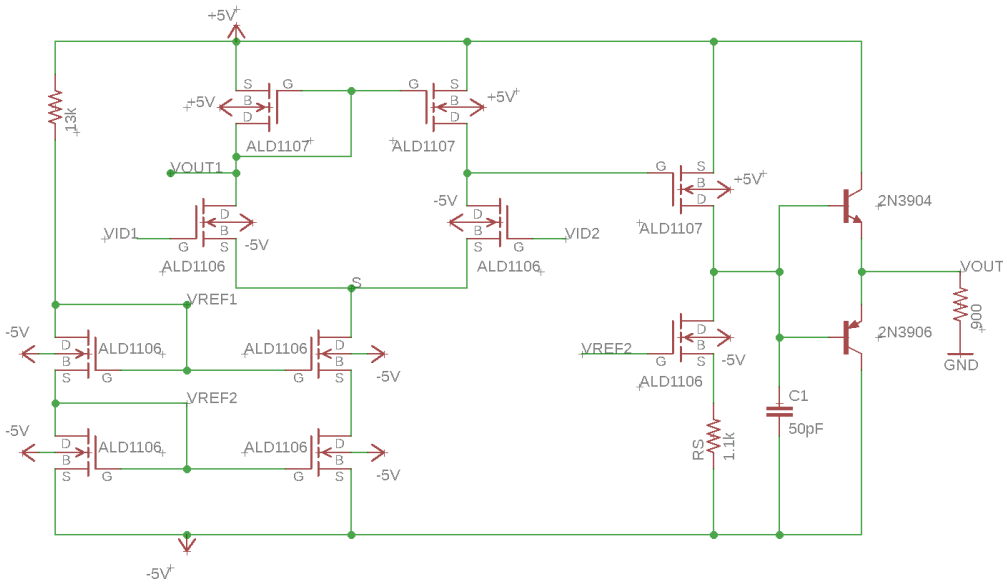

Figure 1: Simulated Circuit

The value of 13 kΩ was taken from the previous lab which gave a reference current of 401 μA. There are several specifications to meet, or at least come near for the completion of this task. The unity gain frequency should be above 150 kHz. A small load resistance of 500 Ω or less should cause a drop of 3 dB from the unloaded gain. Lastly, the gain needs to be high than 200 $\frac{V}{V}$ or 46 dB. The equation for closed loop gain is shown below in equation 1.

$$A_f(j\omega) = \frac{x_o}{x_i} = \frac{A_f(j\omega)}{1 + A_f(j\omega)\beta} \tag{1}$$

The part of the denominator, $A_f(j\omega)\beta$ is the actual loop gain for the amplifier, which it is much greater than one, then the closed loop gain is approximately $\frac{1}{\beta}$. The value of β in this case was found to be $21\frac{V}{V}$. The value for the resistor at the source of the ALD1106 NMOS, RS, was found to be 1.1k in the previous lab, and yielded similar results for this simulation, as it gave the appropriate offset nulling at the base of the BJTs at approximately zero volts. This will allow the amplifier to have it's maximum amount of gain.

The output of the amplifier met the specifications as it was simulated to have a 63.3 dB gain. To find the smallest load resistor that the amplifier could drive, Microcap 11 was used to do a sweep of load resistor values from 250 Ω to 2.5 kΩ. The goal is to find the load resistor value that will cause a 3 dB drop from the unloaded gain, which would be 60.3 dB, or at least a value close to that. The result can be seen in Figure 4 below.

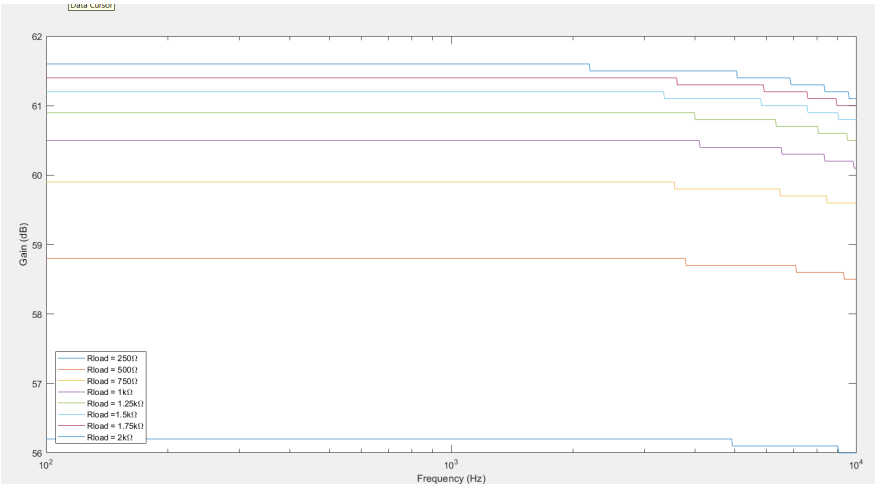

Figure 2: Sweep values of load resistor vs gain

It was found that the load of approximately 900 Ω caused a 3 dB drop in gain. A load of 500 Ω caused a 6 dB drop. Therefore, 900 is the smallest load the circuit can drive according to the simulation. Using this value for the load, a simulation was conducted and the resulting data was exported to Matlab to plot. The gain verses frequency plot at a 900 Ω load resistance is seen below in Figure 3.

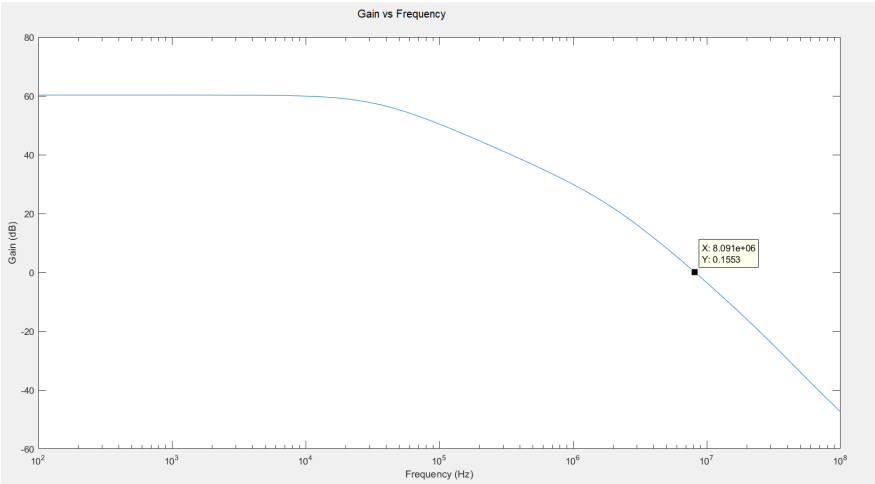

Figure 3: Gain with 900 Ω load resistance

As seen, the gain is valued at just over 60 dB, which meets the 3 dB drop in gain requirement at 900 Ω load. The zero crossing for the gain was found to be approximately 8 MHz. In order to be a stable amplifier, the phase shift should not change more than 180 degrees before the zero crossing of the gain. The resultant phase plot from simulations is see in Figure **??** below.

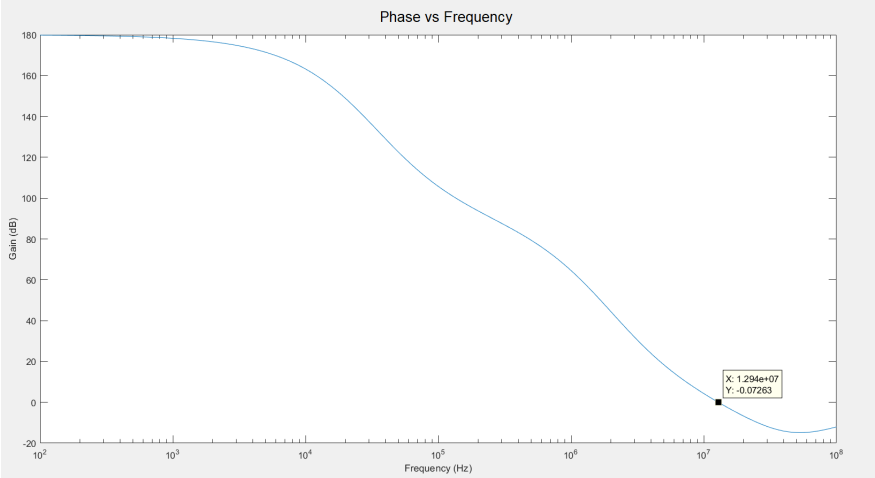

Figure 4: Phase plot with 900 Ω load resistance

Table 1: Current values from simulated circuit

Simulated current values	
I_{Ref}	410.8 μA
I_{D_1}	204.4 μA
I_{D_2}	204.4 μA
I_{CS}	$\approx$ 227 μA
I_C	$\approx$ 2 μA

Table 2: Current values from simulated circuit

Simulated voltage values	
V_{Ref_2}	-340 mV
V_{Ref_1}	-2.987 V
V_{D_1}	2.796 V
V_{D_2}	2.796 V
V_Base	9.7 μV
V_{out}	$\approx$ 0 V

3 Experimental Implementation

4 Discussion

After several minor changes, both circuits operated correctly. This lab served as introduction to the main differences between MOSFET and BJT devices. The two components are both transistors but have defining differences, mainly the polarity of the devices. The specifications are outlined in Table 3.

Table 3: BJT and NMOS comparison

BJT	Values	NMOS	Values
Q_1, Q_2, Q_3	2N3904	N_1, N_2, N_3	2N7000
R_ref	19.3kΩ	R_Ref	22kΩ
R_C	4.7kΩ	R_D	8.2kΩ
R_B	10kΩ	R_G	1MΩ
R_E	3.3kΩ	R_S	8.2kΩ
R_L	1kΩ	R_L	1kΩ
C_B, C_C, C_E	470nF	C_G, C_S, C_D	10μF
Gain	25 dB	Gain	22 dB

Notably, different voltages than those specified in the lab manual were used as the Analog Discovery handles small voltage signals very poorly, producing a lot of noise. Other than this both circuits had little issue performing as expected.

The BJT, while having a larger gain and much less 2nd harmonic distortion, did not have the required cutoff frequency to meet the specification for the optical link project, thus the NMOS CS amplifier was chosen for it's ability to meet specification.

One of the biggest challenges of this lab was the mathematical assumptions and operations used to solve for the transistor values in simulation. When dealing with such devices the assumptions used can sometimes give wildly incorrect values and lead to repetition of calculations until correct. Fortunately simulations help greatly with reducing the time it takes to get to the correct solution.

The final circuits fell well within specifications and operated correctly after minor component alterations.

5 Conclusion

The design, simulation, and construction of experiments to measure the performance of feedback to the op amp. The FINAL VALUES GO HERE. This circuit will help the circuit achieve and maintain stability of the operational amplifier in task 6. An important lesson learned during this lab was that achieving a gain too high over specification is not helpful when trying to measure values and achieving stability, which is as important as the final gain value(ADD TO / CHANGE THIS).

References

[1] D.E. Kotecki Lab.(2017) Lab #5 Voltage Amplifier [Online]. Available: http://davidkotecki.com/ECE342/labs/ECE342_2017_Lab5.pdf

[2] ON Semiconductor. (2017) 2N7000 [Online]. Available: http://www.onsemi.com/PowerSolutions/supportDoc.do?type=models&rpn=2N7000