RADAR / LADAR Signal Generator and Processor Chip

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Synopsis

A mixed-signal IC for RADAR/ LADAR signal generation and processing is proposed. The design is geared towards chirped FM RADAR / LADAR, with a specific application envisioned in miniaturized LADAR systems for robotic navigation [1]. The programmable signal generator will be based on a direct digital synthesizer (DDS) approach, and will include an RF power amplifier to drive the off-chip laser and detectors. The receiver side will include IF amplifiers, mixers, and a DSP core to convert the frequency measurement into distance and velocity information.

Background

The proliferation of autonomous vehicles, whether unmanned airborne vehicles (UAVs) or unmanned ground vehicles (UGVs), has led to the development of RADAR and LADAR systems as navigation aids [2]. An example of such applications can be found in the DARPA Urban Challenge [3]. Miniaturized robotic vehicles, such as the PackBot [4], are also gaining increased use for both military and civilian applications. A compact, miniaturized LADAR system would be a key enabler for such systems.

Proposed Work

A mixed-signal IC for LADAR signal generation and processing is proposed. The chip will output a chirped FM signal, with frequencies ranging from 100 MHz to 2 GHz. The photodetectors' outputs will be fed into the chip, where they will be mixed with the LO signal, amplified and digitized. A DSP core will be used to convert the digitized return signal into the frequency domain via a fast frequency transform (FFT). The frequency data will be analyzed to extract distance and velocity information.

Analog inputs to the chip are the return signals from the photodetector array. The analog output channel will provide the chirped FM signal. A constant amplitude of 0 dBm (1 mW a 50Ω load) will be provided across the chirp. A digital I/O bus will be used to program the chirp parameters and to read out the target information.

A DDS will be at the heart of the signal generator subsystem. A microcontroller core will be used to control the DDS parameters. The DDS output will be amplified with a wide band (100 MHz – 2 GHz) automatic gain amplifier. A constant 0 dBm amplitude will be provided across the chirp.

The receiver-side circuit will consist of a mixer, low pass filter, transimpedance amplifier (TZA) and analog-digital converter (ADC). The return RF signal will be mixed with the reference LO signal, and filtered with a low pass filter (f_c = 1 MHz) to obtain the IF signal. The IF signal will be amplified with the TZA (gain = 10 MΩ) and digitized.

The DSP core will be used to convert the resulting data for each chirp period to the frequency domain via a fast frequency transform. The relative amplitudes of the frequency peaks will a function of target distance, while their absolute amplitude will be a function of both distance and reflectivity. The frequency shift from their reference positions will be due to the Doppler effect, and a measure of target velocity. This information, on a pixel-by-pixel basis, will be output via the digital I/O bus, for each chirp period.

Past Experience

Dr. Emanetoglu received his B.S. in Electronics and Communications Engineering from the Istanbul Technical University in 1995, and his M.S. and Ph.D. in Electrical and Computer Engineering from Rutgers the State University of New Jersey in 1998 and 2003, respectively. At ITU, Dr. Emanetoglu designed an 8 bit 31 word programmable Rank-Order-Filter using capacitive threshold logic, including logic & circuit design, layout and simulation using CADENCE tools. Dr. Emanetoglu was an Oak Ridge Associated Universities (ORAU) post-doctoral research fellow at the US Army Research Laboratory (ARL), where he worked on device- and system-level LADAR development. Dr. Emanetoglu moved to the University of Maine in January of 2007.

Dr. Kotecki received his B.S. in Electrical Engineering from The University of Dayton in 1988, and his M.S. and Ph.D. in Engineering Applied Science from The University of California at Davis in 1984 and 1988, respectively. After working for eleven years in the Microelectronics Division of IBM, Dr. Kotecki joined the faculty in the Electrical and Computer Engineering Department at The University of Maine in 1999. He is currently an Associate Professor and his research is in the areas of electronic materials, high–speed mixed–signal circuits, and computer modeling.

Mr. Nikolic graduated with his B.S. in Electrical Engineering at the University of Maine in 2006. Before obtaining his A.S. in Electronics Technology at Southern Maine Community College in 2001, Mr. Nikolic attended Electronic Engineering Technology Program at Cork Institute of Technology, Cork, Ireland on a George J. Mitchell Peace Scholarship. In ECE547 VLSI Design / Layout class at the University of Maine, Mr. Nikolic has designed a Direct Digital Synthesizer (DDS) where he performed CMOS transistor level design, simulation, layout, verification, and parasitic extraction.

References

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[3] DARPA Urban Challenge website at http://www.darpa.mil/GrandChallenge/index.asp

[4] iRobot PackBot site at http://www.irobot.com/sp.cfm?pageid=109