Task 5: Operational Amplifiers: Feedback and Stability

Optical Uplink

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Abstract

The design, simulation and construction of a differential amplifier circuit (developed in task 4) with feedback is described. In this task a multistage op-amp with a class B output amplifier will be developed, simulated and constructed. The required differential voltage gain for this circuit is 200 $\frac{V}{V}$ while driving the smallest load possible. The uncompensated unity gain is required to be larger than 150 kHz. The gain was measured at 63.3 dB while unloaded. The smallest value for the load resistor which caused a 3 dB drop in gain was found to be 900 Ω, with a gain measured at 61.3 dB. The unity gain uncompensated unity gain frequency was measured at 2 MHz.

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1 Introduction

This report describes design, implementation and test of two voltage amplifiers. One consisting of negative metal oxide semconducting field effect transistors (NMOS). The other comprised of bipolar junction transistors. Figure **??** demonstrates where in the optical uplink project the voltage amplifier is placed.

The voltage amplifier is required by the optical uplink project. The output signal from the multi-feedback bandpass filter (MFBP) is in the hundreds of millivolt range. In order to make a more easily detectable signal, a voltage amplifier is required. This can achieved through the use of either a common source or common emitter amplifier. The specifications for this lab are summarized in Table 1.

Table 1: Voltage amplifier specifications

Specifications	Required
Peak gain, with load	21 dB ± 1dB%
Bias current for N_1	1mA
Lower cut-off frequency	≥100 mA
Upper cut-off frequency	at least 200 kHz
R_{in}, small signal	at least 1 MΩ
R_{out}, small signal	at least 3 kΩ
2^{nd} Harmonic distortion @ 1kHz	<2%
Supply voltages	±12 V

The voltage amplifier circuit receives the voltage signal from the MFBP and increases the amplitude of the voltage wavefrom. The desired final output being 5 V. This is achieved with either the use of a NMOS common source amplifier or an NPN BJT common emitter amplifier.

Section 2 of this report describes the design and simulations of the common source amplifier and the common emitter amplifier. Experimental results are addressed in section 3. A discussion of the results, sources of error, and areas of possible improvement are outlined in section 4. Section 5 concludes this report.

2 Circuit Development

This section covers the design choices associated with the actively loaded differential amplifier with cascoded current mirror and a class B amplifier for an output stage. Frequency compensation will also be considered in the development to ensure stability.

The circuit that was developed in task 4 will be used for the purposes of this circuit development section. The output stage will be added in this task which will be a class B amplifier. The class B amplifier will consist of a 2n3904 NPN BJT and a 2n3906 PNP BJT. The simulations were conducted in Microcap 10. As these schematics are difficult to read, a set of schematics with identical values and components were created in Eagle by Autodesk. The simulated schematic can be seen in Figure 1 below.

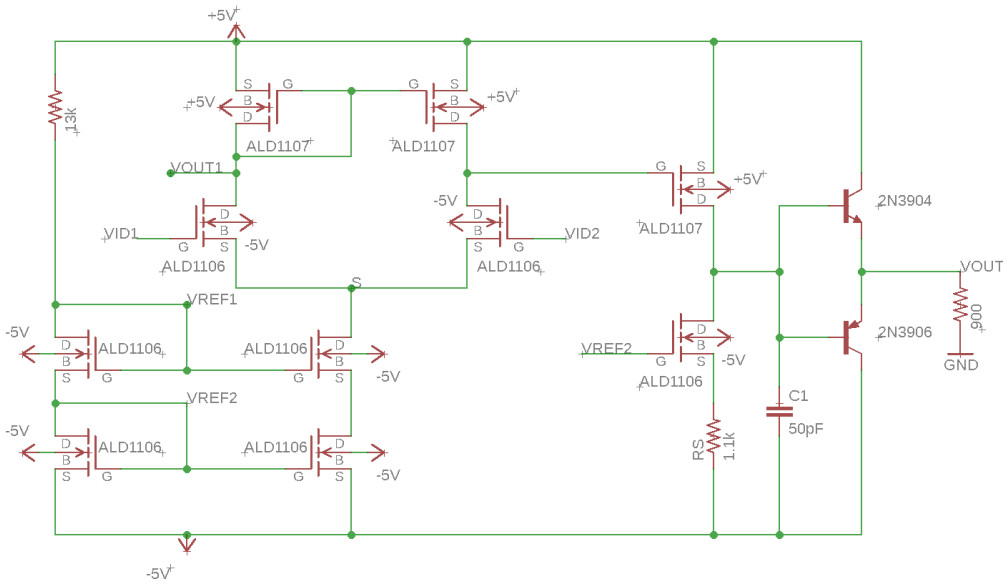

Figure 1: Simulated Circuit

The value of 13 kΩ was taken from the previous lab which gave a reference current of 401 μA. There are several specifications to meet, or at least come near for the completion of this task. The unity gain frequency should be above 150 kHz. A small load resistance of 500 Ω or less should cause a drop of 3 dB from the unloaded gain. Lastly, the gain needs to be high than 200 $\frac{V}{V}$ or 46 dB. The equation for closed loop gain is shown below in equation 1.

$$A_f(j\omega) = \frac{x_o}{x_i} = \frac{A_f(j\omega)}{1 + A_f(j\omega)\beta} \tag{1}$$

The part of the denominator, $A_f(j\omega)\beta$ is the actual loop gain for the amplifier, which it is much greater than one, then the closed loop gain is approximately $\frac{1}{\beta}$. The value of β in this case was found to be $21\frac{V}{V}$. The value for the resistor at the source of the ALD1106 NMOS, RS, was found to be 1.1k in the previous lab, and yielded similar results for this simulation, as it gave the appropriate offset nulling at the base of the BJTs at approximately zero volts. This will allow the amplifier to have it's maximum amount of gain.

The output of the amplifier met the specifications as it was simulated to have a 63.3 dB gain. To find the smallest load resistor that the amplifier could drive, Microcap 11 was used to do a sweep of load resistor values from 250 Ω to 2.5 kΩ. The goal is to find the load resistor value that will cause a 3 dB drop from the unloaded gain, which would be 60.3 dB, or at least a value close to that. The result can be seen in Figure 4 below.

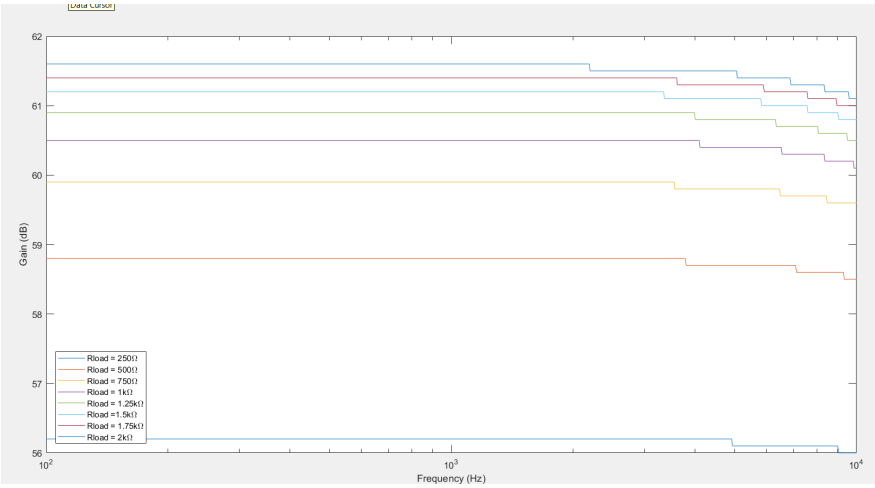

Figure 2: Sweep values of load resistor vs gain

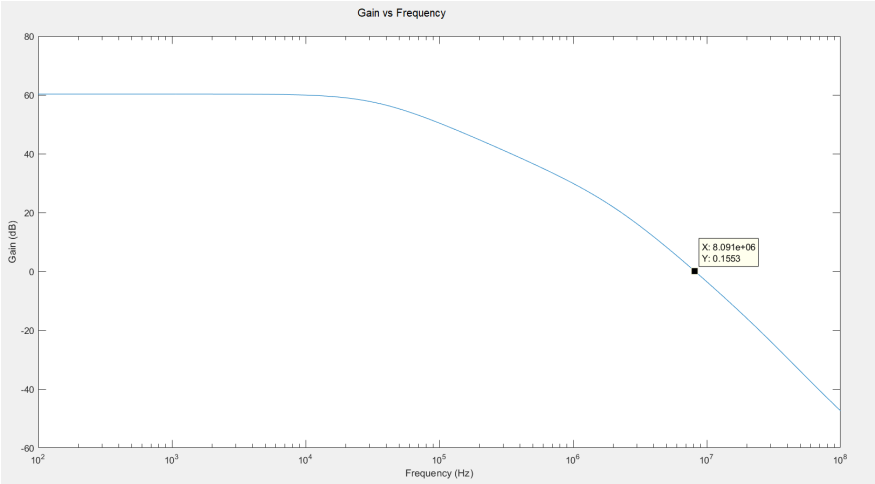

Figure 3: Gain with 900 Ω load resistance

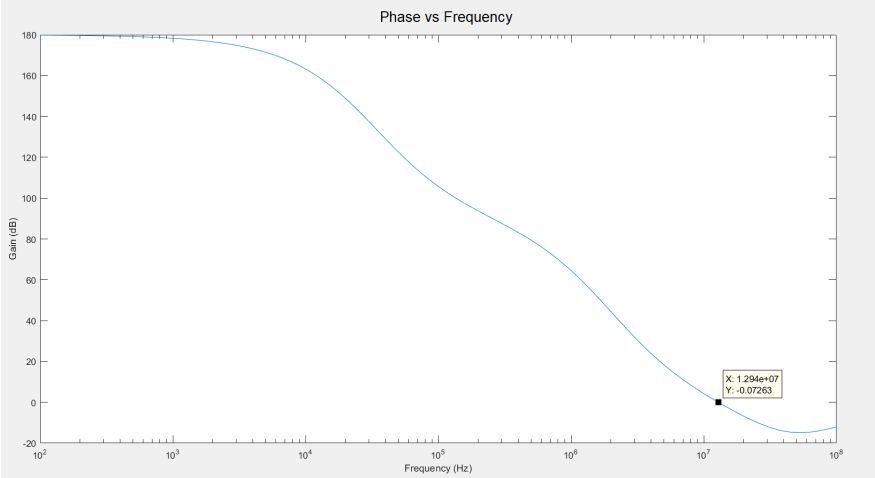

Figure 4: Phase plot with 900 Ω load resistance

3 Experimental Implementation

The circuits required only minor changes from simulation to experimental implementation.

3.1 NMOS amplifier

The final circuit is shown in Figure **??**.

Some of the resistor values had to be changed in order to meet specifications. The capacitors had to be increased as well due to the poor performance of the equivalent nominal value electrolytics. The implemented capacitors are parallel plate which operate better at higher frequencies. Figure **??** demonstrates the experimental frequency response of the NMOS amplifier.

The gain was just on the high end of the specification at 22 dB. The lower cutoff frequency is less than 1 kHz. The upper cutoff also meets spec by being greater than 200 kHz. The FFT of the circuit can by seen in Figure **??**.

The second harmonic distortion was slightly too high at 5%. This can be altered by the negative bias voltage, for the purpose of this lab, 5% was deemed acceptable. Table 2 shows the summary of the experimental NMOS circuit.

Table 2: NMOS experimental values

Q_1, Q_2, Q_3	2N7000
R_ref	22 kΩ
R_g	1 MΩ
R_d	8.2 kΩ
R_s	8.2 kΩ
R_L	1kΩ
C_B, C_C, C_E	10 μF
Gain	21 dB
Lower cutoff	600 Hz
Upper cutoff	10 MHz

After minor alterations the circuit operated correctly.

3.2 BJT amplifier

The BJT required only a slight change of capacitor values, due to availability. Figure **??** shows the final circuit for the BJT amplifier circuit.

The BJT was built using the provided components. The experimental frequency response of the circuit is shown in Figure **??**.

The gain was a little less than the simulated, at 24 dB, but the lower cutoff was quite higher at 6 kHz, far higher than the specified 1 kHz. The upper cutoff can not be measured exactly due to the limitations of the Digilent Discovery board's network analyzer. The measured values are only accurate up to 500 kHz. The measured FFT of the BJT can be seen in Figure **??**.

The second harmonic distortion was significantly less than the NMOS while still being in spec, at roughly 1%. Table 3 shows the summary of the BJT performance.

Table 3: BJT experimental values

Q_1, Q_2, Q_3	2N3904
R_ref	19.3kΩ
R_C	4.7kΩ
R_B	10kΩ
R_E	3.3kΩ
R_L	1kΩ
C_B, C_C, C_E	470nF
Gain	25 dB
Lower cutoff	6 kHz
Upper cutoff	>500 kHz

Overall, the BJT operated as expected, discussion and comparison of the two circuits can be found in Discussion.

4 Discussion

After several minor changes, both circuits operated correctly. This lab served as introduction to the main differences between MOSFET and BJT devices. The two components are both transistors but have defining differences, mainly the polarity of the devices. The specifications are outlined in Table 4.

Table 4: BJT and NMOS comparison

BJT	Values	NMOS	Values
Q_1, Q_2, Q_3	2N3904	N_1, N_2, N_3	2N7000
R_ref	19.3kΩ	R_Ref	22kΩ
R_C	4.7kΩ	R_D	8.2kΩ
R_B	10kΩ	R_G	1MΩ
R_E	3.3kΩ	R_S	8.2kΩ
R_L	1kΩ	R_L	1kΩ
C_B, C_C, C_E	470nF	C_G, C_S, C_D	10μF
Gain	25 dB	Gain	22 dB

Notably, different voltages than those specified in the lab manual were used as the Analog Discovery handles small voltage signals very poorly, producing a lot of noise. Other than this both circuits had little issue performing as expected.

The BJT, while having a larger gain and much less 2nd harmonic distortion, did not have the required cutoff frequency to meet the specification for the optical link project, thus the NMOS CS amplifier was chosen for it's ability to meet specification.

One of the biggest challenges of this lab was the mathematical assumptions and operations used to solve for the transistor values in simulation. When dealing with such devices the assumptions used can sometimes give wildly incorrect values and lead to repetition of calculations until correct. Fortunately simulations help greatly with reducing the time it takes to get to the correct solution.

The final circuits fell well within specifications and operated correctly after minor component alterations.

5 Conclusion

The design, simulation, and implementation of a voltage amplifier have been explained. The specifications required, for the purposes of use in the optical uplink project, are a lower cutoff frequency of $\leq$ 1kHz, upper cutoff frequency of 200 kHz, and a peak gain of 21 dB $\pm$ 1 dB. Also, the 2nd Harmonic distortion for a 20 mVp-p sinusoidal signal at 1 kHz must be $< 2\%$. The sinusoidal source was 20 mV_{P-P} at 1kHz, and the supply voltages were $\pm$ 12V. This resulted in a lower cutoff frequency of approximately 600 Hz and the upper cutoff frequency was in the MHz range, which exceeds the required $\geq$ 200 kHz. The 2nd harmonic distortion was measured to be approximately 5%. An important lesson was learned about the comparison between a voltage amplifier using NMOS components and a voltage amplifier using BJT components.

References

[1] D.E. Kotecki Lab.(2017) Lab #5 Voltage Amplifier [Online]. Available: http://davidkotecki.com/ECE342/labs/ECE342_2017_Lab5.pdf

[2] ON Semiconductor. (2017) 2N7000 [Online]. Available: http://www.onsemi.com/PowerSolutions/supportDoc.do?type=models&rpn=2N7000