Task 4: LED Driver

Optical Uplink

Joseph Arsenault
Ryan Dufour
Phil Robb

Abstract

The design, simulation, and construction of an LED driver circuit are described. In task 4 of the optical uplink project, a signal conditioning circuit and current driver are explored. A signal conditioner using the MCP6004 operational amplifier as a Schmitt trigger was built in order to output a square wave with 50% duty-cycle. The current driver was constructed using a MCP6004 operational amplifier which drives an 2N3904 BJT. The current driver receives the output voltage from the conditioner and converts it to a current signal. The output of LED driver was required to operated at approximately 20 kHz, 50% duty-cycle, with a current of 100mA amplitude. a sinusoidal wave form, at a frequency of 20.1 kHz, a duty cycle of 50.1% and 150mA peak amplitude.

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Contents

1 Introduction **1**

2 Circuit Development **1**

2.1 Ring Oscillator 1

2.2 Signal Conditioner 3

2.3 Current Driver 3

2.4 Voltage Regulator 4

3 Experimental Implementation **5**

3.1 Ring Oscillator 5

3.2 Signal Conditioner 5

3.3 Current Driver 5

4 Discussion **6**

4.1 NMOS inverter 6

4.2 CMOS inverter 7

4.3 AND gate 7

4.4 Ring oscillator 7

5 Conclusion **8**

List of Figures

1 Block diagram for optical uplink [1] 1

2 CMOS ring oscillator schematic 2

3 Simulated CMOS ring oscillator output 2

4 Generic current driver circuit [2] 3

5 Simulated current 4

6 Voltage regulator 4

7 Simulated circuit 5

8 Experimental signal conditioner 6

List of Tables

1 Simulated Results 5

2 Comparison of NMOS 6

3 CMOS inverter comparison 7

4 Truth Table: AND 7

5 Comparison of ring oscillator results 8

1 Introduction

This report describes the design, implementation and test of an LED driver.

This report describes the design, implementation and test of a signal generator using various NMOS and CMOS inverter designs. Two different signal generators were designed, an astable multivibrator and a ring oscillator. Notably, negative metal oxide semiconducting field effect transistors (NMOS), complementary metal oxide semiconducting field effect transistors (CMOS), and finally the conjunction of the two to form an AND logic gate. Figure 1 demonstrates where in the optical uplink project the signal generator is placed. The signal generator creates the waveform that drives the LED that is detected by the photodetector.

Figure 1: Block diagram for optical uplink [1]

The output from the the signal generator is not a square wave, nor does it output enough current to drive the LED. The current driver will be created in a subsequent lab. The voltage transfer characteristics (VTC) of an ideal inverter is shown in Figure **??**.

Figure **??** describes the ideal VTC of an inverter, where the voltages for logic low and logic high are shown. Both the ring oscillator and the astable multivibrator are created by cascading several CMOS inverters together,

Section 2 of this report describes the design, and when relevant, the simulations of the NMOS, CMOS inverter, the AND gate, the ring oscillator, and finally the astable multivibrator. Experimental results are addressed in section 3. A discussion of the results, sources of error, and areas of possible improvement are outlined in section 4. Section 5 concludes this report.

2 Circuit Development

This section covers the design choices associated with the various circuits constructed. The individual circuits designed were a Schmitt trigger configured op amp as the signal conditioner and an op amp driving a BJT for the current driver. The input waveform was generated using the ring oscillator from Lab 3. The supply voltage was created using a voltage regulator.

The order in which the circuits are discussed is as follows: first, the ring oscillator, followed by the signal conditioner, then the current driver, and then finally the voltage regulator..

2.1 Ring Oscillator

The design of the CMOS ring oscillator consists of three CMOS inverters connected in series with the output of the last inverter connected to the input of the first inverter. The ring oscillator will also have a capacitor at each output connected to ground. The schematic for the CMOS ring oscillator can be seen in

Figure 2.

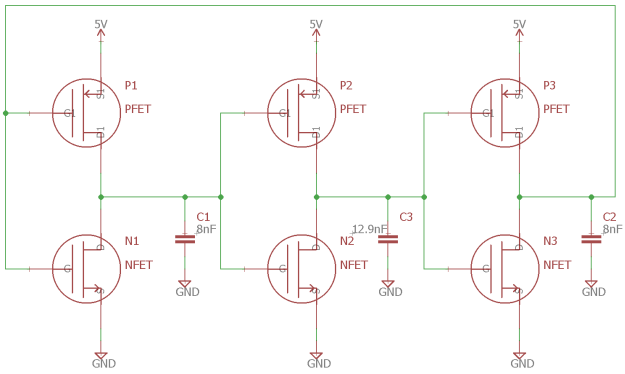

Figure 2: CMOS ring oscillator schematic

The operation of the ring oscillator uses a series of inverters. The output of one inverter inverts the input signal. Therefore, if there are a series of inverters, then each odd inverter will have the same inverted output as the first. In this instance, there are three stages of inverters used, with the output of the third inverter being fed back into the input of the first inverter. This feedback from the output to the input causes an oscillation. The simulated output of the ring oscillator is depicted in Figure 3.

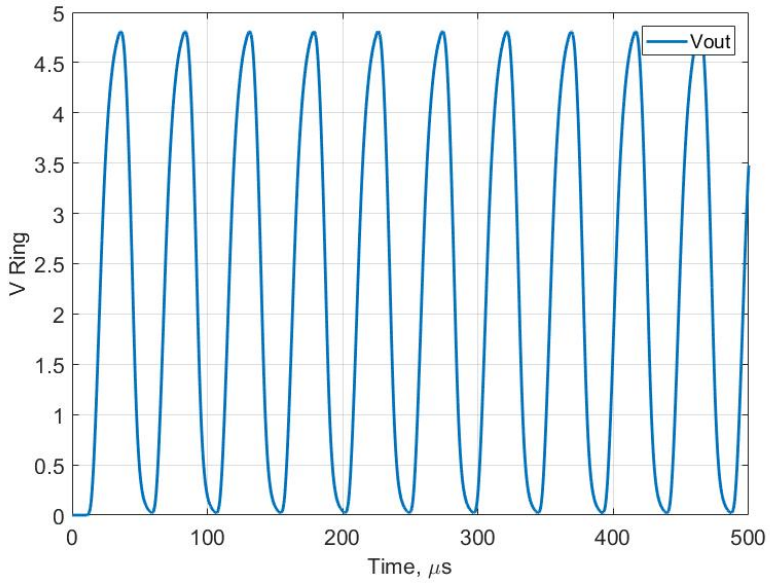

Figure 3: Simulated CMOS ring oscillator output

The ring oscillator circuit requires only a DC power source with a threshold voltage above what is required of the MOSFETS, and the oscillations will occur. To increase the frequency, the DC supply can be increased, causing an increase in current as well as frequency.

2.2 Signal Conditioner

2.3 Current Driver

The current driver for this lab was created using an MCP6004 op amp. The op amp is to act as the driver for the gate of a 2N3904 Bipolar Junction Transistor (BJT). The generic circuit for the current driver is shown in Figure 4.

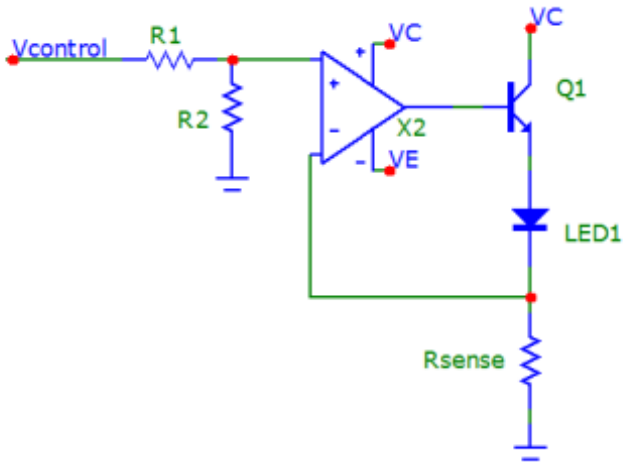

Figure 4: Generic current driver circuit [2]

The key to operation of the current driver is the BJT transistor. A BJT transistor, in contrast with the metal oxide semi-conducting field effect transistor (MOSFET), is capable of producing current by both types of Charge Carriers. This effectively allows the BJT to behave as a NPN or PNP transistor depending on the size of the input current. This also allows the BJT to use a smaller current signal to control a larger current.

The operation of a BJT is paramount for this lab. The MCP6004 is only capable of outputting around 20mA of current. The IR LED in use, however, has a forward current of 100mA [**?**]. A much larger current has to generated in order for the LED to operate.

The MCP6004 is used to set the node voltage for R_{sense}. The op amp is assumed to be ideal, so $V_- = V_+$. In order to ensure that the LED is forward biased, the node voltage should be less than the sum of the voltage drops from V_{supply} over the BJT and the diode. The lab briefing [2] states to set V_- less then 3V.

In order to attain a suitable voltage, a voltage divider is placed at the input to the op amp. The source voltage is the output from the signal conditioner, and was found to be 5V. In order to be less than 3V, a 50/50 voltage divider was used in order to create an input of 2.5V. With this voltage, and the maximum forward current of 200mA, the value for R_{sense} can solved using Ohm's Law. The final value for R_{sense} is 13Ω.

The simulated circuit for current driver is seen in Figure **??**.

The circuit required no changes from design to simulation. The current through the LED can be seen in Figure 5. The simulation was performed using a transient analysis integrated with Matlab.

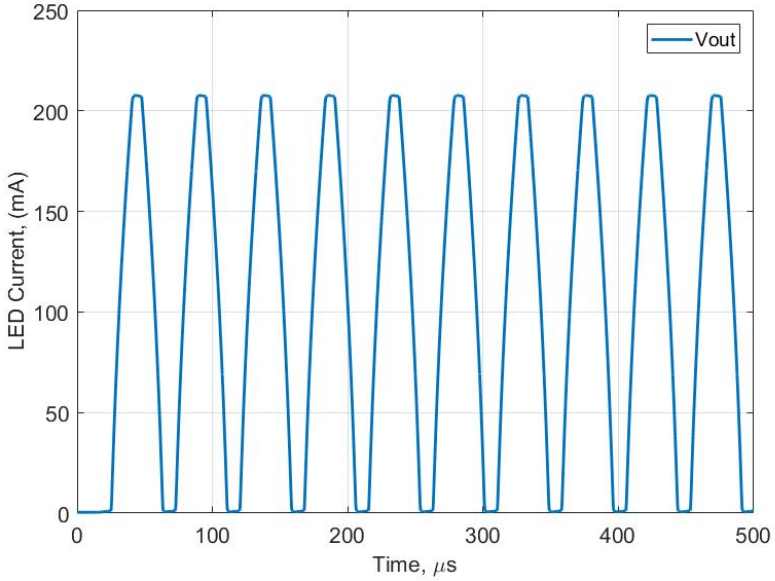

Figure 5: Simulated current through the LED

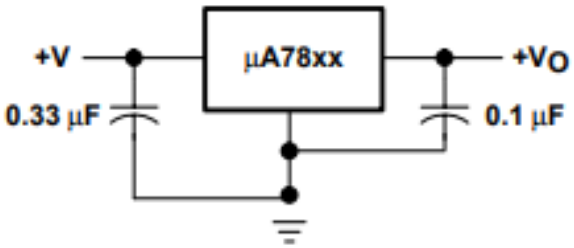

Figure 6: Configuration of voltage regulator[3]

The current through the LED matched the calculated value of 200mA. The LED is in an operational state.

2.4 Voltage Regulator

The Voltage regulator used was a LM7805. The voltage regulator is used because the CMOS ring oscillator and LED driver were designed to run on a source voltage of 5V. The power supply provided, however, is a 9V DC battery. The voltage, therefore, needs to be reduced. The voltage regulator operates by taking an input voltage and step it down to some lower voltage by shedding the difference in energy between the two potentials in the form of heat. Figure 6 shows the circuit configuration for the LM7805.

The equivalent circuit model for the LM7805 is shown. Notably, the circuit was not included in simulations and was constructed during the Implementation phase.

The final simulated circuit is shown in Figure 7. The summary of simulated results is shown in Table 1.

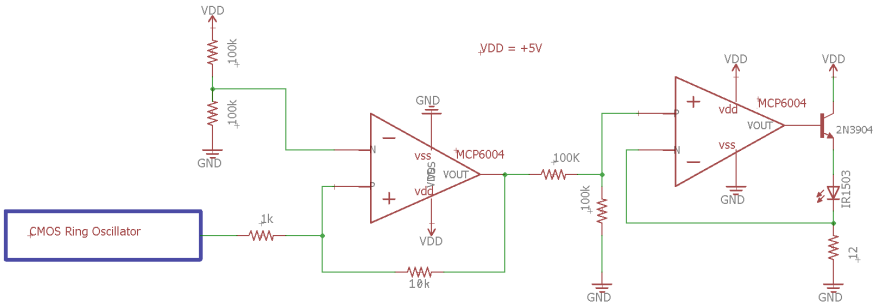

Figure 7: Simulated LED driver

Table 1: Simulated Results

Component	Simulated Values
Conditioned Voltage	5V
Conditioned Frequency	20kHz
Conditioned Duty-Cycle	48%
Output Current	200mA
R_{sense}	12Ω

The simulated circuit operated as expected and provided enough current in order to drive the LED.

3 Experimental Implementation

3.1 Ring Oscillator

3.2 Signal Conditioner

The signal conditioner required several small changes in order to be functional. The 100kΩ resistor voltage divider was switched to a 10kΩ potentiometer in order to facilitate easier adjustment of the output duty-cycle. The resistors in the feedback configuration were changed to 10kΩ and 100kΩ. This was done in order to minimize the loading effects between the signal conditioner and the current driver. The output waveform is shown in Fig 8.

The output waveform operated with a 4.5V peak, 20.26kHz and 45% duty-cycle.

3.3 Current Driver

Needs a donkey kicking

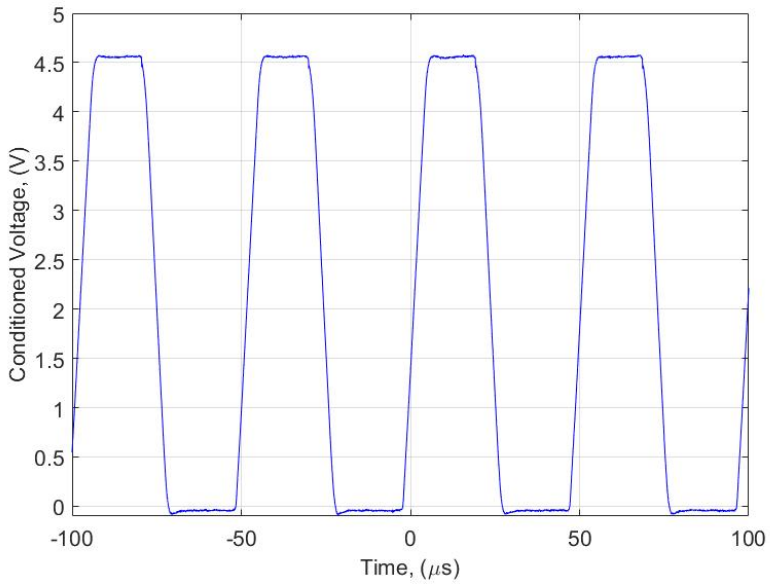

Figure 8: Voltage output of signal conditioner

4 Discussion

This lab served as introduction to MOSFETS and implementation of digital logic. When using transistors to create digital devices, it is often assumed that the device behaves ideally. When the device is logic high, it is one voltage, and when it is logic low it is another. Based on this logic, it is assumed that the switching on and off of the MOSFETS happen instantaneously. Based on the results of the ring oscillator and other inverter circuits, the MOSFETS do not switch instantaneously. Instead, power is consumed by the MOSFETS when they transition from one state to another. This consumption of power causes a small time delay. Each of the circuits described in this report are discussed in the following subsections, excluding the astable multivibrator. The astable multivibrator was not constructed during the experimental phase of this task.

4.1 NMOS inverter

The NMOS inverter worked as simulated and required no significant design changes in order to function. The measured power consumption was different from the simulated values, but it operated within a tighter band of values. The comparison of the NMOS with simulations is shown in Figure 2.

Table 2: Comparison of NMOS

Component Values	Simulated	Experimental
R	4.4kΩ	4.3kΩ
Max Power	31.2mW	5.8mW
Min Power	69.5pW	37μW
Rise Time	199ns	11μs
Fall Time	195ns	1.22μs

The rise and fall times were significantly greater as well. This can be accounted for by the fact the implemented circuit, in addition to board parasitic capacitance, also had capacitance from the jumpers connecting the pins of the device. Each jumper added capacitance to the circuit, which in turn increased the time constant for the circuit, which would account for the increased transition times.

4.2 CMOS inverter

The CMOS inverter required no changes from simulation. The circuit behaved as expected, with the VTC matching that of the simulations. One of the strengths of the CMOS is the faster transition between logic states. This is reflected in the slope of the experimental VTC. The CMOS also represents logic low with zero volts, as opposed to the NMOS were logic low was still some positive voltage. The DC power consumption of the CMOS was also negligible compared to that of the NMOS. Table 3 shows the differences between the simulated and measured CMOS circuit.

Table 3: CMOS inverter comparison

Component Values	Simulated	Experimental
Rise Time	142ns	235ns
Fall Time	114ns	177ns
Power	0	5μW

The experimental results for the CMOS inverter are shown in Table 3.

4.3 AND gate

The AND gate operated as expected. This lab served as an introduction to the use of transistors as logic devices. The use of binary logic is fundamental in the design of digital logic. The construction of a physical AND gate demonstrates the real device characteristics of logic circuits. The truth table for the constructed AND gate is shown in Table 4.

Table 4: Truth Table: AND

Inputs		Output
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

4.4 Ring oscillator

The ring oscillator circuit designed with the CMOS did not initially meet the specifications required in the lab. The simulations were accurate, but real-world parasitic capacitances from the board and jumper wires impacted the circuit. To remedy the situation, a capacitor of 4.7 nF was added in parallel after the second inverting gate. By increasing the capacitance, we lowered the frequency from 22.8 kHz to 19.8 kHz. The comparison between the simulated results and experimental is expressed in Table 5

Table 5: Comparison of ring oscillator results

Component Values	Simulated	Experimental
C_1	8nF	8.2nF
C_2	8nF	13.9nF
C_3	8nF	8.2nF
Frequency	20.1kHz	19.8kHz
Amplitude	5V	4.9V

The reason this oscillator is chosen over the astable multivibrator as the signal generator is mostly arbitrary and simply design choice for the optical uplink project [4]. Although one of the benefits of the ring oscillator is that from the sensitivity testing it is less affected by component tolerances than the astable multivibrator. This is significant since the capacitors available for circuit construction are 10% tolerances.

5 Conclusion

The design, simulation, and implementation of the ring oscillator signal generator have been explained. NMOS inverters, CMOS inverters, and logic gates were also investigated. Lab specification required that the signal generator have a frequency of approximately 20kHz, a duty-cycle of approximately 50%, and an amplitude of 5V. The signal generator takes an input DC voltage and creates an sinusoidal waveform at the output. The signal generator circuit was constructed using the following parts: three 8.2nF capacitors, a 4.7nF capacitor; and finally a CD4007 CMOS integrated circuit with 5V supply voltages. The frequency was 19.8kHz, with a duty-cycle of 51%, and an amplitude of 4.9V. An important lesson about the behavior real logic circuits was learned. Real digital circuits have measurable electrical characteristics and do not behave ideally.

References

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