Final Report

Optical Link

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Team 7

Abstract

The design, simulation and test of an infrared optical link transmitter and receiver is described. The optical link is required to transmit and recieve at a distance of at least 50 ft. The transmitter should send a signal of 20 kHz ±5%. The signal is required to have a duty-cycle of 50% ±5%. The LED driver current is required to be less than 200 mA. The final circuit transmitted 77 ft with a 20.1 kHz signal with a 50.1% duty-cycle. The LED driver current was 150 mA. The transmitter consumed 540 mW of power. The receiver consumed. 14.4 mW of power. Figure 1 below is the block diagram of the optical link project.

Figure 1: Optical link block diagram [1]

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December 11, 2017

1 Introduction

Table 1 shows the device specifications and measured performance of the Optical Link project.

Table 1: Performance summary of optical link project

Parameter	**Specified Value**	**Measured Value**	
Transmission distance (in feet)	> 50'	77'	
Signal Frequency	20 kHz ± 5%	20.1 kHz	App
Duty cycle of signal	50% ± 5%	50.1 %	App
LED Peak drive current	<200mA	150 mA	App
Transmitter Power Consumption	-	540 mW	
Receiver Power Consumption	-	14.4 mW	
Frequency sensitivity to capacitor tolerance in ring oscillator (simulation)	-	-	App

Table 2 shows the comparison from simulated values and those measured in the final device.

Table 2: Simulated and measured comparison]

Parameter	**Specified Value**	**Measured Value**	**Simulated Value**
Signal Frequency	20 kHz ± 5%	20.1 kHz	20 kHz
Duty cycle of signal	50% ± 5%	50.1 %	48 %
LED Peak drive current	<200mA	150 mA	200 mA

The circuit operated as expected and within specifications. A rather large modification that was required was the removal of the final voltage amplifier, Task 5. This circuit ended up introducing far too much noise into the final design and resulted in more harmonic distortion. The final circuit met specification without the addition of the voltage amplifier. The final circuit did not need the 200 mA simulated. This is because the real IR LED should be driven with less than 200 mA of current. The circuit was simulated with 200 mA as a way of ensuring, upon circuit implementation, that the LED had enough current to operate.

References

[1] N.W. Emanatoglu "Lab #1; photodetector and transimpedence amplifier," University of Maine, Orono, ME, 2017.

Appendices

A Transimpedence Amplifier

Optical Uplink

Transimpedence Amplifier Module

Ryan Dufour
Phil Robb

Abstract

The design, simulation, and construction of a transimpendence amplifier are described. An LF356 operational amplifier, with rail voltages of ±12V was used to convert the current output supplied by an OP999 photo-diode to a measurable voltage. An infrared LED was driven with a 20kHz, 5V square wave in order to generate the input for the photodiode. An output voltage of $8V_{pp}$ was generated. The Amplifier operated with a 3dB cuttoff frequency of 41kHz.

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1 Introduction

This report describes the design, implementation and test of a transimpedance amplifier(TZA). The TZA consists of an inverting operational amplifier and a feedback resistor. The TZA takes an input current and converts it to an output voltage. The TZA allows for a very high gain. The circuit uses a photodiode to generate an input current. A compensation capacitor was used in order to ensure that the TZA remained stable. Figure 1 belows demonstrates where in the optical link relay design the TZA falls.

Figure 1: Block diagram for optical uplink[1]

Section 2 of this report describes the design of the TZA as well as the rationale behind LED choice. Simulations are discussed in section 3 and experimental results are in section 4. A discussion of the results, sources of error, and areas of possible improvement are outlined in section 5. Section 6 concludes this report.

2 Circuit development

This section covers the design choices associated with the TZA and LED module. In order to choose an appropriate LED the LED datasheets were used. The operational amplifier was provided for the lab as was compensation capacitor[1]. Figure 2 is the schematic of the TZA as well as the LED.

The LED circuit in Figure 2 will not be included in the optical uplink design. The LED circuit in this lab was designed for testing purposes only. The resistor is chosen to be a sufficient value as to not exceed the breakdown current of the diode.

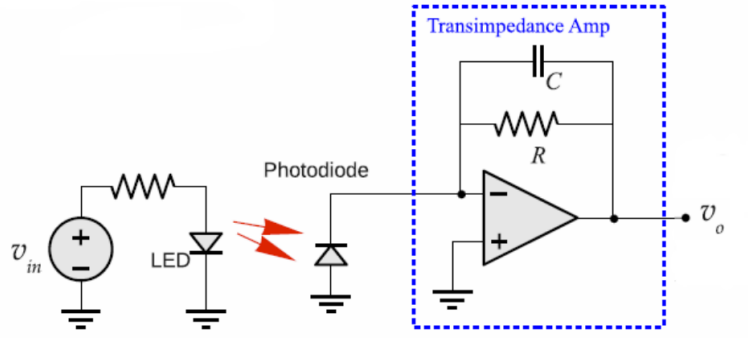


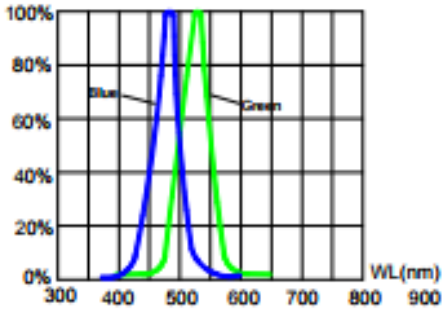
Figure 2: Basic Circuit Schematic for Design[2]

Section 2.1 describes how the LED was chosen. Section 2.2 describes the design of the TZA.

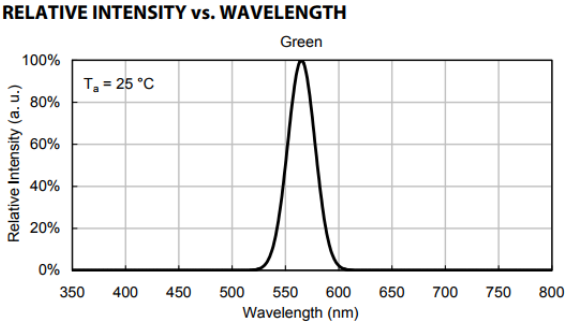
2.1 Choosing an LED

The LED is an integral part of the circuit design. In order for current to be emitted from the reverse-biased photodiode a incident light source is required. The photodiode used in this lab is a reverse-biased PIN silicon photodiode, the OP999. When an incident light of the proper wavelength and strength is used to activate the OP999, there is a transfer of energy from the photons from the light to the atoms inside the OP999.

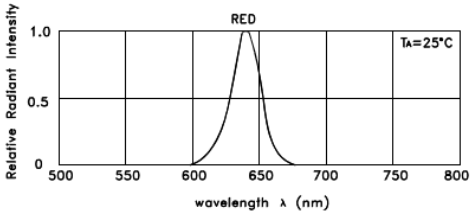
The electrons freed during this reaction will induce a reverse current from the OP999. There is also another current that is present at all times called dark current. This is a leaking current produced by photodiodes from the natural light. The current is small, but causes undesired affects on the circuit in the form of noise. Since the OP999 photodiode is reverse-biased, the dark current is increased. However, the noise for the purpose of this lab created by the dark current is negligible.



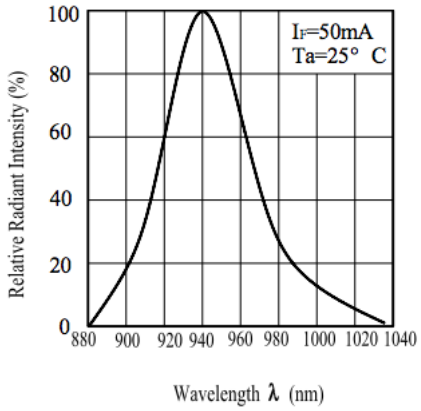
(a) Blue LED intensity v. wavelength [3]



(b) Green LED intensity v. wavelength [4]



(c) Red LED intensity v. wavelength [6]



(d) Infrared LED intensity v. wavelength [7]

Figure 3: Intensity graphs for LED's

The OP999 photodiode requires that for a maximum current output, a wavelength of 935nm needs to be emitted from the light source[5]. The light source will be chosen from among four light emitting diodes(LED) seen in Figure 3. Figure 4 below gives the spectral response of the OP999 photodiode.

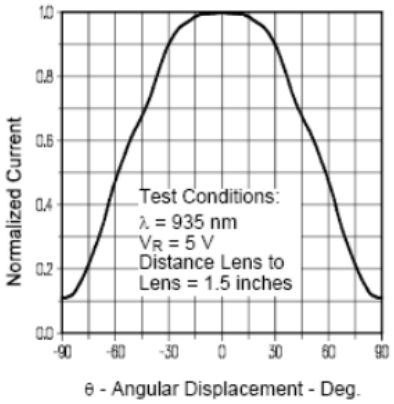


Figure 4: Spectral response of OP999[5]

The blue, bright green and red LED's ranged from 465nm to 640nm. These outputs would not have worked as a wavelength of 700nm will achieve only 20% of the photodiode's max current output. The Infrared LED, IR1503, has a wavelength of 940nm, which incidentally is what is required for the photodiode to achieve 95% or more of it's max current output. Table 1 below shows the values for maximum intensity for each LED.

Table 1: Maximum intensity wavelengths

Type of LED	Blue LED C503B-BCS/BCN-030	Green LED WP7113SGC	Red LED WP7113SEC/J3	Infrared LED OP999
Max Intensity Wavelength (nm)	465	565	625	940

2.2 Design of transimpedance amplifier

The schematic of the TZA is shown in Figure 5. The choice of TZA is that it provides large gain while still maintaining a large frequency bandwidth.

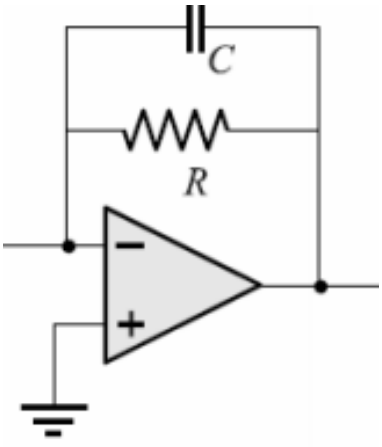


Figure 5: Transimpedence amplifier [2]

The frequency limit of the TZA is described by Equation 1.

$$f_{limit} = \sqrt{\frac{GBW}{2\pi RC_{pd}}} \tag{1}$$

GBW is the gain product, R is the feedback resistance and C_{pd} is the parasitic capacitance of the photodiode. The closed loop gain of the TZA is described by Equation 2.

$$Gain = \frac{v_0}{i_i} \tag{2}$$

Where v_0 is the output voltage and i_i is the input current. By performing Kirchoff's Current Law(KCL) at the noninverting input of the op-amp, the gain can be found to be Equation 3.

$$Gain = R_f \tag{3}$$

R_f is the feedback resistance of the TZA. The gain of the TZA can be made as large as the feedback resistance. This, however, will likely lead to the amplifier becoming unstable. Therefore, a compensation capacitor should be used to ensure stability. The 3dB cutoff, as provided by the lab manual states that $f_{3dB} \geq 2f_0$. From this, the 3dB cutoff can be found via Equation 4

$$f_{3dB} = \frac{1}{2\pi R_f C} \tag{4}$$

Using the 22pF provided by the briefing[1], a feedback resistance of 180kΩ can be found. Using these components a cut off frequency of 39.8kHz is acheived.

3 Simulations

This section describes the simulation of the TZA using NGSpice intregrated with Matlab.The output voltage and frequency response were simulated using these two prgrams. The OP999 photodiode was simulated by converting it to an equivalent circuit, seen in Figure 6.

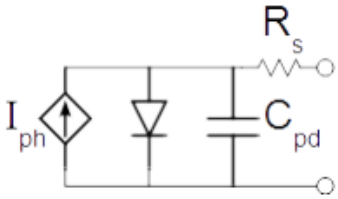


Figure 6: Equivalent ciruit of photodiode[2]

The final circuit that was simulated is shown in Figure 7.

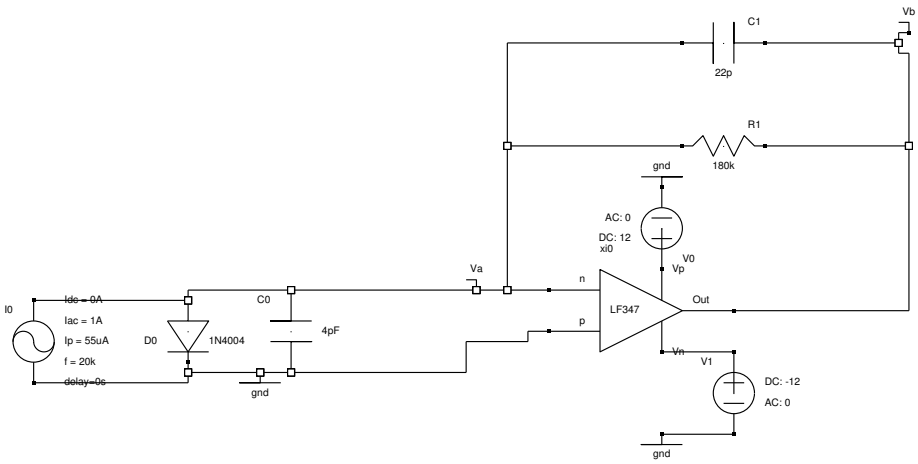


Figure 7: Equivalent ciruit of photodiode[2]

First the output voltage was simulated, and then finally the frequency response.

3.1 Output voltage

The output voltage was simulated using a transient analysis in NGSpice. Figure 8 below shows the unsaturated output voltage of the TZA. If the TZA were to operate while saturated it would produce distortion and the output would no longer behave linearly.

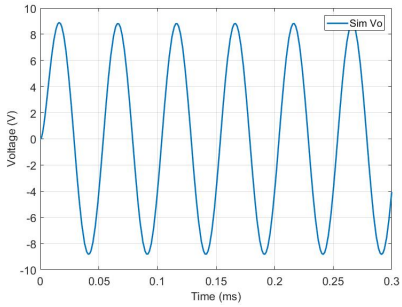


Figure 8: Simulated transient analysis of TZA output voltage

Notably, this is the op amp operating at the maximum input current prior to saturation. This provides

the highest operating condition at which the circuit still behaves linearly. The other circuit parameter of interest was the frequency response.

3.2 TZA frequency response

The TZA gain was measured doing an AC analysis in NGSpice. The 3dB cutoff should be greater than 40kHz. The pole frequency should be greater than 40kHz in order to ensure that TZA remains stable and does not turn into a oscillator.The simulated frequency response is found below in Figure 9.

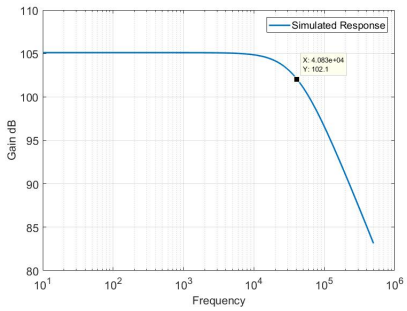


Figure 9: Simulated AC analysis of TZA Gain

The 3dB bend was found to be at a little greater than 40kHz. This ensures that the op amp remains stable under operating conditions.

4 Experimental implementation

The experimental design required only one change. The LF347 op amp was switched to an LF356 op amp. The LF347 operated with much higher noise than the LF356. Further information is found in the Discussion section. The following results were found using the simulated values and with the distance from LED to diode being several centimeters apart. The final circuit is shown in Figure 10 below.

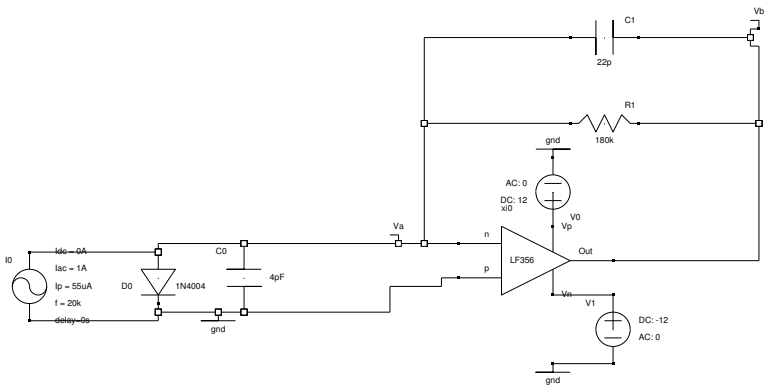


Figure 10: Experimental circuit schematic

First the output voltage was measured and then finally the frequency response was measured.

4.1 Output Voltage

The measured voltage output is found below in Figure 11.

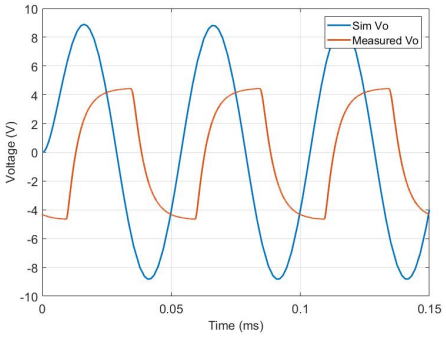


Figure 11: Voltage output of TZA: sim and experimental

The output signal was well within range and did not saturate the op amp. A notable discrepency is that the measured signal is not a perfect sinusoid. Finally, the frequency response was measured.

4.2 Frequency Response

The measured frequency response is found below in Figure 12. The actual gain of the circuit could not be measured, but a frequency sweep could be done using the Digilent Discovery 2's network analyzer.

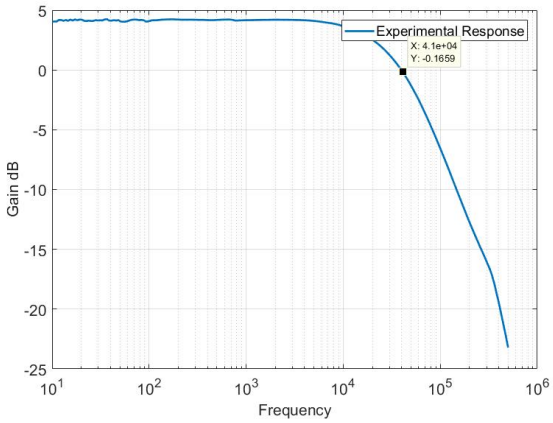


Figure 12: Experimental AC Analysis: Gain v. Frequency

The 3dB frequency was greater than the required 40kHz. Notably, the network analyzer could only generate data reliably upto 500kHz, unlike simulations which were performed up to 10MHz.

5 Discussion

Based on the development and design of the transimpedance amplifier, the actual results were similar, but with some variations. The voltage output of the simulated transimpedance amplifier was approximately $18V_{pp}$. The measured value of the voltage output of the practical amplifier fell well short of that at approximately $8V_{pp}$ This is due to the current being provided by the current source in the simulation was the max allowable current before saturation and the photodiode's output current is well below that limit. The other noticeable difference is the shape of the outputs when compared. The simulated output is a smooth sinusoid which doesn't display the normal behavior of capacitors. The experimental output has discontinuities due to the exponential charging of the capacitor in the feedback of the TZA.

It also must be assumed that real-world factors had a parasitic effect on the circuit as well. The photodiode must be positioned properly with the LED, and even then, there will be some loss unless more of the photons are redirected towards the photodiode.

Finally, an LF356 op amp was chosen over the LF347 because the LF356 produced an output signal with far less noise. The LF356 benefits from having fewer onboard op amps, reducing interference at the output.

6 Conclusion

The design, simulation, and implementation of the transimpendence amplifier have been explained. Lab specification required that the TZA have an 3dB cutoff frequency of at least 40kHz. The TZA takes a very small input current and then outputs a measurable voltage signal. The TZA circuit was constructed using the following parts: a OP999 photodiode, a 22pF capacitor, a 180kΩ resistor, and finally an LF356 operational amplifier with $\pm$12V rail voltages. An IR LED was used, with a series 50Ω resistor, as the light source that was driven with a 5V, 20kHz square wave. The output voltage was $8V_{pp}$ with a cutoff frequency of 41kHz. An important lesson about the behavior of non-ideal op amps was displayed with the inclusion of the capacitor to keep the op amp stable.

A References

[1] N.W. Emanatoglu "Lab #1; photodetector and transimpedence amplifier," University of Maine, Orono, ME, 2017.

[2] D.E. Kotecki "Lab #1," University of Maine, Orono, ME, 2017.

[3] Cree 5-mm Blue and Green LED. Cree, 2017.

[4] WP7113SGC. Kingbright, 2017, p. 3.

[5] "PIN Silicon Photodiode", 2017. [Online]. Available: http://web.eece.maine.edu/ kotecki/ECE342/datasheets/OP993-999_0.pdf. [Accessed: 24- Sep- 2017].

[6] WP7113SEC/J3. Kingbright, 2017, p. 3.

[7] IR1503. EVERLIGHT, 2017, p. 4.

B Multifeedback Bandpass Filter

Optical Uplink

Multiple Feedback Bandpass Filter Module

Ryan Dufour
Phil Robb

Abstract

The design, simulation, and construction of a multiple feedback bandpass filter are described. An LF347 wide bandwidth quad JFET input operational amplifier integrated circuit, MFBP filter, with rail voltages of ±12V, was used to amplify the output signal from a transimpedance amplifier. This is used as a module for an optical uplink circuit. The filter is required to have a center frequency of 20kHz, a 3dB bandwidth between 1.5kHz and 5kHz, a gain of greater than 60dB, and rail supplies of ±12V. A sinusoidal waveform with an amplitude of 100mV and frequency of 20kHz was used for the input to the MFBP filter. The output voltage operated with a gain of 71.4dB, with a bandwidth at 3dB of 2.11kHz and a center frequency of 20.2kHz.

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1 Introduction

This report describes the design, implementation and test of an active multifeedback bandpass (MFBP) filter. The MFBP filter consists of a wide bandwidth quad JFET input operational amplifier integrated circuit with negative and positive rail voltages, and a voltage divider at the input. The MFBP filter takes a small input and converts it to a greater output voltage. This circuit uses a sinusoidal input waveform generated by the Digilent Analog Discovery 2 (DAD2) which is fed into the voltage divider at the input of the circuit. A unity gain buffer is located at the output of the MFBP filter to lower the impedance generated by the operational amplifier IC. Figure 1 below demonstrates where in the optical link relay design the MFBP filter falls.

Figure 1: Block diagram for optical uplink[1]

The output from the previous module, the photodetector TZA seen in 1, will be in the μV range, which is too small for the purposes of the optical link project. The noise output from the TZA also needs to be filtered by using an active bandpass filter, similar to the one in Figure 2.

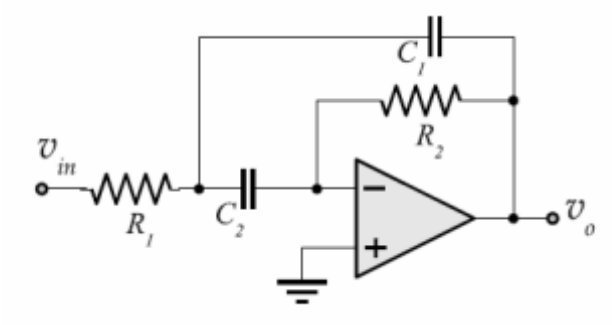

Figure 2: General schematic of the MFBP[1]

Figure 2 is the generic schematic for a multiple feedback bandpass filter. By passing the signal through this active bandpass filter, the noise is reduced and the signal will be amplified.

Section 2 of this report describes the design of the MFBP filter. Simulations are discussed in section 3 and experimental results are in section 4. A discussion of the results, sources of error, and areas of possible improvement are outlined in section 5. Section 6 concludes this report.

2 Circuit Development

This section covers the design choices associated with the MFBP filter module. The LF347 quad operational amplifier was provided for this lab with the intention of providing options regarding the amount of

of cascading operational amplifiers that would be used to reach the desired specifications. Figure 3 is the schematic design of the MFBP filter for this lab.

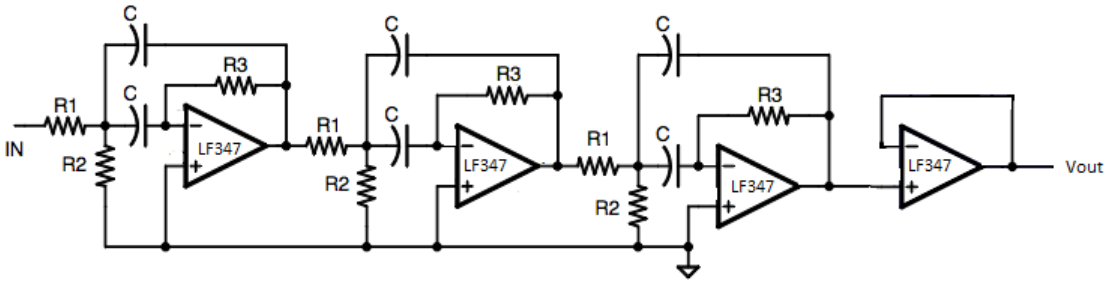

Figure 3: Basic schematic for three stage MFBP filter with unity gain buffer

In Figure 3, a three stage MFBP filter is shown. Each successful stage has will have a gain that is approximately 100 times smaller than the gain specification for this lab of 1000 $\frac{V}{V}$. By doing this, we will not need a single MFBP filter with high gain and a high quality factor. After each stage, the gain is increased and the 3dB bandwidth decreases.

The choice of using three stages for the MFBP filter is due to the lab requirement that the bandwidth between 1.5 kHz and 5 kHz. The gain and quality factor can not be set independently[2] By using three cascading LF347 operational amplifiers, the bandwidth can be kept narrow by setting the gain of an individual op amp to be relatively small. Instead of attempting to have the full gain with a single stage, which would result in a wide bandwidth, the op amps are cascaded together. This relation can be seen with Equation 1[2],

$$Q = \frac{f_c}{\Delta f} \tag{1}$$

where f_c is the center frequency and Δf is the bandwidth. This method allows sufficient gain while still maintaining a narrow bandwidth.

There are considerations that need to be taken in regarding the range of values that are usable for the capacitors. For the purposes and design of this three stage MFBP filter, the capacitor values need to be less than 1nF because the effect on the value of the resistors would be minimal and unrealistic to use in this circuit. The other reasoning is the capacitors need to be large enough to filter the noise, as this is an active bandpass filter.

There are two approached to consider for choosing component values with regard to the capacitors and resistors. The first approach is to initially choose realistic capacitor values, each being equivalent to each other. The second approach is to choose a value for the resistor value for R_1, then derive the remaining components.

In choosing the values for each of these components, the output specifications of the active filter must be used. These can be seen in Table 1.

Table 1: MFBP filter specifications

Filter Topology	MFBP Filter Specification Requirements
Center Frequency (f_c)	20 kHz
$3dB$ Bandwidth	Between 1.5 kHz and 5 kHz
Gain	Greater than 1000 $\frac{V}{V}$
Rail Supplies	$\pm$ 12 V

Table 1 summarizes the specifications of the lab. The approach chosen for the purpose of this lab is the first, to choose capacitor values to derive the values of the resistors needed to match specifications. The values of C_1 and C_2 were chosen to be 470pF as they are in the middle of the desired range of values and readily available. Larger capacitor values result in smaller resistor values. In order to minimize the loading effects on the stages of the MFBP, the input resistance should be kept greater than 1kΩ.

In order to determine the values, the transfer function is needed to derive the equations needed for each component base on the chosen capacitor, quality, gain and center frequency values. The transfer function for the MFBP filter is shown in Equation 2

$$H(s) = \frac{\frac{-1}{R_1 R_2 C_1 C_2}}{s^2 + s\frac{1}{C_1}(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}) + \frac{1}{R_2 R_3 C_1 C_2}} \tag{2}$$

The values of the capacitors were chosen to be 470pF. The quality factor needs to have a realistic value as well. The higher the Q, the narrower the bandwidth. The desired bandwidth range at 3_{dB} is between 1.5kHz and 5kHz. The quality factor will initially be chosen at 5. the value of the quality factor, Q, reflects the ratio of the center-frequency to the 3dB bandwidth.

The center frequency, f_o has already been determined to be 20 kHz. Based on the required specifications of the active filter, a gain of more than $1000\frac{V}{V}$ is needed, so G must be more than 10. Real world factors will affect the circuit so the the gain was set to 12 to account for losses during experimentation. The capacitor values C_1 and C_2 were chosen to be 470pF. Equation 3 will be used to calculate the needed values for the first resistor, R_1.

$$R_1 = \frac{Q}{G * 2\pi f_o C_1} \tag{3}$$

Equation 3 demonstrates the solution for R_1. R_2 can be found by Equation 4,

$$R_2 = \frac{Q}{(2 * Q^2 - G)2\pi f_o C_1} \tag{4}$$

where, notably, the Q factor begins to dominate the denominator in Equation 4. R_3 can be found by Equation 5.

$$R_3 = \frac{Q}{\pi f_o C} \tag{5}$$

Equation 5, is no longer dependent on gain or Q in the denominator. Based on the relationships between the components of this active filter, the center frequency, in Equation 6, can be found.

$$f_o = \frac{1}{2\pi C}\sqrt{\frac{R_1 + R_2}{R_1 R_2 R_3}} \tag{6}$$

The role resistors play in changing center frequency can be seen with Equation 6. The gain can be found similarly in Equation 7.

$$G = \frac{1}{2\frac{R_1}{R_3}} \tag{7}$$

The gain, from Equation 7, can be seen to depend only on R_1 and R_3. All values that were calculated based on the specifications can be seen in Table 2.

Table 2: Calculated

Component	Value
R_1	7kΩ
R_2	2.2kΩ
R_3	170kΩ
$C_1 = C_2$	470pF
V_{CC}	12V
V_{EE}	-12V

Table 2 demonstrates that the calculated values fall within the lab specifications. Based on these calculations, simulations will be conducted in Section 3.

3 Simulations

This section describes the simulation of the MFBP using NGSpice integrated with Matlab.The frequency response, including center frequency, bandwidth, and gain were simulated.

The final circuit that was simulated is shown in Figure 4.

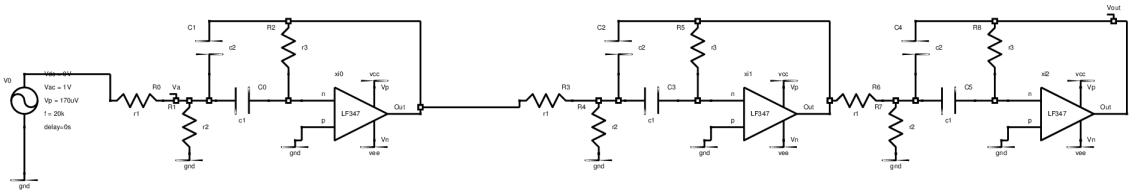

Figure 4: Simulated circuit of MFBP

Figure 4 uses the same design structure as Figure 2 seen in Section 2. All of the simulated circuit values are summarized in Table 3.

Table 3: Simulated values

Component	Value
R_1	7kΩ
R_2	2.2kΩ
R_3	170kΩ
$C_1 = C_2$	470pF
V_{CC}	12V
V_{EE}	-12V

Table 3 was simulated using the same values that were calculated in Section 2. These simulations were close to the required specifications.

The frequency response was simulated using an AC sweep in NGSpice. Figure 5 below shows the frequency response. The simulation was performed from 100Hz to 1MHz.

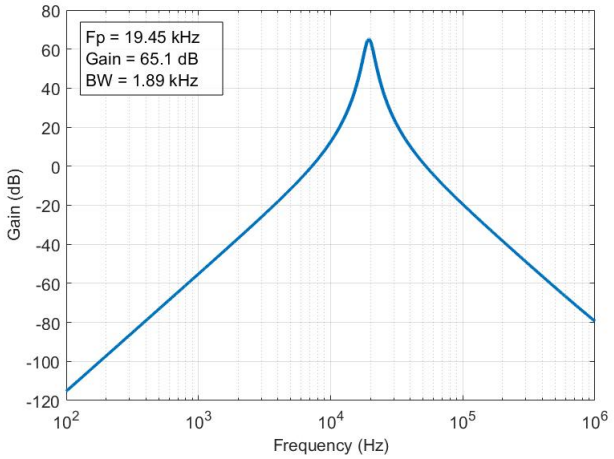

Figure 5: Simulated AC analysis of MFBP

The center frequency in Figure 5 was found to be a little less than the required 20kHz. However, upon taking into account the frequency bandwidth, the MFBP is within specifications. The resistors available for design have a ±5% tolerance about their nominal value. The available capacitor values have a±10% value about their nominal value. The effect of these tolerances on the performance is summarized in Figure 6. The simulation was performed in 10 iterations using Matlab random number generator to choose values that fell within the respective component tolerances[3].

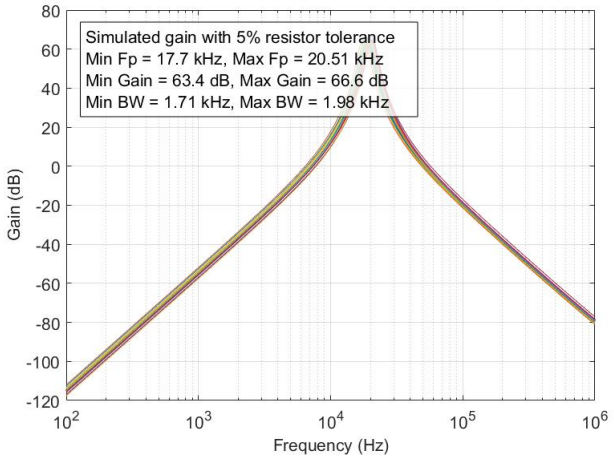

Figure 6: Two-sigma variation

As Figure 6 the tolerances could lower the center frequency quite significantly. Care should be taken when constructing the circuit to choose components that fall close to their nominal values. Table 4 summarizes the simulated results of the circuit.

Table 4: Simulated results

Value	Simulated
Center Frequency	19.45 kHz
Gain	65.1 dB
Bandwidth	1.89 kHz

The simulated results in Table 4 fell within an acceptable margin of error for this simulation.

4 Experimental Implementation

The LF347 is a model featuring four on board op amps. Only three were required by the final design, the fourth was instead used as a unity gain buffer one the output. The final circuit is shown in Figure 7 below.

Figure 7: Experimental circuit schematic

The experimental design required several changes, as seen in Figure 7, compared to the simulated model. Notably, the simulated design failed to meet the 60dB specification with a peak gain of 54dB. The MFBP was subsequently redesigned due to failing to meet the specified values in a real world scenario. The final component values are summarized in Table 5.

Table 5: Experimental values

Component	Value
R_1	2.7kΩ
R_2	4.3kΩ
R_3	160kΩ
$C_1 = C_2$	470pF
V_{CC}	12V
V_{EE}	-12V

The final values that are expressed in Table 5 are different than the simulated due to real world parasitic capacitance and limitations of the breadboard at higher frequencies. The experimental results are as follows: the output voltage, which did not saturate; the frequency response, with a center frequency of 20.2kHz; and the bench test, where the specifications were met.

4.1 Output Voltage

The measured voltage output is found below in Figure 8. The time domain signal was measured using the Digilent Discovery and Waveforms software. The time domain was measured on a 50μs/div scale with a voltage range of 2V/div.

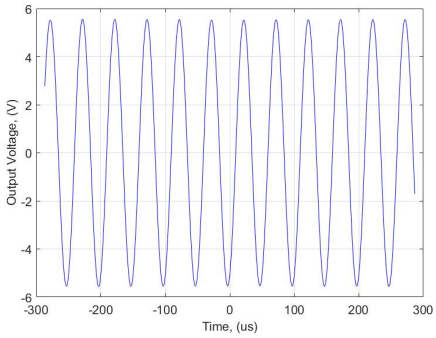

Figure 8: Voltage output of MFBP

The output signal, as seen in Figure 8, did not saturate the op amp and had no discernible noise. Notably, the signal was still well within rail voltages so the risk of saturation is small. Finally, the frequency response was measured.

4.2 Frequency Response

The measured frequency response is found below in Figure 9. A frequency sweep was done using the Digilent Discovery 2's network analyzer. The frequency sweep was performed from 1kHz to 500kHz. The wave generator was attached to the input of the voltage divider. The channel one scope was used as a reference channel and was tied to the input of the circuit. Channel 2 was used to measured the output of the MFBP filter.

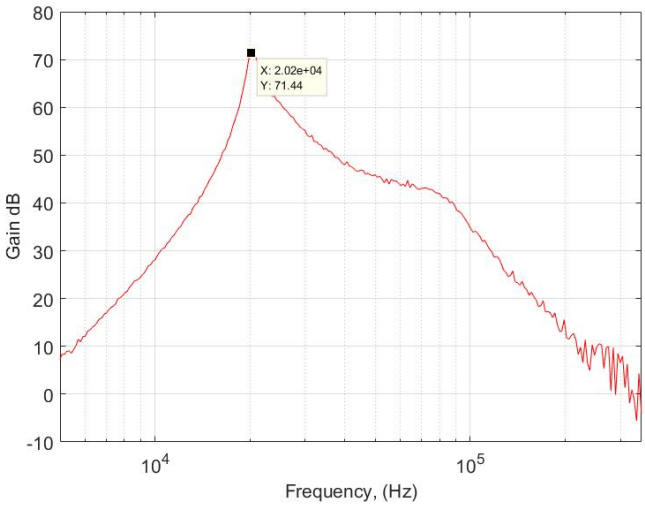

Figure 9: Experimental AC analysis

As seen in Figure 9, the center frequency was found to be 20.2 kHz with a gain of 71.4 dB. Notably there was another pole located at 70kHz; this is addressed in the Discussion section. The bandwidth is shown in Figure 10.

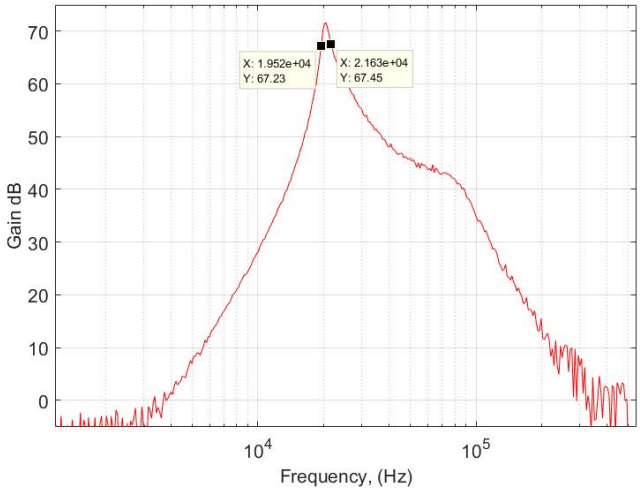

Figure 10: Experimental bandwidth

The bandwidth was found to be, in Figure 10, 2.11kHz, which is within the specifications of the lab.

4.3 Bench Test

The final circuit operated mostly as expected under testing conditions. The DC output while the input tied to ground was found to be 5mV. While greater than ±2mV outlined, it was still within allowable tolerances. The AC output was found to be ±50mV, which falls within the allowable range of around 0V.. The circuit also returned to the ±50mV noise upon the removal of an input waveform. The professor, Dr. Kotecki, noted that the differences between the results and that of the benchmark were minor and fell within allowable ranges.

The final experimental results are summarized in Table 6.

Table 6: Experimental results

Value	Experimental
Center Frequency	20.2 kHz
Gain	71.4 dB
Bandwidth	2.11 kHz

As seen in Table 6, the experimental results fall within the lab specifications outlined.

5 Discussion

The simulated circuit failed to meet lab specifications after construction. This can be accounted for by analysis of Figure 6. The simulated values were not available in the parts store and had to be created using several resistors in series. With each additional resistor the chance of tolerances affecting the circuit

increases. Component tolerances can quite significantly change the center frequency. This would explain why the built circuit failed to meet specifications. If the center frequency was on the low on end of 17kHz, then the input 20kHz signal would not see the max gain, and thus fail to meet specifications. The Table 7 outlines the specifications for this lab.

Table 7: MFBP filter specifications

Filter Topology	MFBP Filter Specification Requirements
Center Frequency (f_c)	20 kHz
$3dB$ Bandwidth	Between 1.5 kHz and 5 kHz
Gain	Greater than 1000 $\frac{V}{V}$
Rail Supplies	$\pm$ 12 V

Table 7 summarizes the specifications that were required by this lab. Another consideration for this design was the role center frequency and gain played. If the gain of the circuit was designed to be too high (¿100dB) then upon applying rail voltages the op amp would be pushed into oscillation. The circuit would also be pushed into saturation. The op amps would then no longer be operating in their linear regions and the circuit would essentially be behaving as an multivibrator. This is a key difference between ideal and non ideal op amps. From mathematical background, it would make sense to try and design the filter to generate as high a gain as possible. The real circuit, however, is in fact bound by rail and feedback limitations. Attempting to build this circuit with too high of a gain will result in a nonfunctional circuit. Table 8 summarizes the simulated and experimental results of this report.

Table 8: Results summary

Values	Simulated	Experimental
R_1	7kΩ	2.7kΩ
R_2	2.2kΩ	4.3kΩ
R_3	170kΩ	160kΩ
C	470pF	470pF
Gain	65.1dB	71.4dB
Center Frequency	19.45kHz	20.2kHz
Bandwidth	1.89kHz	2.11kHz

Table 8 provides an overview of the major results from this lab.

The circuit was then redesigned using parts that were readily available in the parts store. the gain was also increased to ensure that the 60dB threshold was reached. The final circuit performed within lab specifications. The final circuit did, however, "fail" some of the bench tests. Notably the DC noise was 5mV, which is greater than that stated on the bench test. This, however, was said to be still to be in an allowable range by the Professor. The AC noise was $\pm$50mV, which was said to be within the allowable range. To help eliminate some of the noise bypass capacitors were added to the positive and negative rail voltages. A parallel plate capacitor was added in parallel with a electrolytic capacitor. The parallel plate capacitor filters our high frequency noise, while the electrolytic filters out low frequency noise.

Section 6 that follows concludes this report.

6 Conclusion

The design, simulation, and implementation of the multi-feedback bandpass filter have been explained. Lab specification required that the MFBP have a center frequency of approximately 20kHz, a bandwidth of between 1.5k and 5kHz, and a gain of at least 60dB. The MFBP takes an input voltage and filters out frequency outside of the bandwidth around the center frequency as well as generates a gain. The MFBP circuit was constructed using the following parts: a 2.7kΩ, a 4.3kΩ, and a 160kΩ resistors; a 470pF capacitor; and finally an LF347 operational amplifier with ±12V rail voltages. An 100:1 voltage divider was used at the output of the wave generator in order to create an appropriately small input to the MFBP filter. The gain was 71.4 dB, with a bandwidth of 2.11kHz centered at 20.2kHz. An important lesson about the behavior of non-ideal op amps was displayed by the tendency of an op amp to be pushed into oscillation when the gain is set too high.

References

[1] D.E. Kotecki Lab.(2017) Lab #2 Active Bandpass Filters [Online]. Available: http://web.eece.maine.edu/ kotecki/ECE342/labs/ECE342_2017_Lab2.pdf

[2] N.W. Emanatoglu.(2017) Lab #1; photodetector and transimpedence amplifier [Online]. Available: http://web.eece.maine.edu/ kotecki/ECE342/labs/ECE342_2017_Lab2.pdf

[3] N.W. Emanatoglu.(2017) Lab #1; photodetector and transimpedence amplifier [Online]. Available: http://web.eece.maine.edu/ kotecki/ECE342/labs/ECE342_2017_Lab2_MFBF.pdf

C MOSFET Based Logic Gates and Digital Oscillator

Task 3: MOSFET Based Logic Gates and Digital Oscillator

Optical Uplink

Ryan Dufour
Phil Robb

Abstract

The design, simulation, and construction of a signal generator using MOSFET based logic gates are described. In task 3 of the optical uplink project, several inverting circuits are explored using NMOS and CMOS MOSFETS. An inverter based ring oscillator was simulated and constructed using the CD4007 CMOS integrated circuit. Simulations were also conducted using various configurations of NMOS and PMOS inverters, which are described in this report. The ring oscillator was chosen to be the signal generator for the optical uplink project. The required output of the CMOS ring oscillator for the use in the optical uplink project are a frequency of 20kHz, a 50% duty-cycle, and a $5V_{pp}$ amplitude. The final design featured a sinusoidal wave form, at a frequency of 19.8kHz, a duty cycle of 51% and $4.9V_{pp}$ amplitude. .

Electrical and Computer Engineering
University of Maine
ECE - 342
December 11, 2017

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1 Introduction

This report describes the design, implementation and test of a signal generator using various NMOS and CMOS inverter designs. Two different signal generators were designed, an astable multivibrator and a ring oscillator. Notably, negative metal oxide semiconducting field effect transistors (NMOS), complementary metal oxide semiconducting field effect transistors (CMOS), and finally the conjunction of the two to form an AND logic gate. Figure 1 demonstrates where in the optical uplink project the signal generator is placed. The signal generator creates the waveform that drives the LED that is detected by the photodetector.

Figure 1: Block diagram for optical uplink [1]

The output from the the signal generator is not a square wave, nor does it output enough current to drive the LED. The current driver will be created in a subsequent lab. The voltage transfer characteristics (VTC) of an ideal inverter is shown in Figure 2.

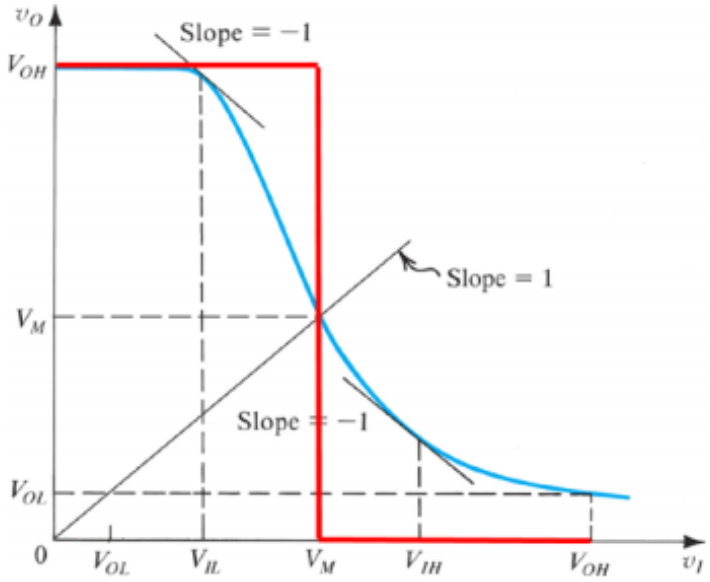

Figure 2: Ideal VTC of inverters [1]

Figure 2 describes the ideal VTC of an inverter, where the voltages for logic low and logic high are shown. Both the ring oscillator and the astable multivibrator are created by cascading several CMOS inverters together,

Section 2 of this report describes the design, and when relevant, the simulations of the NMOS, CMOS inverter, the AND gate, the ring oscillator, and finally the astable multivibrator. Experimental results are addressed in section 3. A discussion of the results, sources of error, and areas of possible improvement are outlined in section 4. Section 5 concludes this report.

2 Circuit Development

This section covers the design choices associated with the various circuits constructed. A common trait among all of the designs included is the use of MOSFETS. MOSFETS are silicon based components that take advantage of the semiconducting properties of silicon in order to behave as a switch. The ability for a MOSFET to transition from "open" to "closed" is the foundation for digital circuits. In digital circuits, voltages are not represented as analog continuous signals, but instead as discrete binary values, where 1 represents logic high and 0 represents logic low. One of the properties investigated in this report is the real electrical characteristics of these digital logic circuits. These circuits do not behave ideally and the real switching time of the circuits can lead to problems during circuit implementation.

The order in which the circuits are discussed is as follows: first, the resistively loaded NMOS, followed by the CMOS inverter, then the CMOS logic gate and finally the ring oscillator and the astable multivibrator.

2.1 NMOS inverter

The first inverter designed was the resistively loaded NMOS transitor. This designed features only one NMOS transistor in series with a resistor. The source is supplied some voltage and driven with a PWM source. The analysis of the NMOS circuit stems from two extreme cases: 1) the input V_{gate} is 0V and the voltage at the drain, $V_{drain} = V_{DD}$ and 2) input $V_{gate} = V_{DD}$ and output V_{drain}=0V. Case 1) describes the state in which no current is flowing through the MOSFET and the it is operating in cut-off. Case 2) described the state in which the transistor is operating in the triode region. The current through the MOSFET is described by Equation 1

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2], \tag{1}$$

where the drain current is found to be equal the hole mobility μ_n, the capacitance between the oxide terminals, the ratio of the width to the length of the channel, and V_t is the threshold voltage.

The design for resistively loaded followed by solving for an arbitrary input. For the purpose of this lab we are interested in V_{out}=2.5 when V_in=2.5 [2]. From these assumptions, it follows that $V_{GS} > V_t$ so the MOSFET is on, but somewhere in the triode to saturation range. It is known from $V_{DS} > V_{GS}$ that the MOSFET is in fact in saturation. Equation 1 simplifies to Equation 2

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_t)^2], \tag{2}$$

where the drain current now only depends on the gate voltage and the threshold voltage. For the CD4007, the k' parameter, seen in Equation 3

$$k' = \mu_n C_{ox} \frac{W}{L}, \tag{3}$$

where k' is equal to approximately $500\frac{\mu A}{V^2}$. From this current the load resistance can be found by application of Ohm's Law, which results in 4.4kΩ. The circuit was simulated using NGspice integrated with Matlab. The simulated circuit is shown in Figure 3.

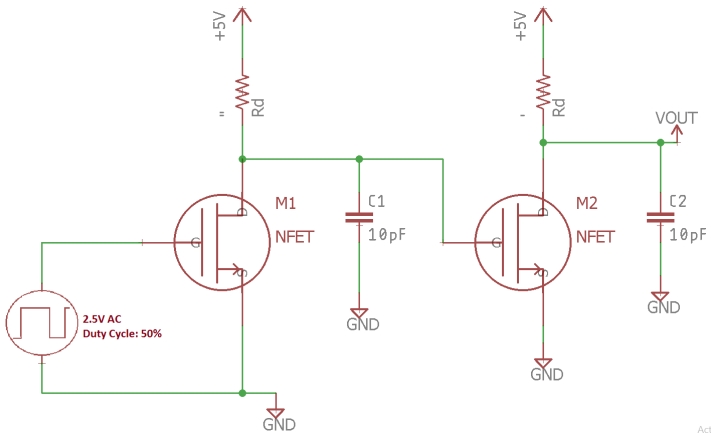

Figure 3: Simulated NMOS inverter

The parasitic capacitance of the breadboard was approximated by the inclusion of the 10pF capacitors at the outputs of the inverters. Figure 4 demonstrates the output voltage as a function of the load resistance. The output voltage was measured while performing a sweep of resistor values.

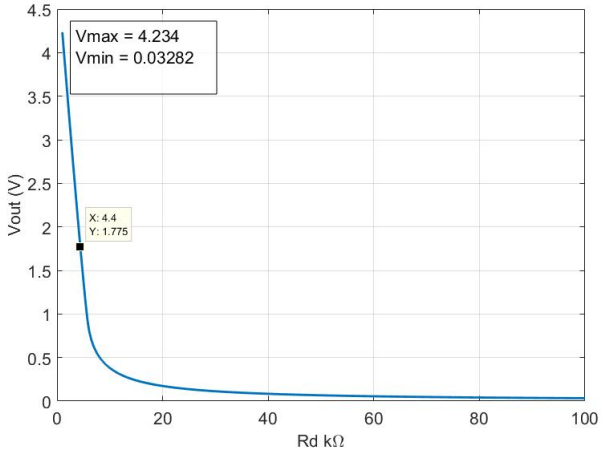

Figure 4: Simulated NMOS Vout vs R

The position of the calculated resistance in Figure 4 demonstrates the simulated output voltage at a 4.4kΩ value. Notably, the upper threshold of effective resistor values is around 9kΩ. The VTC of the NMOS inverter is shown in Figure 5 for three resistor values.

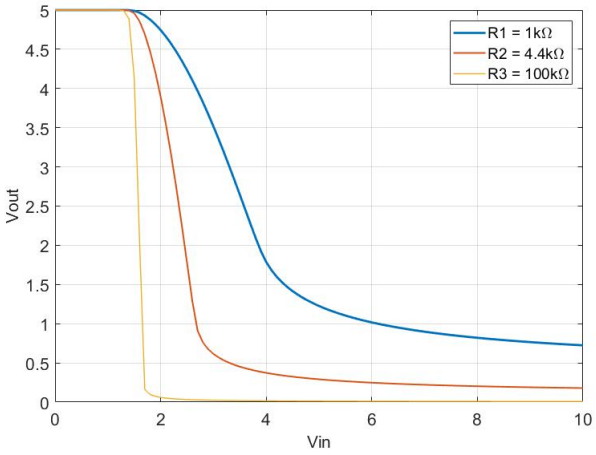

Figure 5: Simulated VTC of single NMOS inverter

The 100kΩ resistor features the most abrupt transition between logic states. The voltage at which it transitions, however, is below the supplied V_{in} of 2.5V, meaning this gate would subsequently change states at incorrect voltages. The 4.4kΩ resistor produces a transition at the voltage 2.5V, as calculated.

The transient analysis of the NMOS inverter was performed in NGSpice in conjunction with MATLAB. The time-domain graph of the inverter with a resistance of 1kΩ is shown in Figure 6.

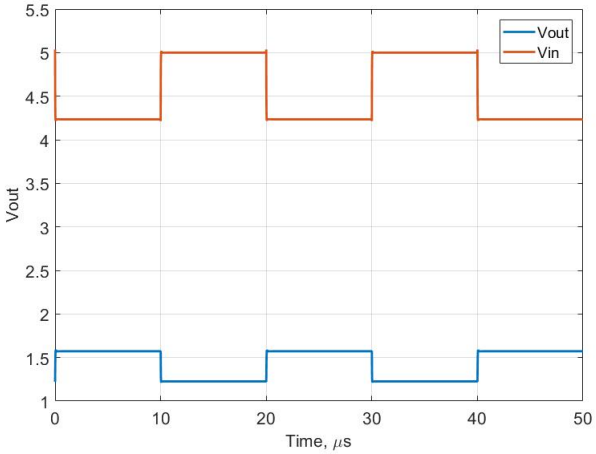

Figure 6: Simulated transient with 1k resistor

The output voltage is far below that of the input voltage in 6. The output waveform had a rise time of 129ns and a fall time of 122ns. The output waveform can then be contrasted with the output voltage calculated using a 4.4kΩ resistor seen in Figure 7.

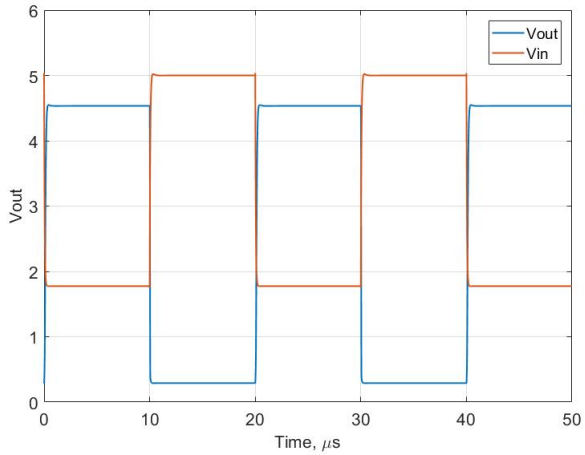

Figure 7: Simulated transient with 4.4k resistor

The output voltage, as seen in Figure 7, now outputs a voltage that is very nearly the supply voltage. The rise time was found to be 1.15 μs and the fall time was 133ns. The time-domain voltages for the 100kΩ resistor was also found, as shown in Figure 8.

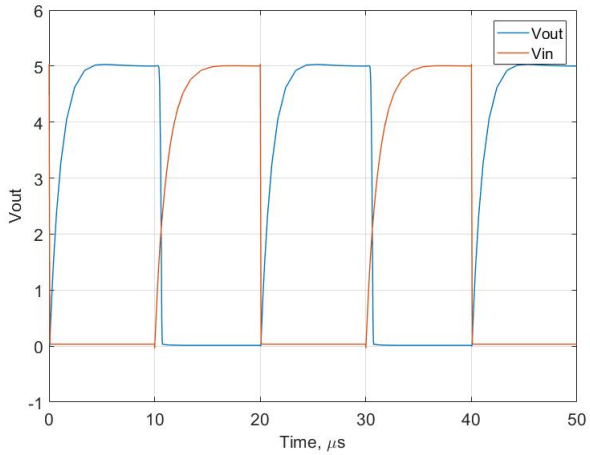

Figure 8: Simulated transient with 100k resistor

The introduction of the 100kΩ resistor dramatically increased the rise time of the output waveform. The rise time was found to be 12.1μs with a fall time of 1.19μs. The larger resistance increased the time constant of the equivalent RC circuit from the resistor and parasitic capacitance. The supply voltage was also increased in order to determine the effect on the inverter. Figure 9 shows the output voltage with a 10V supply and the 4.4kΩ resistor.

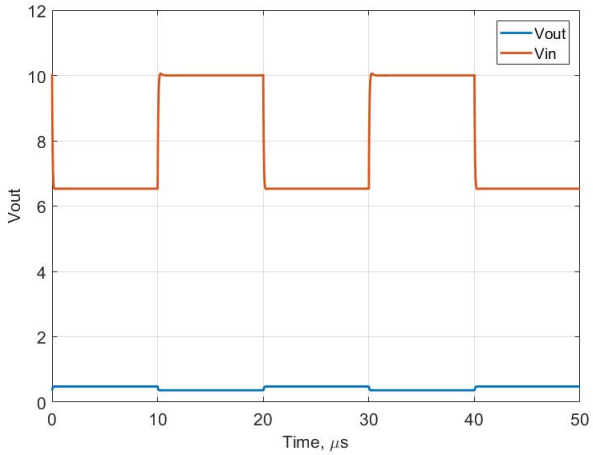

Figure 9: Simulated transient with 4.4k resistor and 10V supply

The output voltage decreases with the supply voltage, which agrees with Equation 2. The rise time was then found to be 1.11μs with a fall time of 185ns. The disparity between the supply voltage and the output voltage is seen when the supply is increased to 15V, as show in Figure 10.

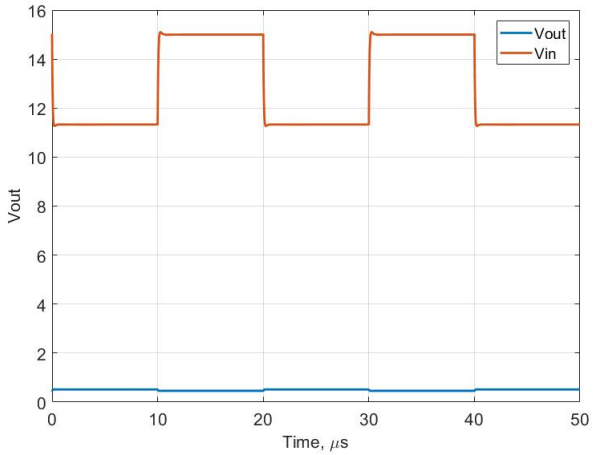

Figure 10: Simulated transient with 4.4k resistor and 15V supply

The rise and fall times were found to be 199ns and 195ns respectively. The supply voltage did not play a significant role in rise or fall times, but did dramatically alter the output voltage. Table 1 shows the simulated results for the NMOS inverter.

Table 1: NMOS simulated results

Values	Results
R	4.4kΩ
Min Power	69.5pW
Max Power	31.2mW
V_{max}	4.23V
V_{min}	32.8mV
Rise Time	129ns
Fall Time	122ns

The simulated results were in line with the theoretical values, the inverters operated as expected.

2.2 CMOS inverter

The CD4007UBE integrated circuit will be modeled using NGSpice in conjunction with MATLAB for this purposes of the simulations for the signal generator. In Figure 11, the pin connections for the IC as well as the internal design of the NMOS and PMOS MOSFETS connections.

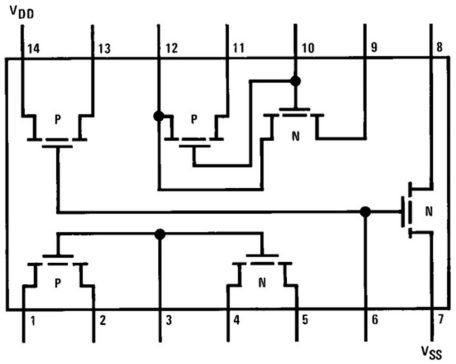

Figure 11: CD4007UBE internal schematic

There are two circuits that will be simulated. The first simulation is a CMOS inverter. The second simulated circuit will be a CMOS ring oscillator. Each of these simulations will be based on the design of the CD4007UBE IC. The CD4007UBE has three NMOS and PMOS transistors connected in pairs. The first two pairs have their gates connected to each other while the third pair have their gates and drains connected together. The third pair is best for implementing a single inverter due to it's connections.

2.2.1 CMOS inverter

The design of the CMOS inverter will consist of a pair of MOSFETS, one being a PMOS and one being an NMOS connected in series between V_{DD} and the reference, GND. The simulation schematic is shown in Figure 12 below.

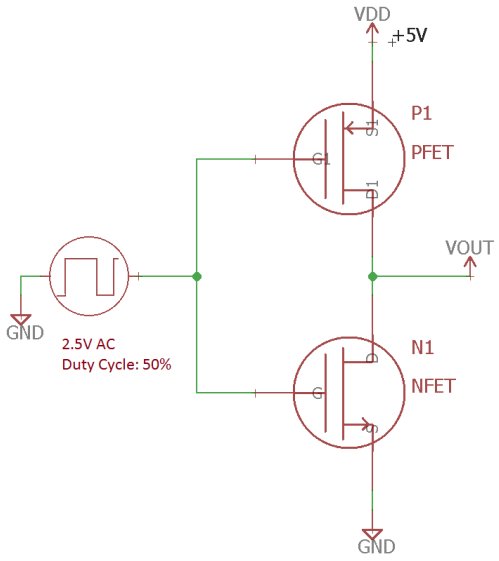

Figure 12: CMOS inverter schematic

Based on the characteristics of the CMOS inverter circuit, which contains a PMOS and NMOS, a load-line plot can be drawn representing the voltage transfer function characteristics, VTC. This graphical interpretation is shown below in Figure 13.

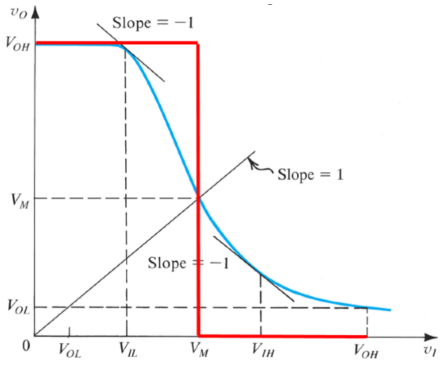

Figure 13: Voltage transfer function characteristics

In the first region of the VTC inverter graph, between 0 and before V_{IL}, known as the input voltage at the low logic state, the PMOS device is on. This is due to a low voltage being applied to it. The NMOS is essentially a large resistor because it has no use of free electrons, which disallows conduction. As a result, there is no current flowing through the inverter, so the output voltage is equivalent to supply voltage, V_{DD}, because there is no voltage drop across the PMOS. Once the voltage reaches V_{IL}, the NMOS is already on and saturated because of a large V_{DS} value.

At V_{IL}, the slope of the VTC is -1, which is the maximum input voltage in this state. Afterwards, there is a point in the VTC at V_M where $V_I = V_O$. This is the gate threshold voltage. At this time, the voltage dropped across the PMOS and NMOS are the same, and are both in a saturated state. In the area after the point V_M, the NMOS is conducting linearly, and the PMOS is being driven to saturation. The minimum voltage input at the high logic state occurs at V_{IH}, where the slope of VTC is once again -1 .

After V_{IH}, the NMOS will still technically be conducting, but the drain current is too small due to a small leakage current from the PMOS. In real world applications, this value is extremely small and negligible. In the case of CMOS inverters, $V_{OH} = V_{DD}$ at this stage. The simulated VTC matches the expected VTC graph as shown below in Figure 14.

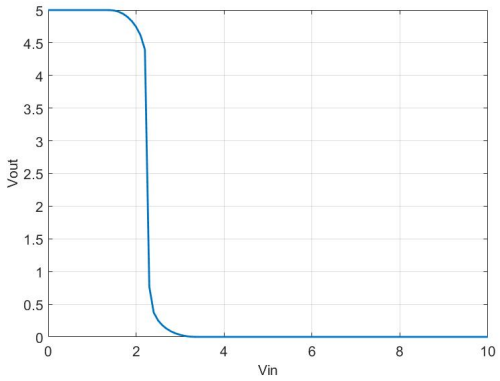

Figure 14: Voltage transfer characteristics - simulated

The simulated VTC graph shows voltage input at the low logic state, $V_{IL} \approx 0V$ and the input at high logic state, $V_{OH} \approx 5V$. The voltage output is essentially the same as the voltage input to the gate except it is inverted. This means that when the input is high, the output will be low and when the input is low, the output will be high. However, the input pulse wave has virtually no rise and fall time for the purposes of this simulation. The output, due to constraints places on it by the characteristics of MOSFETS, will have a rise and fall time for each pulsed wave. These can be seen in Figure 15.

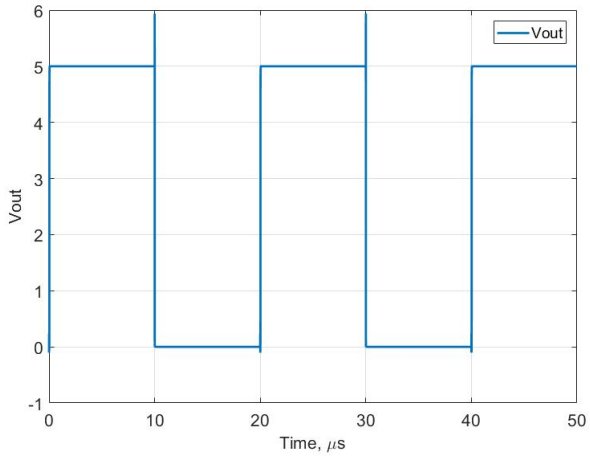

Figure 15: CMOS inverter voltage output

From the graph, the rise time is calculated as 142ns, while the fall time is calculated at 114ns.

2.2.2 CMOS astable multivibrator

The astable multivibrator is another circuit providing an oscillating output. The unique quality that this circuit has, compared to others, is that it has no stable state. Instead, it is in a continuously switching state. This is due to the feedback network which returns the output voltage to the gate of the first inverter, which in turn, causes the state of the input to switch. The oscillation frequency can be altered by the charge and discharge rates of the RC circuit. The operating frequency for the astable multivibrator is described by Equation 4 [3]

$$f = \frac{1.44}{RC}, \tag{4}$$

where the frequency is inversely proportional to resistance and capacitance. The constant 1.44 is a coefficient resulting from the derivation of Equation 4 [3]. The resistance can then be solved for in Equation 4, with an additional factor of three being added, due to three stages, to result in Equation 5.

$$R = \frac{1.44}{3fC}, \tag{5}$$

R is found to be 24kΩ when C is set to 1nF. The schematic for the astable multivibrator using a CMOS is shown in Figure 16.

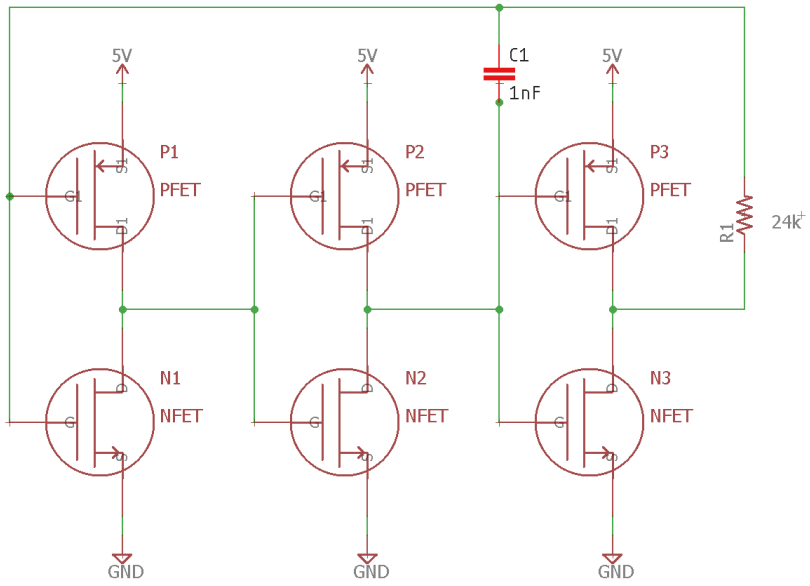

Figure 16: CMOS astable multivibrator schematic - simulated

The resulting waveform is found by using transient analysis in NGSpice, which is shown in Figure 17. The frequency was found to be approximately 19kHz. Subsequently, sensitivity testing was performed on the astable multivibrator using NGSpice.

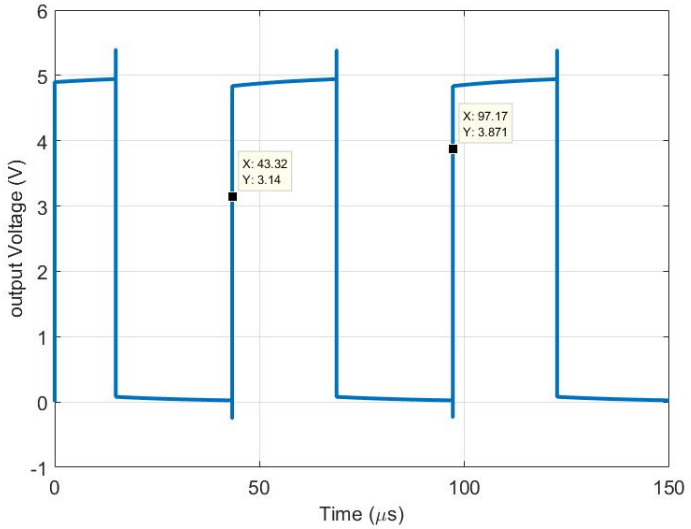

Figure 17: CMOS astable multivibrator output

Subsequently, sensitivity testing was performed on the astable multivibrator using NGSpice. First, 5% tolerance for capacitor values was simulated, and can be seen in Figure 18.

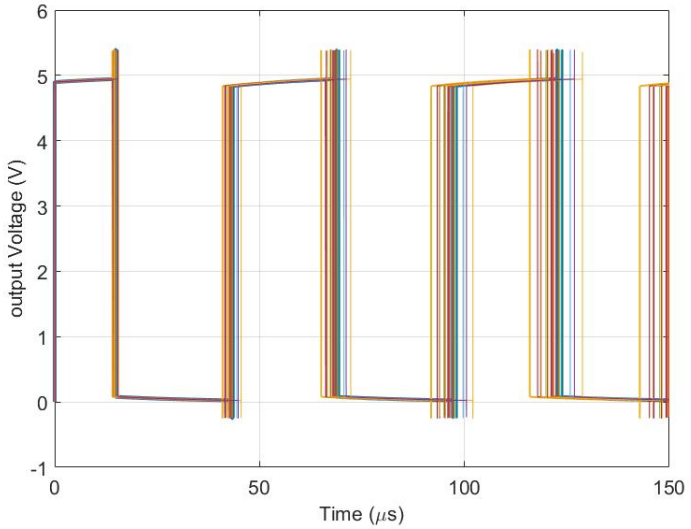

Figure 18: CMOS astable multivibrator - 5% tolerance simulated

This test was performed with 25 iterations, and the effect 5% tolerance had was significant. The effect, however, is even more dramatic when 10% tolerances are used. This can be seen in Figure 19.

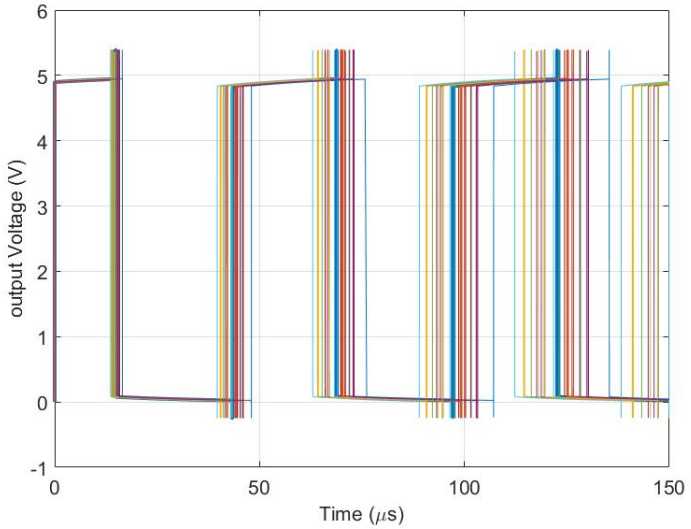

Figure 19: CMOS astable multivibrator - 10 % tolerance simulated

This test was performed with 25 iterations, and tolerances can play a key role in the operating frequency.

2.2.3 CMOS ring oscillator

The design of the CMOS ring oscillator will consist of three CMOS inverters connected in series with the output of the last inverter connected to the input of the first inverter. The ring oscillator will also have a capacitor at each output connected to ground. The schematic for the CMOS ring oscillator can be seen in Figure 20.

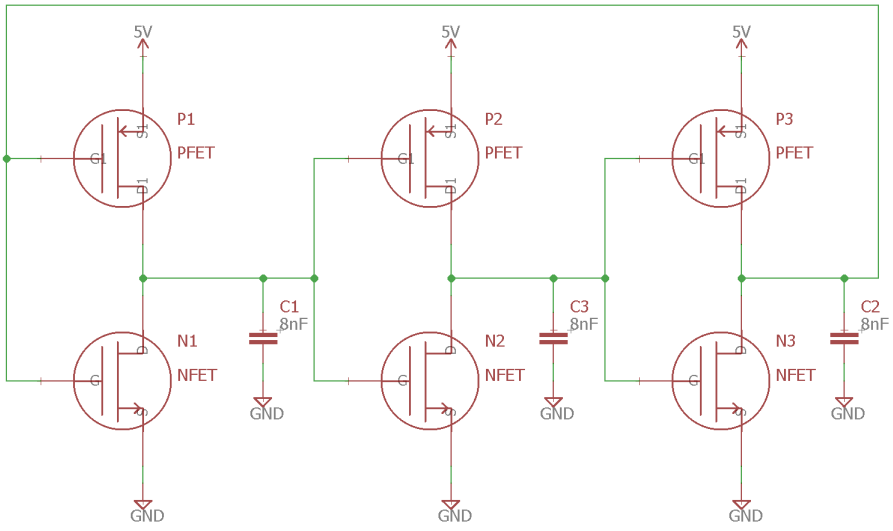

Figure 20: CD4007UBE ring oscillator

The operation of the ring oscillator uses a series of inverters. The output of one inverter inverts the input signal. Therefore, if there are a series of inverters, then each odd inverter will have the same inverted output as the first. In this instance, there are three stages of inverters used, with the output of the third inverter being fed back into the input of the first inverter. This feedback from the output to the input causes an oscillation. Based on this, it would be impossible to provide an oscillation using an even number of inverters connected in series.

The ring oscillator circuit requires only a DC power source with a threshold voltage above what is required of the MOSFETS, and the oscillations will occur. To increase the frequency, the DC supply can be increase, causing an increase in current as well as frequency.

The inverse of the oscillation frequency, the oscillation period, is based on the delay in each stage of the ring oscillator. The period is equivalent to double the sum of all propagation delays. These delays are caused by gates being unable to switch instantly in the real world. In this case, the gate capacitance must be charged before a connection is made between the source and the drain. Otherwise, current will be unable to flow between the source and the drain. The time it takes for the gate capacitance to reach the necessary charge adds a delay to the oscillator. Increasing the number of stages increases the delay time and reduces the frequency. The output waveform is shown in Figure 21.

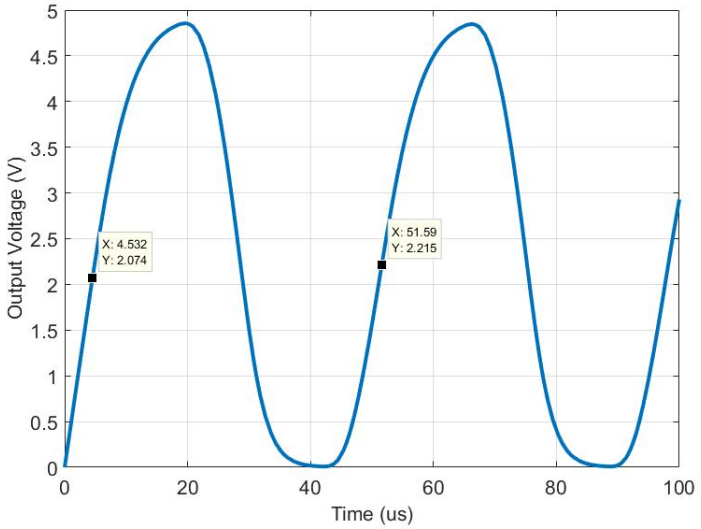

Figure 21: CD4007 ring oscillator output

The operating frequency was found to be approximately 20kHz. Sensitivity testing was performed on the circuit, as seen in Figure 22. The simulated output based on a tolerance of $\pm$ 5% in each of the capacitor values is shown.

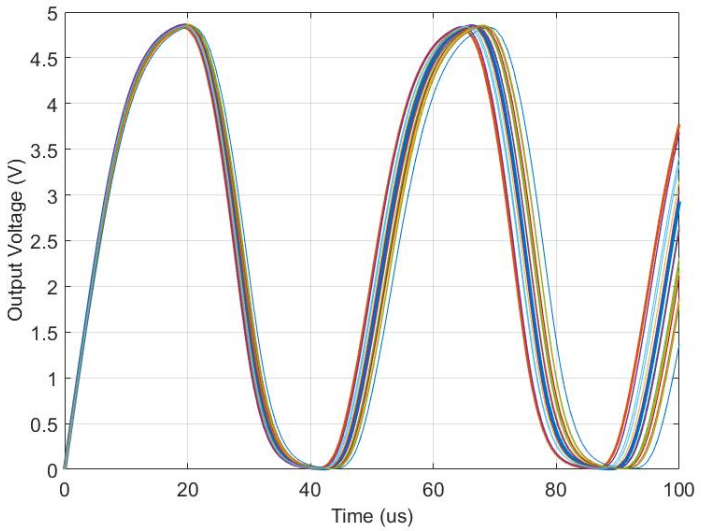

Figure 22: CD4007 ring oscillator - 5% tolerance simulation

As the simulation shows, this slight change in values has an undesired affect on the outputs. Despite only a small percentage change in capacitor values, the output of at 5% does not stray too far from the expected output at ideal values. The simulated output in Figure 23.

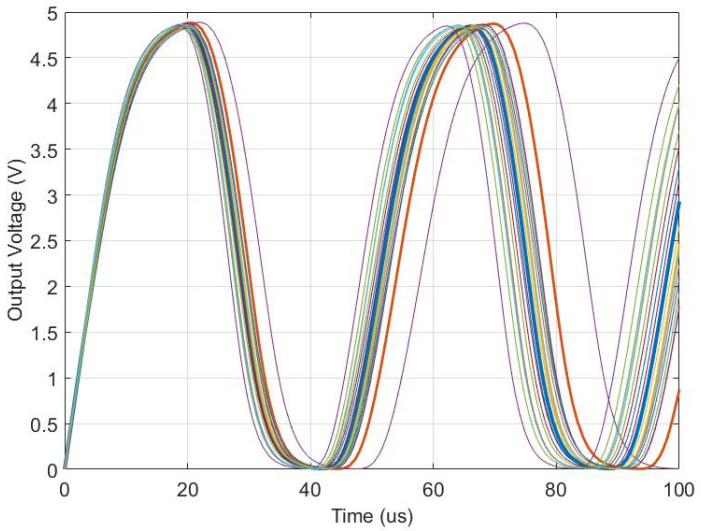

Figure 23: CD4007 ring oscillator - 10% tolerance

As the tolerance of the capacitors in the ring oscillator increase, it causes a larger discrepancy in the values. As time goes on there are variances of almost $10\mu s$ between simulated outputs. Based on these simulations the propagation delay caused by the gates is $\tau_P = 110ns$. The capacitor values were not calculated. Instead, the initial value of 1nF was chosen, then increased until a suitable output was found.

3 Experimental Implementation

The CD4007UBE is a model featuring four on board CMOS circuits tied together. The various circuits were constructed by utilizing these onboard CMOS circuits. The experimental results will be discussed as follows: the NMOS inverter, the CMOS inverter, the AND logic gate, the ring oscillator, and finally the astable multivibrator.

3.1 NMOS inverter

The only change required by the NMOS inverter is that the 4.4kΩ resistor was switched to a 4.3kΩ resistor due to the lack of the availability of the 4.4kΩ resistor. The substitution of a 4.3kΩ in series with a 100Ω with 5% tolerances would introduce too much error into the design.

The VTC of the NMOS inverter is shown in Figure 24.

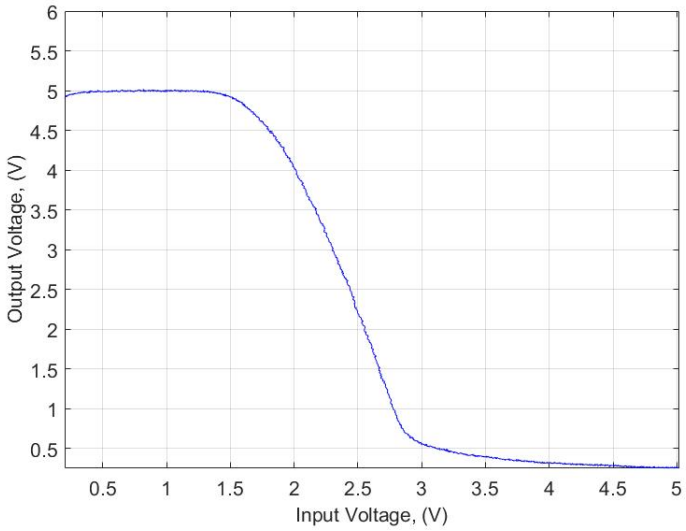

Figure 24: Experimental VTC NMOS

The respective voltages for logic low versus logic high are shown. As expected from simulations, the low logic is not 0V, but instead a rather significant voltage. This accounts for the comparatively significant power consumption used by the NMOS inverter. The power consumption was found to be 5.8mW for logic high and 37μW for logic low. The output waveform is shown in Figure 25

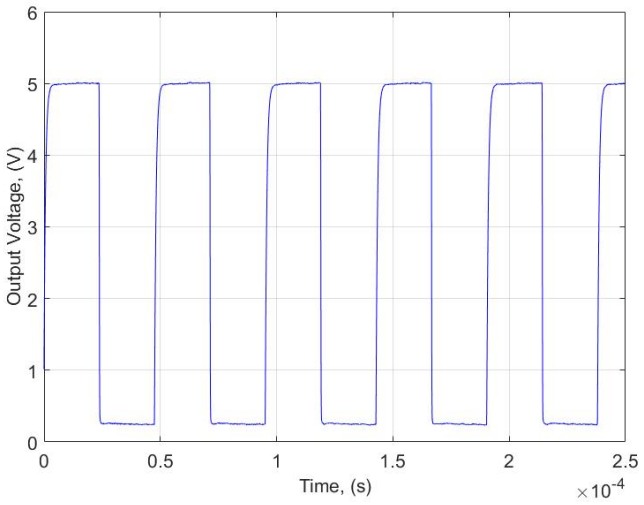

Figure 25: Measured output of NMOS inverter

The rise and fall times were found by the Digilent scope, the rise time was 11.4μs, and the fall time was 1.22μs. The experimental values for the NMOS inverter is shown in Table 2.

Table 2: Experimental values

Experiment Values	Results
R	4.3kΩ
Min Power	37μW
Max Power	5.8mW
V_{max}	5V
V_{min}	400mV
Rise Time	11.4μs
Fall Time	1.22μs

The experiment values that are expressed in Table 2 are different than the simulated due to real world parasitic capacitance and limitations of the breadboard at higher frequencies. The experimental results are as follows: the output voltage, which did not saturate; the frequency response, with a center frequency of 20.2kHz; and the bench test, where the specifications were met.

3.2 CMOS inverter

The only change required for implementation was that all three CMOS inverters were wired together in order to create three inverters in series as opposed to the only simulated two. The measurements were still taken from the output of the first stage. The VTC from the first stage is shown in Figure 26

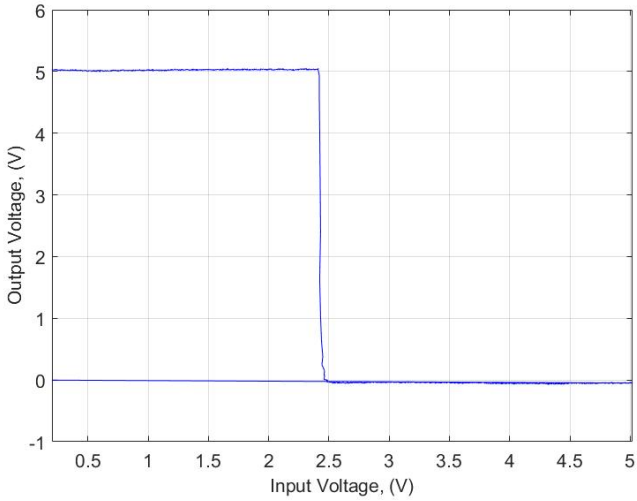

Figure 26: Measured VTC of CMOS inverter

The VTC, as seen in Figure 26, represents logic low as 0V, and improvement over the 400mV of the NMOS inverter. The CMOS inverter also features $0V_{DC}$ power consumption opposed to the NMOS inverter. The output waveform for the CMOS is shown in Figure 27.

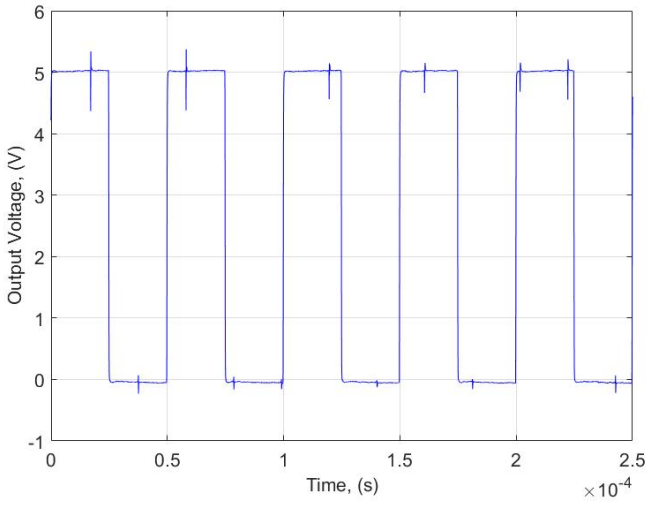

Figure 27: Measured output of CMOS inverter

The subsequent rise and fall times were measured using the Digilent and were found to be 235ns for rise time and 177ns for the fall time. These are greater than those of the simulation, but is not unexpected due to parasitic capacitances and inductances from the jumper wires.

3.3 AND gate

The AND gate was created using all three CMOS circuits on the chip. A NAND gate was constructed using the first two on board CMOS circuits which were then inputed to a CMOS inverter. Figure 28 shows the pinout for an AND gate using the CD4007 IC.

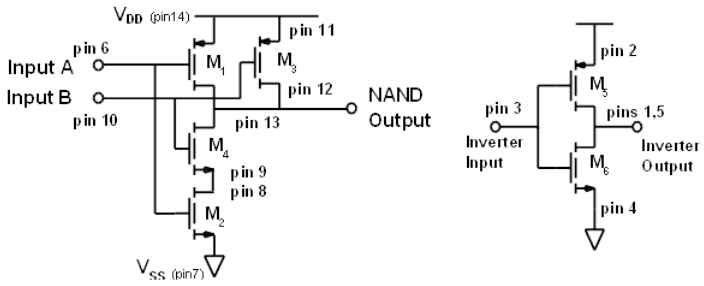

Figure 28: Pinout for AND gate

The output from the NAND gate but before the inverter is expressed in Table 3.

Table 3: Truth Table: NAND

Inputs		Output
A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

The inputs A and B were created by using the Digilent wave generator set to the DC setting, a logic 1 was 2.5V and logic 0 was 0V. The final output after the inverter is expressed in Table 4.

Table 4: Truth Table: AND

Inputs		Output
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

The time-domain graphs for these outputs are of little value, as they express simply a DC voltage at either 2.5V or 0V.

3.4 Ring oscillator

The experimental oscillator required several changes. 8.2nF capacitors were the closest value available to the calculated 8nF. The circuit built with the 8.2nF operated at a frequency of 22.8kHz, which is not within specifications, that frequency is too far outside the bandwidth of the MFBP filter from the previous lab. An additional 4.7nF capacitor was added in parallel with the second stage of the oscillator, resulting in the final circuit is shown in Figure 29.

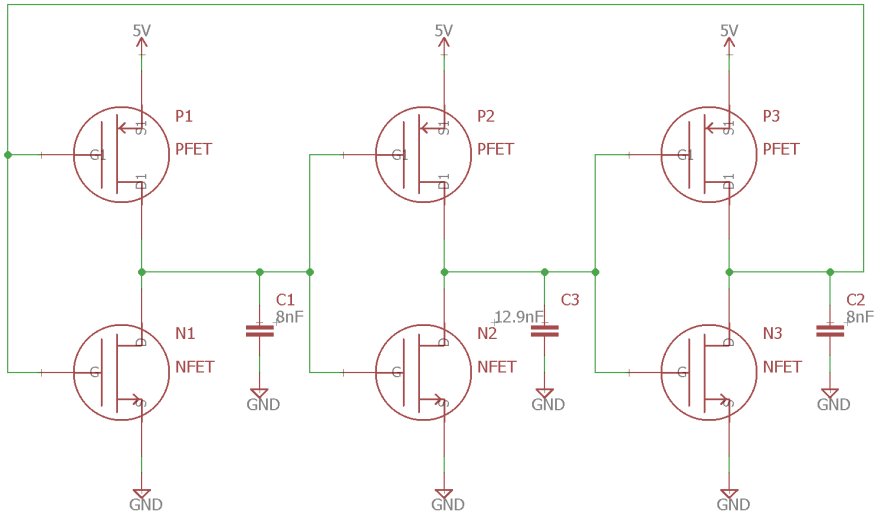

Figure 29: Experimental ring oscillator circuit

The transient analysis was performed on the circuit using the Digilent Scope function. The output waveform is shown in Figure 30.

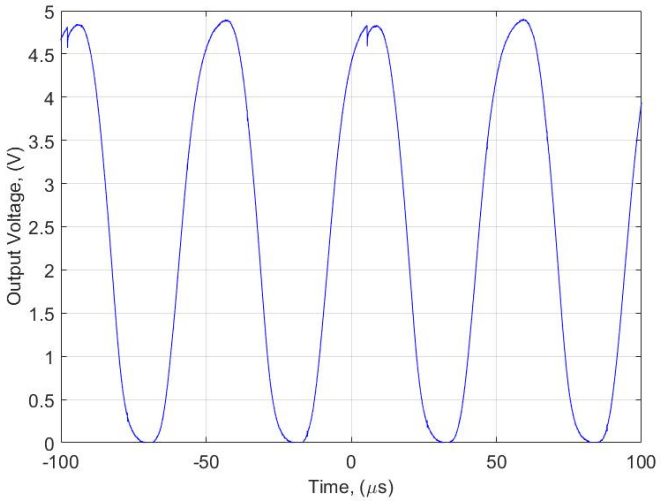

Figure 30: Experimental transient analysis

The frequency was found to be 19.8kHz, a 51% duty-cycle, with a 4.9V peak to peak amplitude. This frequency falls well within the bandwidth of the MFBP filter.

The final experimental results are summarized in Table 5.

Table 5: Experimental results

Value	Experimental
Center Frequency	19.8 kHz
Duty-cycle	51%
Amplitude	4.9V

The experimental results fall within the lab specifications outlined.

4 Discussion

This lab served as introduction to MOSFETS and implementation of digital logic. When using transistors to create digital devices, it is often assumed that the device behaves ideally. When the device is logic high, it is one voltage, and when it is logic low it is another. Based on this logic, it is assumed that the switching on and off of the MOSFETS happen instantaneously. Based on the results of the ring oscillator and other inverter circuits, the MOSFETS do not switch instantaneously. Instead, power is consumed by the MOSFETS when they transition from one state to another. This consumption of power causes a small time delay. Each of the circuits described in this report are discussed in the following subsections, excluding the astable multivibrator. The astable multivibrator was not constructed during the experimental phase of this task.

4.1 NMOS inverter

The NMOS inverter worked as simulated and required no significant design changes in order to function. The measured power consumption was different from the simulated values, but it operated within a tighter band of values. The comparison of the NMOS with simulations is shown in Figure 6.

Table 6: Comparison of NMOS

Component Values	Simulated	Experimental
R	4.4kΩ	4.3kΩ
Max Power	31.2mW	5.8mW
Min Power	69.5pW	37μW
Rise Time	199ns	11μs
Fall Time	195ns	1.22μs

The rise and fall times were significantly greater as well. This can be accounted for by the fact the implemented circuit, in addition to board parasitic capacitance, also had capacitance from the jumpers connecting the pins of the device. Each jumper added capacitance to the circuit, which in turn increased the time constant for the circuit, which would account for the increased transition times.

4.2 CMOS inverter

The CMOS inverter required no changes from simulation. The circuit behaved as expected, with the VTC matching that of the simulations. One of the strengths of the CMOS is the faster transition between logic states. This is reflected in the slope of the experimental VTC. The CMOS also represents logic low with zero volts, as opposed to the NMOS were logic low was still some positive voltage. The DC power consumption of the CMOS was also negligible compared to that of the NMOS. Table 7 shows the differences between the simulated and measured CMOS circuit.

Table 7: CMOS inverter comparison

Component Values	Simulated	Experimental
Rise Time	142ns	235ns
Fall Time	114ns	177ns
Power	0	5μW

The difference in rise and fall times can be ascribed to the parasitic capacitances from the board and jumper wires.

4.3 AND gate

The AND gate operated as expected. This lab served as an introduction to the use of transistors as logic devices. The use of binary logic is fundamental in the design of digital logic. The construction of a physical AND gate demonstrates the real device characteristics of logic circuits. The truth table for the constructed AND gate is shown in Table 8.

Table 8: Truth Table: AND

Inputs		Output
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

The AND gate, in addition to the OR gate, are the fundemental building blocks for digital logic, and thus are of the utmost importance.

4.4 Ring oscillator

The ring oscillator circuit designed with the CMOS did not initially meet the specifications required in the lab. The simulations were accurate, but real-world parasitic capacitances from the board and jumper wires impacted the circuit. To remedy the situation, a capacitor of 4.7 nF was added in parallel after the second inverting gate. By increasing the capacitance the frequency was lowered from 22.8 kHz to 19.8 kHz. The comparison between the simulated results and experimental is expressed in Table 9

Table 9: Comparison of ring oscillator results

Component Values	Simulated	Experimental
C_1	8nF	8.2nF
C_2	8nF	13.9nF
C_3	8nF	8.2nF
Frequency	20.1kHz	19.8kHz
Amplitude	5V	4.9V

The reason this oscillator is chosen over the astable multivibrator as the signal generator is mostly arbitrary and simply design choice for the optical uplink project [4]. Although one of the benefits of the ring oscillator is that from the sensitivity testing it is less affected by component tolerances than the astable multivibrator. This is significant since the capacitors available for circuit construction are 10% tolerances.

5 Conclusion

The design, simulation, and implementation of the ring oscillator signal generator have been explained. NMOS inverters, CMOS inverters, and logic gates were also investigated. Lab specification required that the signal generator have a frequency of approximately 20kHz, a duty-cycle of approximately 50%, and an amplitude of 5V. The signal generator takes an input DC voltage and creates an sinusoidal waveform at the output. The signal generator circuit was constructed using the following parts: three 8.2nF capacitors, a 4.7nF capacitor; and finally a CD4007 CMOS integrated circuit with 5V supply voltages. The frequency was 19.8kHz, with a duty-cycle of 51%, and an amplitude of 4.9V. An important lesson about the behavior real logic circuits was learned. Real digital circuits have measurable electrical characteristics and do not behave ideally.

References

[1] D.E. Kotecki Lab.(2017) Lab #2 Active Bandpass Filters [Online]. Available: http://web.eece.maine.edu/ kotecki/ECE342/labs/ECE342_2017_Lab2.pdf

[2] D.E. Kotecki Lab.(2017) Resistively Loaded MOSFET Gate [Online]. Available: http://web.eece.maine.edu/ kotecki/ECE342/labs/ECE342_2017_Lab3_Inverter.pdf

[3] Texas Instruments, "LM555 Datasheet", http://www.ti.com/lit/ds/symlink/lm555.pdf

[4] N.W. Emanatoglu.(2017) Lab #3; MOSFET based logic gates [Online]. Available:http://web.eece.maine.edu/ kotecki/ECE342/labs/ECE342_2017_Lab3_Briefing.pdf

D LED Driver

Task 4: LED Driver

Optical Uplink

Joseph Arsenault
Ryan Dufour
Phil Robb

Abstract

The design, simulation, and construction of an LED driver circuit are described. In task 4 of the optical uplink project, a signal conditioning circuit and current driver are explored. A signal conditioner using the MCP6004 operational amplifier as a Schmitt trigger was built in order to output a square wave with 50% duty-cycle. The current driver was constructed using a MCP6004 operational amplifier which drives an 2N3904 BJT. The current driver receives the output voltage from the conditioner and converts it to a current signal which controls an IR1503 LED. The output of LED driver was required to operated at approximately 20 kHz, 50% duty-cycle, with a current of at least 100mA amplitude. The final current operated at a frequency of 20.1 kHz, a duty cycle of 50.1% and a 150mA peak amplitude.

Electrical and Computer Engineering
University of Maine
ECE - 342
December 11, 2017

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1 Introduction

This report describes design, implementation and test of an LED driver comprised of a ring oscillator, Schmitt trigger, and a current driver. The ring oscillator is comprised of complementary metal oxide semiconducting field effect transistors (CMOS) inverters connected in series. Figure 1 demonstrates where in the optical uplink project the LED driver is placed.

Figure 1: Block diagram for optical uplink [1]

The LED driver is required by the optical uplink project. The signal generator chosen for the overall design does not output a high enough current in order to operate the IR LED. In addition, the waveform from the signal generator is a distorted sinuisoid without a 50% duty-cycle. For ideal operation, the LED should receive a 50% duty-cycle square wave. In addition, it requires a forward voltage of at least 100mA in order to operate.. The specifications for this lab are summarized in Table 1.

Table 1: LED driver specifications

Specifications	Required
Frequency	20kHz±5%
Duty-cycle	50%
Amplitude	≥100mA

The LED driver circuit supplies the LED with a controlled current. A signal conditioner takes the output from a ring oscillator and creates a 50% duty-cycle square wave. The square wave is then in turn recieved by a current driver. The current driver creates a sufficiently large current in order to operate the LED. A voltage driven output to light the LED is not used due to increased sensitivity from temperature change.

Section 2 of this report describes the design and simulations of the signal conditioner and the current driver. Experimental results are addressed in section 3. A discussion of the results, sources of error, and areas of possible improvement are outlined in section 4. Section 5 concludes this report.

2 Circuit Development

This section covers the design choices associated with the various circuits constructed. The individual circuits designed were a Schmitt trigger configured op amp as the signal conditioner and an op amp driving a BJT for the current driver. The input waveform was generated using the ring oscillator from Lab 3. A voltage regulator supplied a steady 5V from a 9V battery source.

The order in which the circuits are discussed is as follows: first the signal conditioner, then the current driver, and then finally the voltage regulator.

2.1 Signal conditioner

In order to activate the IR LED correctly it must be driven with a square wave. The generated waveform from the ring oscillator circuit is, however, a distorted sinuisoid. The signal must therefore be transformed into a square wave. This requires the use of a signal conditioner. A Schmitt trigger was chosen to implement the signal condition. The Schmitt trigger is an positive feedback configuration for a noninverting amplifier. The Schmitt trigger is described most succinctly by its transfer function, seen in Figure 2.

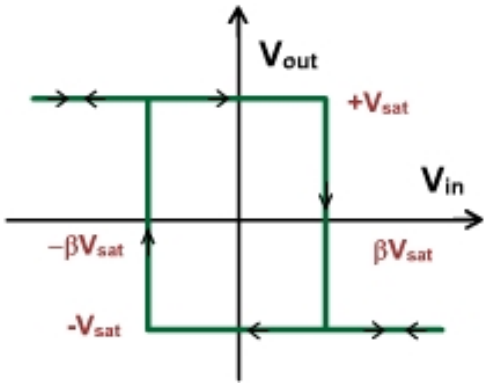

Figure 2: Transfer Function of Schmitt Trigger [2]

The Schmitt trigger outputs two discrete voltages, which are set by the reference node at V_{-}. This voltage determines when the output voltage drops to the low or up to its high voltage. The simulated circuit is shown in Figure 3.

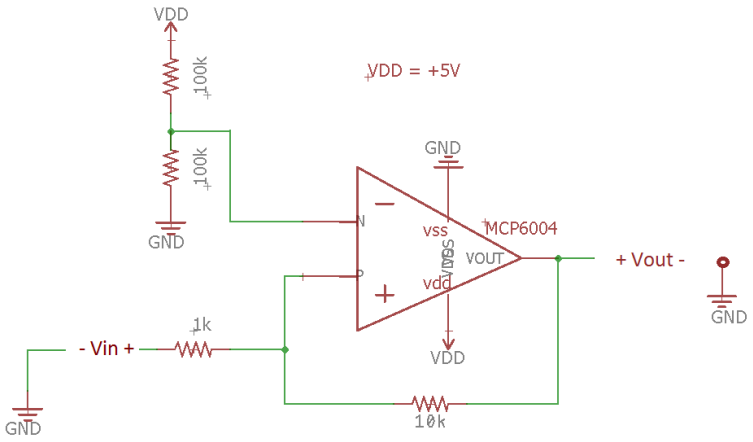

Figure 3: Simulated signal conditioner circuit

The input to the signal conditioner is the 5V peak sinuisoid from the ring oscillator. In order to attain a 50% duty-cycle, the reference voltage should be set to half of the input signal. As a result, the voltage divider at the reference node is a 50/50 voltage divider, resulting in 2.5V at the reference node. The feedback configuration is set to $10V/V$ to ensure that the output from the signal conditioner is 5V. When the input signal is about the reference voltage, the Schmitt trigger is "high" and when the signal is below the

reference voltage the output is "low". This results in an output square wave. The output waveform can be seen in Figure 3.

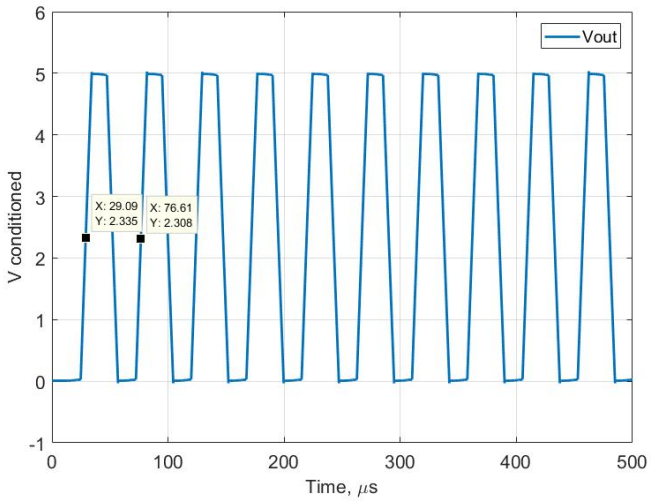

Figure 4: Simulated conditioned signal

The output was simulated by doing transient analysis in NGSpice integrated with Matlab. The signal was measured to have a 20 kHz frequency, a 48% duty-cycle, and a 5V peak amplitude. The reason that the output does not switch instantaneously from high to low is because the op amp is slew rate limited. This output was then passed to a current driver.

2.2 Current driver

The current driver for this lab was created using an MCP6004 op amp. The op amp is to act as the driver for the gate of a 2N3904 Bipolar Junction Transistor (BJT). The generic circuit for the current driver is shown in Figure 5.

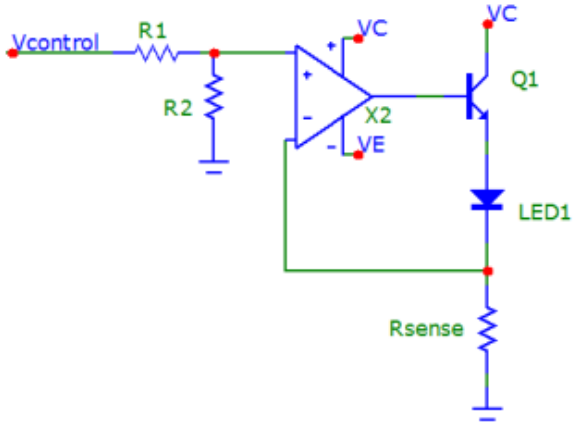

Figure 5: Generic current driver circuit [1]

The key to operation of the current driver is the BJT. A BJT, in contrast with the metal oxide semi-conducting field effect transistor (MOSFET), is capable of producing current by both types of Charge Carriers. This effectively allows the BJT to behave as a NPN or PNP transistor depending on the size of the input current. This also allows the BJT to use a smaller current signal to control a larger current.

The electrical properties of a BJT are paramount for this lab. The MCP6004 is only capable of outputting around 20mA of current. The IR LED in use, however, has a forward current of 100mA [4]. A much larger current has to generated in order for the LED to operate. Figure 6 shows the IV curve for the IR1503 LED.

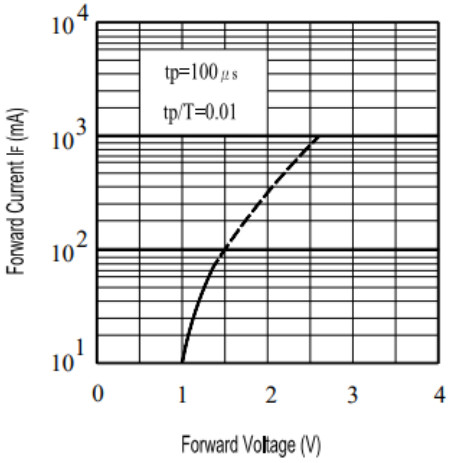

Figure 6: The IV characteristic of the IR1503 [4]

The MCP6004 is used to set the node voltage for R_{sense}. The op amp is assumed to be ideal, so $V_- = V_+$. In order to ensure that the LED is forward biased, the node voltage should be less than the sum of the voltage drops from V_{supply} over the BJT and the diode [3]. The lab briefing [3] states to set V_- less then 3V.

In order to attain a suitable voltage, a voltage divider is placed at the input to the op amp. The source voltage is the output from the signal conditioner, and was found to be 5V. In order to be less than 3V, a 50/50 voltage divider was used in order to create an input of 2.5V. With this voltage, and the maximum forward current of 200mA, the value for R_{sense} can solved using Ohm's Law. The final value for R_{sense} is 12Ω. The simulated circuit for current driver is seen in Figure 7.

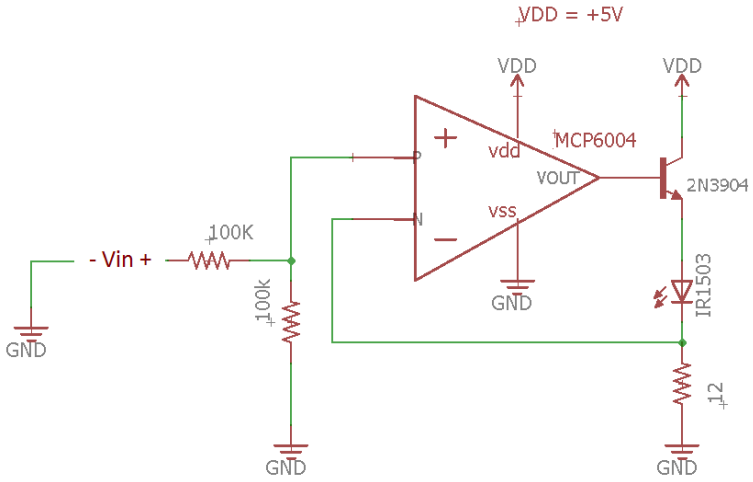

Figure 7: Simulated LED driver circuit

The circuit required no changes from design to simulation. The current through the LED can be seen in Figure 8. The simulation was performed using a transient analysis in NGSpice integrated with Matlab.

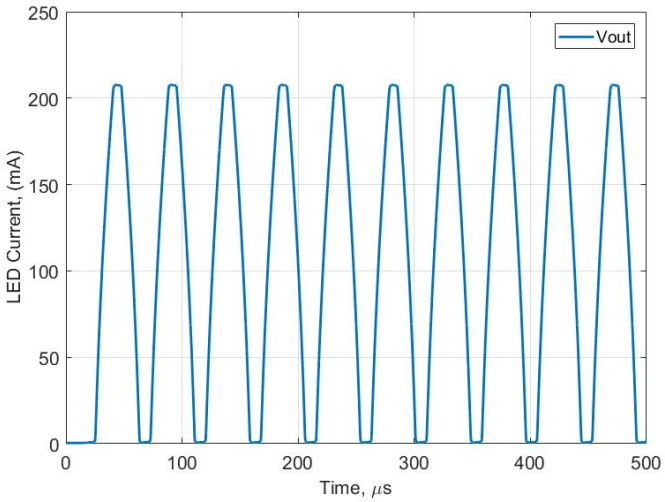

Figure 8: Simulated current through the LED

The current through the LED matched the calculated value of 200mA. The LED is in an operational state. The LED also operates with the correct frequency and duty-cycle from the signal conditioner.

2.3 Voltage regulator

The Voltage regulator used was a LM7805. The voltage regulator is used because the CMOS ring oscillator and LED driver were designed to run on a source voltage of 5V. The power supply provided, however,

is a 9V DC battery. The voltage, therefore, needs to be reduced. The voltage regulator operates by taking an input voltage and step it down to some lower voltage by shedding the difference in energy between the two potentials in the form of heat. Figure 9 shows the circuit configuration for the LM7805.

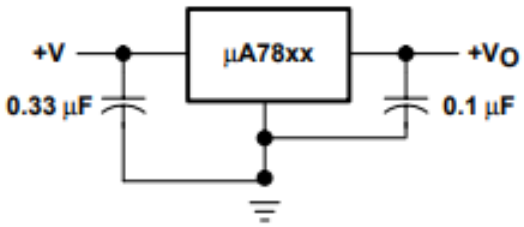

Figure 9: Configuration of voltage regulator[5]

The equivalent circuit model for the LM7805 is shown. Notably, the circuit was not included in simulations and was constructed during the Implementation phase.

2.4 Simulated summary

The final simulated circuit is shown in Figure 10.

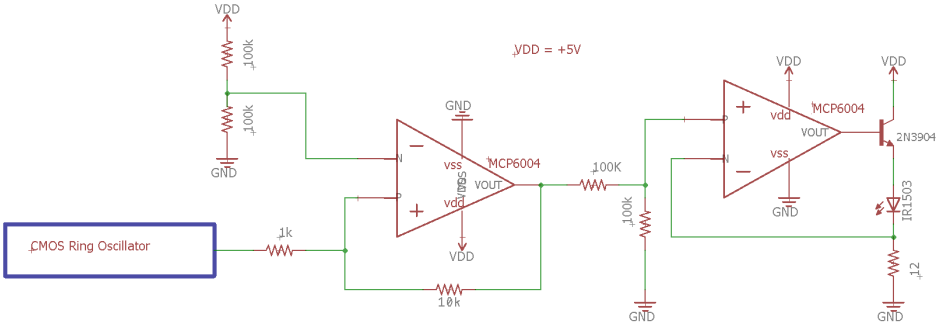

Figure 10: Simulated LED driver

The simulated circuit did require any changes from calculations. One of the most significant margins of error for simulations is that the operation of the simulations is quite dependent on which simulation model for the 2N3904 is used. The "SP3" model from ON Semiconductor was utilized for these simulations [6]. Different models are capable of behaving in unexpected ways due to their interaction with the NGSpice simulation software. The summary of simulated results from this circuit is shown in Table 2.

Table 2: Simulated Results

Component	Simulated Values
Conditioned Voltage	5V
Conditioned Frequency	20kHz
Conditioned Duty-Cycle	48%
Output Current	200mA
R_{sense}	12Ω

The simulated signal conditioner outputted only a 48% duty-cycle directly and is slightly less than the required 50%. However, the final waveform through the LED operated with a 50% duty-cycle as required by specifications. The simulated circuit operated as expected and provided enough current in order to drive the LED. The resulting waveform through the LED is the correct frequency and duty-cycle.

3 Experimental Implementation

The final circuit is shown in Figure 11.

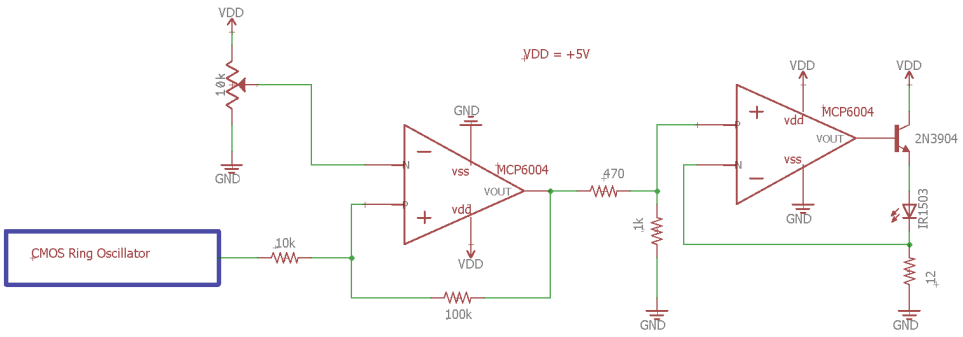

Figure 11: Experimental design

In order to meet specifications, several minor changes to all circuits were made. The individual changes are discussed in their respective subsection as follows, the signal conditioner then the current driver.

3.1 Signal conditioner

The signal conditioner required several small changes in order to be functional. The changes are shown below in Figure 12.

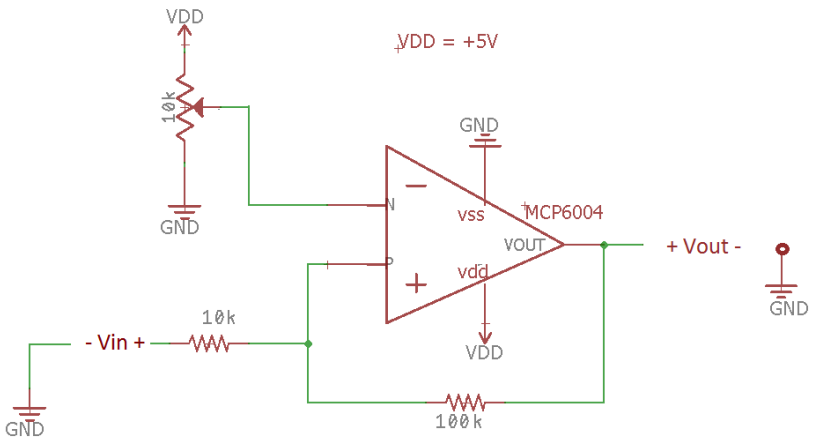

Figure 12: Experimental signal conditioner schematic

The 100kΩ resistor voltage divider was switched to a 10kΩ potentiometer in order to facilitate easier adjustment of the output duty-cycle. The resistors in the feedback configuration were changed to 10kΩ and 100kΩ. This was done in order to minimize the loading effects between the signal conditioner and the current driver. The output waveform is shown in Fig 13.

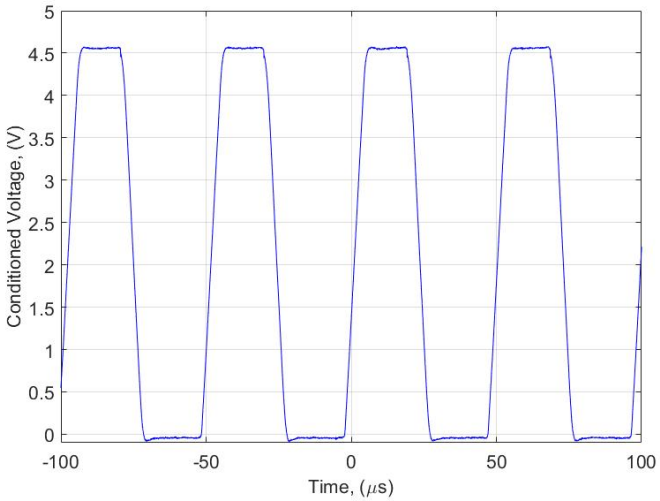

Figure 13: Voltage output of signal conditioner

The output waveform operated with a 4.5V peak, 20.26kHz and 45% duty-cycle. Table 3 summarizes the differences between the simulated and implemented current driver.

Table 3: Comparison of implemented driver

Component Values	Simulated	Experimental
R_1	100kΩ	470Ω
R_2	100kΩ	1kΩ
R_{sense}	12Ω	12Ω
Output current	200mA	150mA
Output current	200mA	150mA

Overall, the circuit required only minor changes to operate within specification.

3.2 Current driver

The constructed current driver that supplies the LED with a controlled current needed a design change from the simulated model. The voltage divider required a change to lower resistance values. The reason for this to reduce loading effects between the signal conditioner and the current driver. This also slightly increased the peak voltage of the signal conditioner output. The schematic for the current driver is shown in Figure 14.

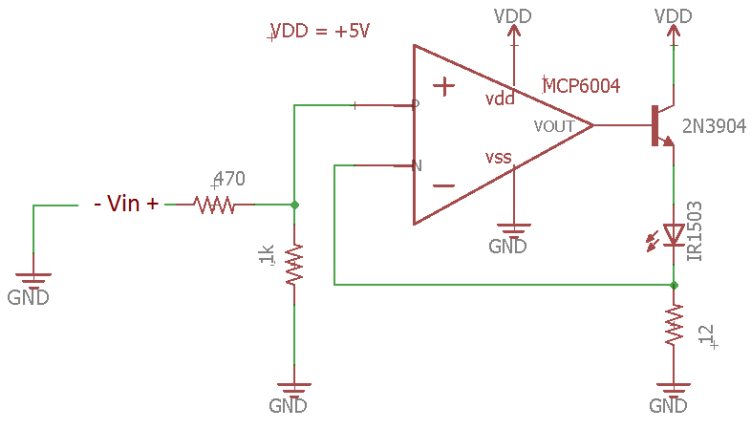

Figure 14: Final schematic of current driver

The resulting output of current through the 12Ω resistor is shown in Figure 15. The output from the current driver operated with at 20.1kHz with a 50.1% duty-cycle.

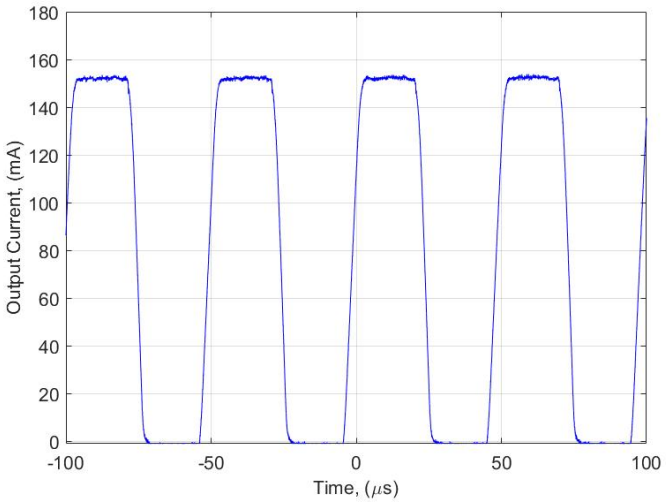

Figure 15: Experimental output of current driver

The experimental output differed from the simulated output shown in Figure 8. The greatest difference between them is the output current peak. The simulated peak current was $\approx$ 200mA, while the experimental output was $\approx$ 150mA. The duty cycle remains unaffected because the circuit allows it to be variable by adjusting the potentiometer depicted in the signal conditioner schematic, Figure 12.

4 Discussion

After several minor changes, the circuit operated correctly. This lab served as introduction to circuits that include both transistors and op amps. The two types of components have been studied separately, but never in conjunction. The specifications are outlined in Table 4.

Table 4: Driver specifications

Specifications	Required
Frequency	20kHz$\pm$5%
Duty-cycle	50%
Amplitude	$\geq$100mA

Notably, the ring oscillator had to have the its output frequency increased. This was due, in part, because of parasitic inductances and capacitances from the board and jumper wires. The propagation of the signal from the oscillator to output resulted in a decrease of frequency. Therefore, increasing the input frequency resulted in a correct output of the LED driver.

Another factor that determined the operating frequency is the fact that most of the components are temperature dependent. The MCP6004 IC, with increasing temperature, has an increased frequency output. The voltage regulator's efficiency, however, decreases with increasing temperature. The current through the LED is also a function of temperature. The behavior of this circuit can be heavily dependent on ambient temperature. This is a vital stipulation as, depending on the bandwidth of the MFBP filter designed

before, the LED signal may fall inside the stopband of the MFBP filter. The receiver would then fail to receive the LED signal and the optical uplink would not operate. The summary of the final results can be seen in Table 5.

Table 5: Simulated vs. experimental results

Component Values	Simulated	Experimental
Output Current	200mA	150mA
Output Frequency	20kHz	20.1kHz
Output Duty-cycle	48%	50.1%

The final circuit fell well within specifications and operated correctly after several component alterations.

5 Conclusion

The design, simulation, and implementation of the LED driver have been explained. Lab specification required that the signal generator have a frequency of approximately 20kHz, a duty-cycle of approximately 50%, and an amplitude of at least 100mA. The LED driver takes a sinuisoidal waveform of variable duty-cycle and outputs a 50% durt-cycle square wave. The waveform is then converted to a suffeciently large driving current by the current driver. The LED driver was constructed using the following parts: a 10kΩ, 100kΩ, 470Ω, 1kΩ, 12Ω and a 10kΩ potentiometer; a MCP6004 quadrature operation amplifier; an IR1503 LED; and finally a 2N3904 BJT. A 9V battery supply is stepped down to 5V with an LM7805 voltage regulator. The frequency was 20.1kHz, with a duty-cycle of 50.1%, and an amplitude of 150mA. An important lesson about the behavior circuits including both op amps and transistors was learned. The meshing of op amps and transistors provide novel solutions to real world problems

References

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[2] NPTEL.(2017) Schmitt Trigger [Online]. Available: http://www.nptel.ac.in/courses/117107094/lecturers/lecture_18/lec

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E Voltage Amplifier

Task 5: Voltage Amplifier

Optical Uplink

Joseph Arsenault
Ryan Dufour
Phil Robb

Abstract

The design, simulation and construction of an amplifier circuit are described. In task 5 of the optical uplink project, a voltage amplifier will increase the signal from the active bandpass filter from a low voltage range from 100mV to 5V. Two ways are explored to accomplish this task. The first is using a common source NMOS circuit. The second is using a NPN BJT common emitter circuit. The specifications required, for the purposes of use in the optical uplink project, are a lower cutoff frequency of $\leq$ 1kHz, upper cutoff frequency of 200 kHz, and a peak gain of 21 dB $\pm$ 1 dB. Also, the 2nd Harmonic distortion for a 20 mVp-p sinusoidal signal at 1 kHz must be $<$ 2%. For the purposes of the optical uplink project, the NMOS was chosen instead of the BJT. The lower cutoff frequency for the BJT was greater than 1kHz, while the NMOS had a lower cutoff frequency of approximately 600 Hz. The NMOS circuit output a 22 dB gain and the BJT output 25 dB gain.

Electrical and Computer Engineering
University of Maine
ECE - 342
December 11, 2017

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1 Introduction

This report describes design, implementation and test of two voltage amplifiers. One consisting of negative metal oxide semconducting field effect transistors (NMOS). The other comprised of bipolar junction transistors. Figure 1 demonstrates where in the optical uplink project the voltage amplifier is placed.

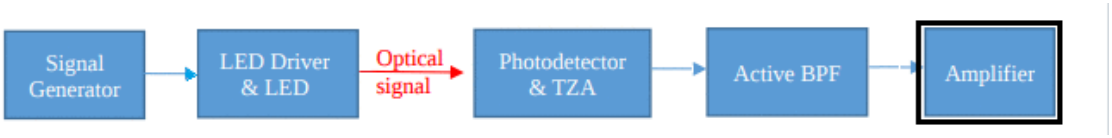

Figure 1: Block diagram for optical uplink [1]

The voltage amplifier is required by the optical uplink project. The output signal from the multi-feedback bandpass filter (MFBP) is in the hundreds of millivolt range. In order to make a more easily detectable signal, a voltage amplifier is required. This can achieved through the use of either a common source or common emitter amplifier. The specifications for this lab are summarized in Table 1.

Table 1: Voltage amplifier specifications

Specifications	Required
Peak gain, with load	21 dB ± 1dB%
Bias current for N_1	1mA
Lower cut-off frequency	≥100 mA
Upper cut-off frequency	at least 200 kHz
R_{in}, small signal	at least 1 MΩ
R_{out}, small signal	at least 3 kΩ
2^{nd} Harmonic distortion @ 1kHz	<2%
Supply voltages	±12 V

The voltage amplifier circuit receives the voltage signal from the MFBP and increases the amplitude of the voltage wavefrom. The desired final output being 5 V. This is achieved with either the use of a NMOS common source amplifier or an NPN BJT common emitter amplifier.

Section 2 of this report describes the design and simulations of the common source amplifier and the common emitter amplifier. Experimental results are addressed in section 3. A discussion of the results, sources of error, and areas of possible improvement are outlined in section 4. Section 5 concludes this report.

2 Circuit Development

This section covers the design choices associated with the various circuits constructed. Both a NMOS common source amplifier and BJT common emitter amplifier. Only the NMOS circuit required design choices as the BJT component values were provided as part of the lab.

The order in which the circuits are discussed is as follows: first the NMOS amplifier followed by the BJT amplifier.

2.1 NMOS common source

The NMOS common source amplifer for this lab was constructed using 2N7000 NMOS transistors. The circuit essentially consists of two parts, the voltage amplifier stage and the current mirror. The generic circuit for the current driver is shown in Figure 2.

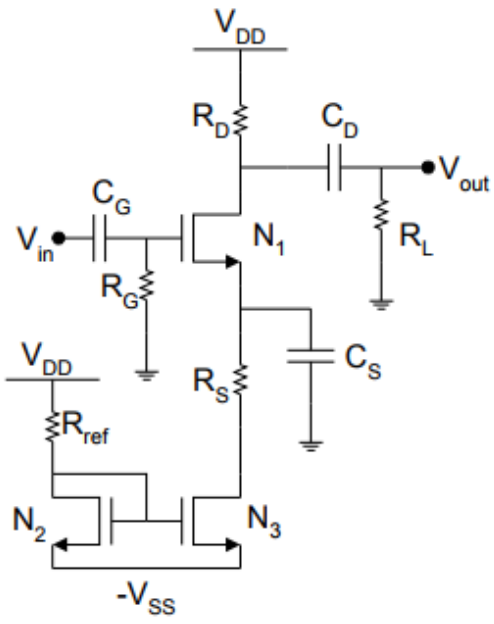

Figure 2: Generic common source amplifier circuit [1]

In order to understand the operation of the circuit, DC analysis of the circuit is required. At DC all the capacitors behave as shorts. It is known that the current through a MOSFET is seen in Equation 1

$$I_D = k(V_{gs} - V_t)^2, \tag{1}$$

Where k is the transconductance parameter, V_{gs} is the gate-source voltage and V_T is the threshold voltage. From the datasheet [2], I_D is 75 mA when V_{gs} is 4.5 V. From Equation 1 k can be found to be 8.5 mA/V. Again using Equation 1, the corresponding V_{gs} for a bias current of 1 mA is found to be 1.85 V. Upon finding the voltage drop over the NMOS, the source resistance can then be found by KCL across the amplifier NMOS. R_s is found to be 8.3 kΩ, R_{ref} can found to be 22.2 kΩ. The capacitor values are chosen such that their impendence is less than their corresponding resistor values. The impendence of the capacitor can be found by Equation 2

$$Z_c = \frac{1}{j\omega C}, \tag{2}$$

where ω is the angular frequency of the input signal in rad/s. By setting Z_c to be less than the corresponding R values, C can be solved to be 4.7 μF.

AC analysis of the circuit is then required in order to find the drain resistance. Figure 3 shows the equivalent small signal model for the NMOS.

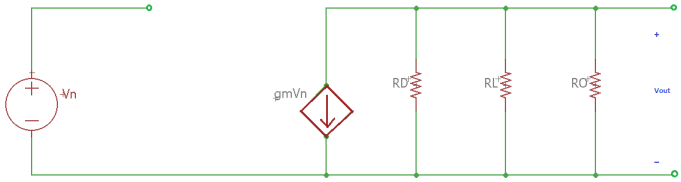

Figure 3: Equivalent small signal circuit

The transconductance of this circuit is defined as Equation 3

$$g_m = \frac{2I_D}{V_{ov}}, \tag{3}$$

where V_{ov} is the overdrive voltage. From this small signal transconductance is found to be 2.8 mA. The small signal r_0, defined as Equation 4

$$r_o = \frac{1}{\lambda I_{DS}}, \tag{4}$$

where λ is the body effect, and found from the datasheet [2] to be zero for the operating conditions. The open circuit gain can then be found by Equation 5

$$\frac{v_o}{v_{in}} = g_m R_o, \tag{5}$$

where R_o is the equivalent resistance of (R_D || R_L). The load resistance is provided by the lab, but for this calculation can be assumed to nearly infinite, therefore R_D is found to be around 2 kΩ. The circuit was then simulated in NGSpice integrated with Matlab. The simulated circuit can be seen in Figure 4.

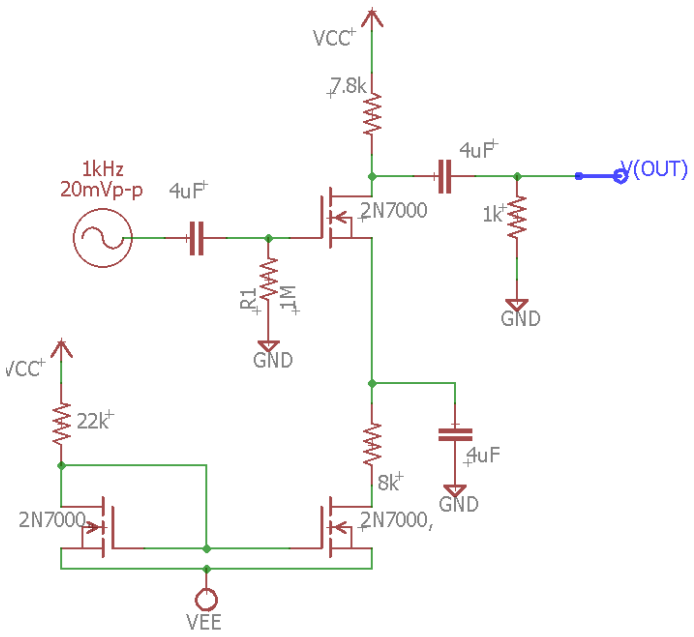

Figure 4: Simulated common source amplifier circuit

A significant change was required in order to meet specs, the R_D value calculated was off by a factor of 4. This is due to assumptions made during analysis for the solution of the transconductance amplifier. The final R_D was found by to be 7.8 kΩ more detail is provided in discussion. In addition, the negative bias voltage was altered to -8 V in order to reduce harmonic distortion. The frequency of the NMOS is shown in Figure 5.

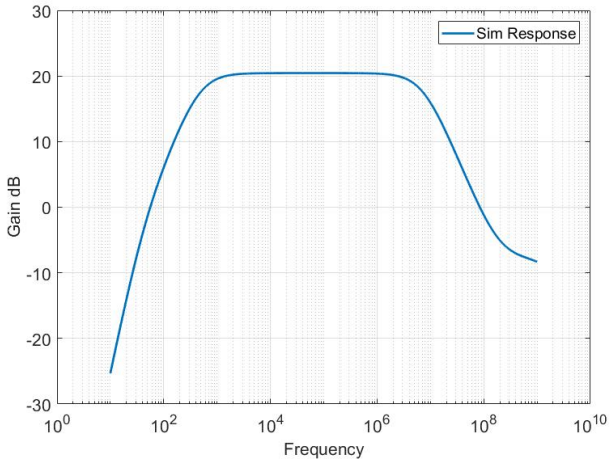

Figure 5: Simulated frequency response of NMOS amplifier

The NMOS met the specified gain at 21 dB with a 3dB lower cut off frequency well below the required 1 kHz. The FFT of NMOS can be seen in Figure 6.

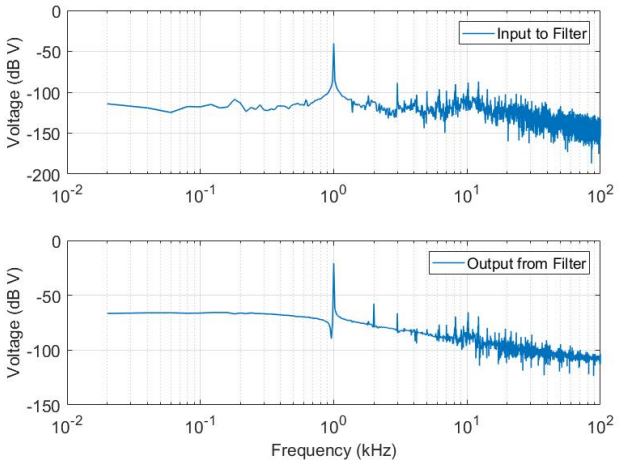

Figure 6: Simulated FFT of second harmonic distortion

This analysis was performed by inputting a 10 mV signal at 1 kHz. The measured distortion on the second harmonic is required to be less than 2%. By inspection the distortion is found to be 1.5%. Table 2 summarizes the NMOS simulation results.

Table 2: NMOS summary

Q_1, Q_2, Q_3	2N7000
R_ref	19.3 kΩ
R_D	7.8 kΩ
R_S	8 kΩ
R_G	1 MΩ
C_g, C_d, C_l	4.7 μF
Lower cutoff	500 Hz
Upper cutoff	10 MHz

After making slight alterations the circuit worked correctly in simulations.

2.2 BJT common emitter

The BJT operates similarly to the NMOS circuit. The difference being it is now an NPN transistor and is therefore a current controlled voltage source, as opposed to the NMOS which is a voltage controlled. The values for the BJT circuit were not solved for, but instead provided as part of the lab, which can be seen in Table 3

Table 3: BJT experimental values

Q_1, Q_2, Q_3	2N3904
R_ref	19.3kΩ
R_C	4.7kΩ
R_B	10kΩ
R_E	3.3kΩ
R_L	1kΩ
C_B, C_C, C_E	500nF
Gain	30db
Lower cutoff	3 kHz
Upper cutoff	100 MHz

The simulated circuit is shown in Figure 7.

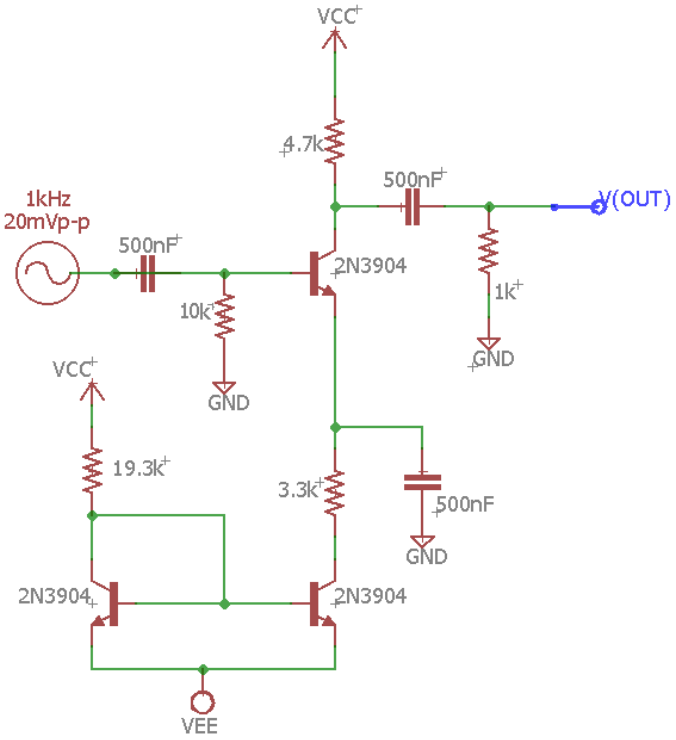

Figure 7: Simulated circuit of BJT

The simulations of the BJT follow and were performed in Matlab integrated with NGspice. The frequency response of the circuit can be seen in Figure 8.

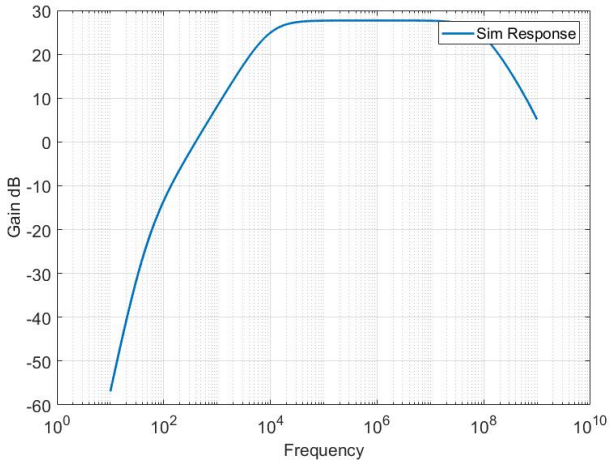

Figure 8: Simulated frequency response of BJT

Notably, the 3dB lower cutoff is greater than 1 kHz. The corresponding passband gain is significantly higher than 20 dB. This is not ideal, because the output could begin to saturate due to excessive gain. The FFT of the BJT can be seen in Figure 9

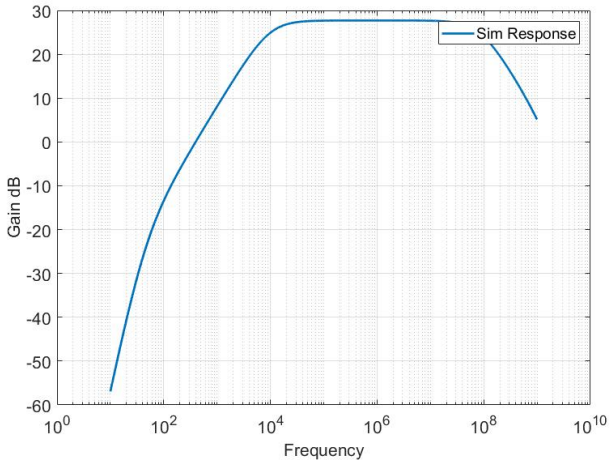

Figure 9: Simulated FFT BJT circuit

The BJT achieved a far smaller second harmonic distortion than the NMOS, with only a .25% distortion for the 2 kHz harmonic.

3 Experimental Implementation

The circuits required only minor changes from simulation to experimental implementation.

3.1 NMOS amplifier

The final circuit is shown in Figure 10.

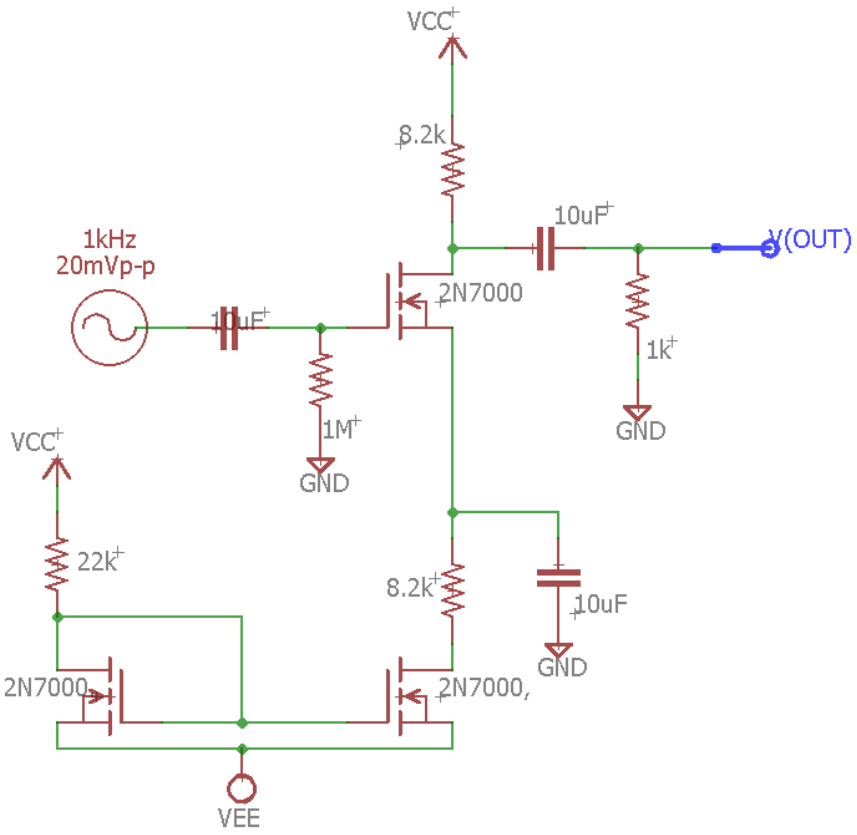

Figure 10: NMOS final circuit schematic

Some of the resistor values had to be changed in order to meet specifications. The capacitors had to be increased as well due to the poor performance of the equivalent nominal value electrolytics. The implemented capacitors are parallel plate which operate better at higher frequencies. Figure 11 demonstrates the experimental frequency response of the NMOS amplifier.

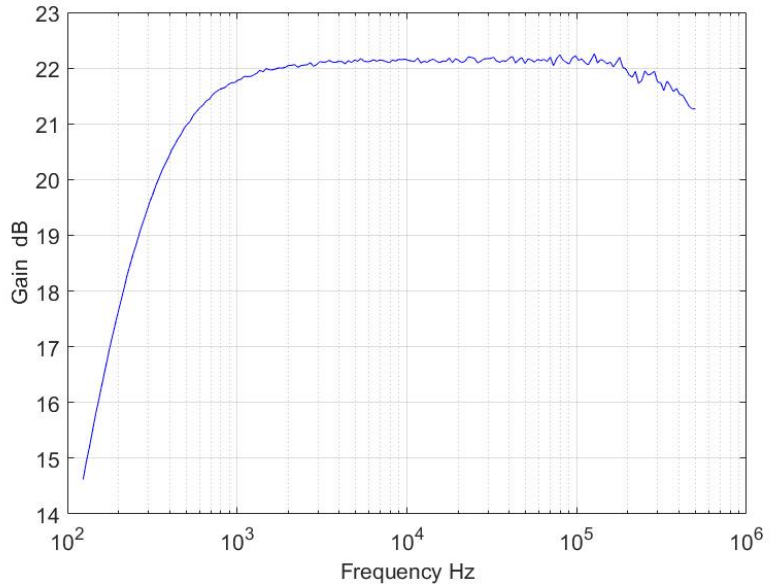

Figure 11: NMOS experimental frequency response

The gain was just on the high end of the specification at 22 dB. The lower cutoff frequency is less than 1 kHz. The upper cutoff also meets spec by being greater than 200 kHz. The FFT of the circuit can by seen in Figure 12.

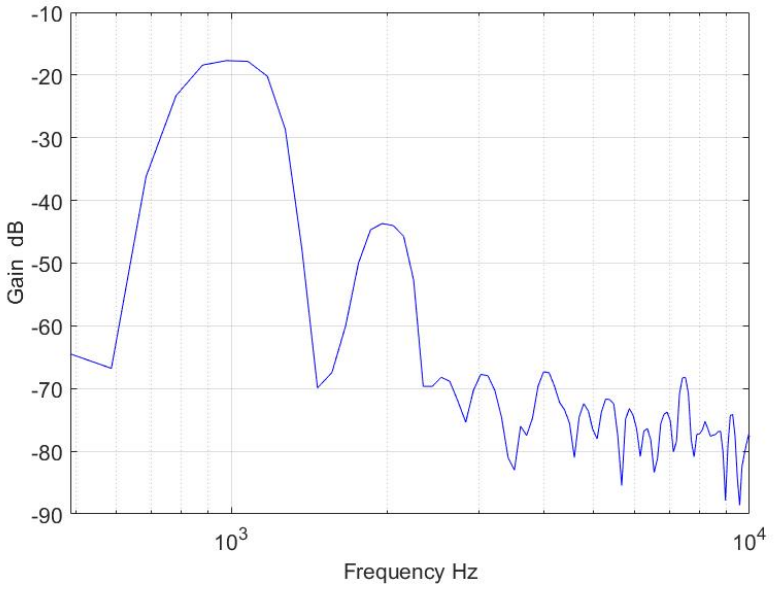

Figure 12: NMOS experimental FFT

The second harmonic distortion was slightly too high at 5%. This can be altered by the negative bias volt-

age, for the purpose of this lab, 5% was deemed acceptable. Table 4 shows the summary of the experimental NMOS circuit.

Table 4: NMOS experimental values

Q_1, Q_2, Q_3	2N7000
R_ref	22 kΩ
R_g	1 MΩ
R_d	8.2 kΩ
R_s	8.2 kΩ
R_L	1kΩ
C_B, C_C, C_E	10 μF
Gain	21 dB
Lower cutoff	600 Hz
Upper cutoff	10 MHz

After minor alterations the circuit operated correctly.

3.2 BJT amplifier

The BJT required only a slight change of capacitor values, due to availability. Figure 13 shows the final circuit for the BJT amplifier circuit.

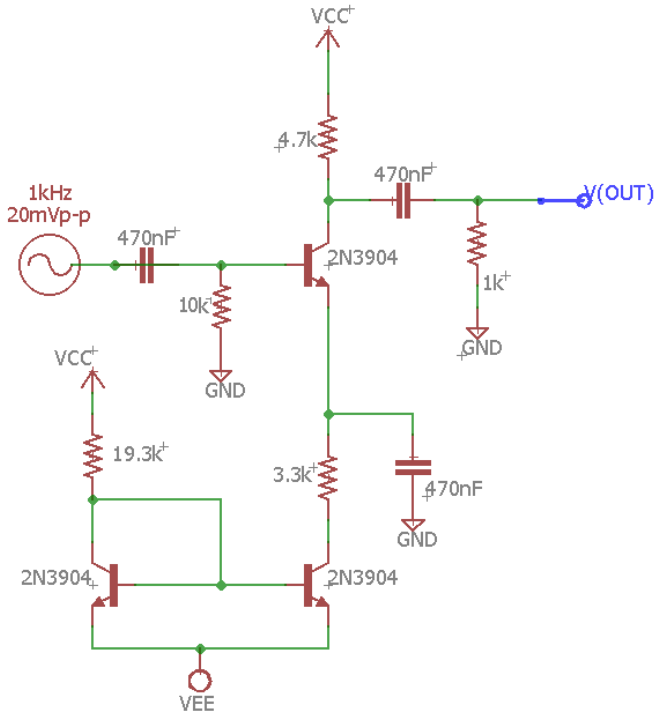

Figure 13: BJT final schematic

The BJT was built using the provided components. The experimental frequency response of the circuit is shown in Figure 14.

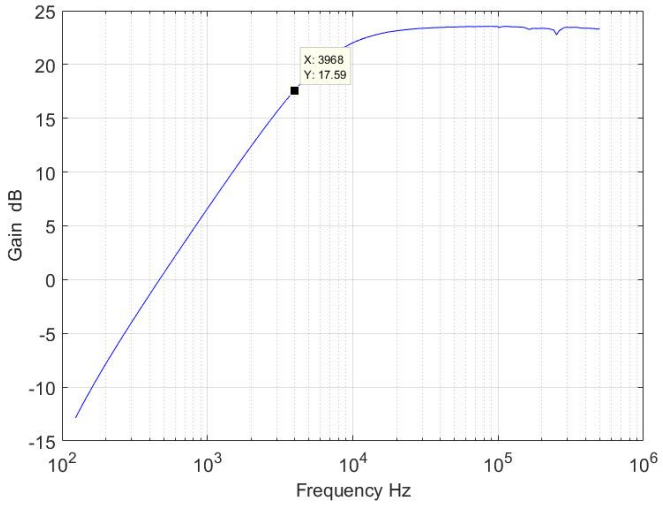

Figure 14: BJT experimental frequency response

The gain was a little less than the simulated, at 24 dB, but the lower cutoff was quite higher at 6 kHz, far higher than the specified 1 kHz. The upper cutoff can not be measured exactly due to the limitations of the Digilent Discovery board's network analyzer. The measured values are only accurate up to 500 kHz. The measured FFT of the BJT can be seen in Figure 15.

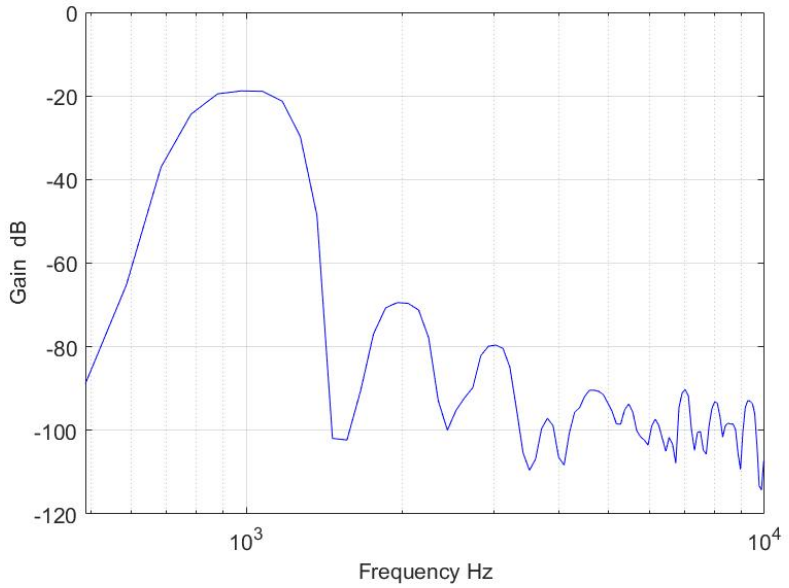

Figure 15: BJT experimental FFT

The second harmonic distortion was significantly less than the NMOS while still being in spec, at roughly 1%. Table 5 shows the summary of the BJT performance.

Table 5: BJT experimental values

Q_1, Q_2, Q_3	2N3904
R_ref	19.3kΩ
R_C	4.7kΩ
R_B	10kΩ
R_E	3.3kΩ
R_L	1kΩ
C_B, C_C, C_E	470nF
Gain	25 dB
Lower cutoff	6 kHz
Upper cutoff	>500 kHz

Overall, the BJT operated as expected, discussion and comparison of the two circuits can be found in Discussion.

4 Discussion

After several minor changes, both circuits operated correctly. This lab served as introduction to the main differences between MOSFET and BJT devices. The two components are both transistors but have defining differences, mainly the polarity of the devices. The specifications are outlined in Table 6.

Table 6: BJT and NMOS comparison

BJT	Values	NMOS	Values
Q_1, Q_2, Q_3	2N3904	N_1, N_2, N_3	2N7000
R_ref	19.3kΩ	R_Ref	22kΩ
R_C	4.7kΩ	R_D	8.2kΩ
R_B	10kΩ	R_G	1MΩ
R_E	3.3kΩ	R_S	8.2kΩ
R_L	1kΩ	R_L	1kΩ
C_B, C_C, C_E	470nF	C_G, C_S, C_D	10μF
Gain	25 dB	Gain	22 dB

Notably, different voltages than those specified in the lab manual were used as the Analog Discovery handles small voltage signals very poorly, producing a lot of noise. Other than this both circuits had little issue performing as expected.

The BJT, while having a larger gain and much less 2nd harmonic distortion, did not have the required cutoff frequency to meet the specification for the optical link project, thus the NMOS CS amplifier was chosen for it's ability to meet specification.

One of the biggest challenges of this lab was the mathematical assumptions and operations used to solve for the transistor values in simulation. When dealing with such devices the assumptions used can some-

times give wildly incorrect values and lead to repetition of calculations until correct. Fortunately simulations help greatly with reducing the time it takes to get to the correct solution.

The final circuits fell well within specifications and operated correctly after minor component alterations.

5 Conclusion

The design, simulation, and implementation of a voltage amplifier have been explained. The specifications required, for the purposes of use in the optical uplink project, are a lower cutoff frequency of $\leq$ 1kHz, upper cutoff frequency of 200 kHz, and a peak gain of 21 dB $\pm$ 1 dB. Also, the 2nd Harmonic distortion for a 20 mVp-p sinusoidal signal at 1 kHz must be $< 2\%$. The sinusoidal source was 20 mV_{P-P} at 1kHz, and the supply voltages were $\pm$ 12V. This resulted in a lower cutoff frequency of approximately 600 Hz and the upper cutoff frequency was in the MHz range, which exceeds the required $\geq$ 200 kHz. The 2nd harmonic distortion was measured to be approximately 5%. An important lesson was learned about the comparison between a voltage amplifier using NMOS components and a voltage amplifier using BJT components.

References

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[2] ON Semiconductor. (2017) 2N7000 [Online]. Available: http://www.onsemi.com/PowerSolutions/supportDoc.do?type=models&rpn=2N7000