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Task 4: LED Driver

Optical Uplink

Joseph Arsenault
Ryan Dufour
Phil Robb

Abstract

The design, simulation, and construction of an LED driver circuit are described. In task 4 of the optical uplink project, a signal conditioning circuit and current driver are explored. A signal conditioner using the MCP6004 operational amplifier as a Schmitt trigger was built in order to output a square wave with 50% duty-cycle. The current driver was constructed using a MCP6004 operational amplifier to create a transconductance amplifier that takes the output from the conditioner and converts it to a current signal. The output of LED driver was required to operated at approximately 20 kHz, 50% duty-cycle, with a current of 100mA amplitude. a sinusoidal wave form, at a frequency of 20.1 kHz, a duty cycle of 50.1% and 150mA peak amplitude.

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1 Introduction

This report describes the design, implementation and test of an LED driver.

This report describes the design, implementation and test of a signal generator using various NMOS and CMOS inverter designs. Two different signal generators were designed, an astable multivibrator and a ring oscillator. Notably, negative metal oxide semiconducting field effect transistors (NMOS), complementary metal oxide semiconducting field effect transistors (CMOS), and finally the conjunction of the two to form an AND logic gate. Figure 1 demonstrates where in the optical uplink project the signal generator is placed. The signal generator creates the waveform that drives the LED that is detected by the photodetector.

Figure 1: Block diagram for optical uplink [1]

The output from the the signal generator is not a square wave, nor does it output enough current to drive the LED. The current driver will be created in a subsequent lab. The voltage transfer characteristics (VTC) of an ideal inverter is shown in Figure **??**.

Figure **??** describes the ideal VTC of an inverter, where the voltages for logic low and logic high are shown. Both the ring oscillator and the astable multivibrator are created by cascading several CMOS inverters together,

Section 2 of this report describes the design, and when relevant, the simulations of the NMOS, CMOS inverter, the AND gate, the ring oscillator, and finally the astable multivibrator. Experimental results are addressed in section 3. A discussion of the results, sources of error, and areas of possible improvement are outlined in section 4. Section 5 concludes this report.

2 Circuit Development

This section covers the design choices associated with the various circuits constructed. A common trait among all of the designs included is the use of MOSFETS. MOSFETS are silicon based components that take advantage of the semiconducting properties of silicon in order to behave as a switch. The ability for a MOSFET to transition from "open" to "closed" is the foundation for digital circuits. In digital circuits, voltages are not represented as analog continuous signals, but instead as discrete binary values, where 1 represents logic high and 0 represents logic low. One of the properties investigated in this report is the real electrical characteristics of these digital logic circuits. These circuits do not behave ideally and the real switching time of the circuits can lead to problems during circuit implementation.

The order in which the circuits are discussed is as follows: first, the resistively loaded NMOS, followed by the CMOS inverter, then the CMOS logic gate and finally the ring oscillator and the astable multivibrator.

2.1 Ring Oscillator

The design of the CMOS ring oscillator consists of three CMOS inverters connected in series with the output of the last inverter connected to the input of the first inverter. The ring oscillator will also have a capacitor at each output connected to ground. The schematic for the CMOS ring oscillator can be seen in Figure 2.

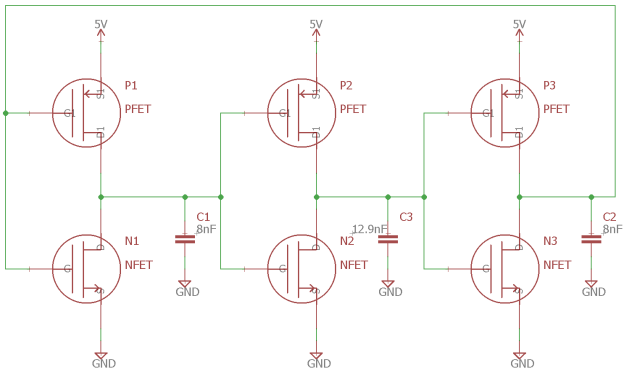

Figure 2: CMOS ring oscillator schematic

The operation of the ring oscillator uses a series of inverters. The output of one inverter inverts the input signal. Therefore, if there are a series of inverters, then each odd inverter will have the same inverted output as the first. In this instance, there are three stages of inverters used, with the output of the third inverter being fed back into the input of the first inverter. This feedback from the output to the input causes an oscillation. The simulated output of the ring oscillator is depicted in Figure 3.

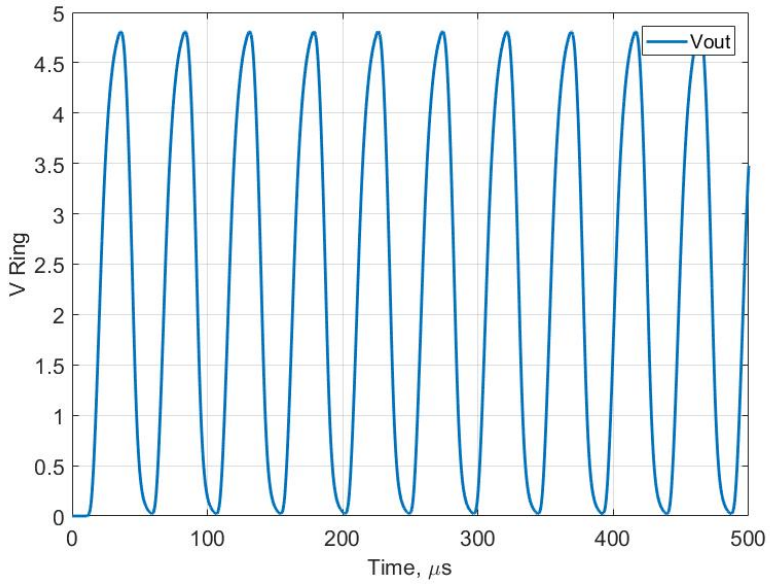

Figure 3: Simulated CMOS ring oscillator output

The ring oscillator circuit requires only a DC power source with a threshold voltage above what is required of the MOSFETS, and the oscillations will occur. To increase the frequency, the DC supply can be increased, causing an increase in current as well as frequency.

2.2 Signal Conditioner

2.3 Current Driver

The current driver for this lab was created using an MCP6004 op amp. The op amp is to act as the driver for the gate of a 2N3904 Bipolar Junction Transistor (BJT). The generic circuit for the signal conditioner is shown in Figure 2.

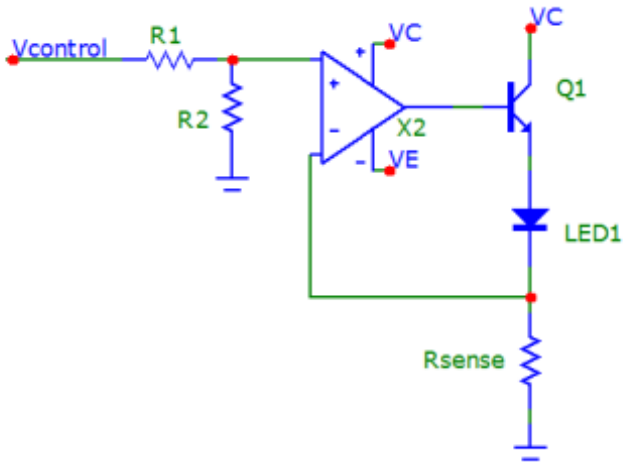

Figure 4: Generic current driver circuit [2]

The key to operation of the current driver is the BJT transistor. A BJT transistor, in contrast with the metal oxide semiconducting field effect transistor (MOSFET), is capable of

2.4 Voltage Regulator

The IC buck converter replaces the entire circuit designed above and replaces it with an IC package. The filter, however still needed to be built around the load. The load used a potentiometer tied to the feedback pin of the IC to enable a variable voltage on the load. Certain limitations of the IC needed to be considered when designing the circuit. A block diagram of a typical Buck converter using this IC is provided below.

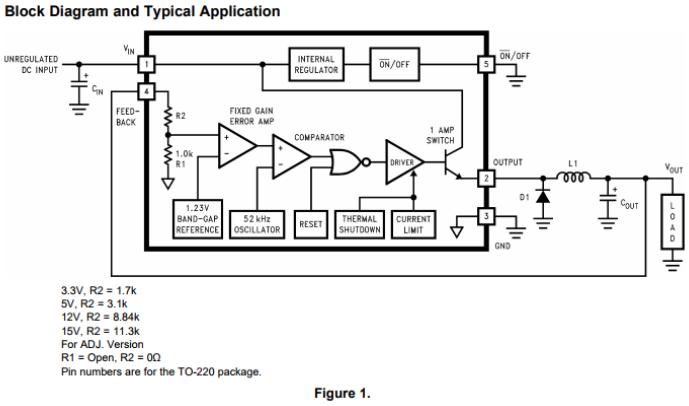

Figure 5: IC Buck converter block diagram [5]

The block diagram above shows the inside of the IC used in designing the final Buck Converter.

3 Experimental Implementation

3.1 Ring Oscillator

3.2 Signal Conditioner

3.3 Current Driver

Needs a donkey kicking

4 Discussion

This lab served as introduction to MOSFETS and implementation of digital logic. When using transistors to create digital devices, it is often assumed that the device behaves ideally. When the device is logic high, it is one voltage, and when it is logic low it is another. Based on this logic, it is assumed that the switching on and off of the MOSFETS happen instantaneously. Based on the results of the ring oscillator and other inverter circuits, the MOSFETS do not switch instantaneously. Instead, power is consumed by the MOSFETS when they transition from one state to another. This consumption of power causes a small time delay. Each of the circuits described in this report are discussed in the following subsections, excluding the astable multivibrator. The astable multivibrator was not constructed during the experimental phase of this task.

4.1 NMOS inverter

The NMOS inverter worked as simulated and required no significant design changes in order to function. The measured power consumption was different from the simulated values, but it operated within a tighter band of values. The comparison of the NMOS with simulations is shown in Figure 1.

Table 1: Comparison of NMOS

Component Values	Simulated	Experimental
R	4.4kΩ	4.3kΩ
Max Power	31.2mW	5.8mW
Min Power	69.5pW	37μW
Rise Time	199ns	11μs
Fall Time	195ns	1.22μs

The rise and fall times were significantly greater as well. This can be accounted for by the fact the implemented circuit, in addition to board parasitic capacitance, also had capacitance from the jumpers connecting the pins of the device. Each jumper added capacitance to the circuit, which in turn increased the time constant for the circuit, which would account for the increased transition times.

4.2 CMOS inverter

The CMOS inverter required no changes from simulation. The circuit behaved as expected, with the VTC matching that of the simulations. One of the strengths of the CMOS is the faster transition between logic states. This is reflected in the slope of the experimental VTC. The CMOS also represents logic low with zero volts, as opposed to the NMOS were logic low was still some positive voltage. The DC power consumption of the CMOS was also negligible compared to that of the NMOS. Table 2 shows the differences between the simulated and measured CMOS circuit.

Table 2: CMOS inverter comparison

Component Values	Simulated	Experimental
Rise Time	142ns	235ns
Fall Time	114ns	177ns
Power	0	5μW

The experimental results for the CMOS inverter are shown in Table 2.

4.3 AND gate

The AND gate operated as expected. This lab served as an introduction to the use of transistors as logic devices. The use of binary logic is fundamental in the design of digital logic. The construction of a physical AND gate demonstrates the real device characteristics of logic circuits. The truth table for the constructed AND gate is shown in Table 3.

Table 3: Truth Table: AND

Inputs		Output
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

4.4 Ring oscillator

The ring oscillator circuit designed with the CMOS did not initially meet the specifications required in the lab. The simulations were accurate, but real-world parasitic capacitances from the board and jumper wires impacted the circuit. To remedy the situation, a capacitor of 4.7 nF was added in parallel after the second inverting gate. By increasing the capacitance, we lowered the frequency from 22.8 kHz to 19.8 kHz. The comparison between the simulated results and experimental is expressed in Table 4

Table 4: Comparison of ring oscillator results

Component Values	Simulated	Experimental
C_1	8nF	8.2nF
C_2	8nF	13.9nF
C_3	8nF	8.2nF
Frequency	20.1kHz	19.8kHz
Amplitude	5V	4.9V

The reason this oscillator is chosen over the astable multivibrator as the signal generator is mostly arbitrary and simply design choice for the optical uplink project [4]. Although one of the benefits of the ring oscillator is that from the sensitivity testing it is less affected by component tolerances than the astable multivibrator. This is significant since the capacitors available for circuit construction are 10% tolerances.

5 Conclusion

The design, simulation, and implementation of the ring oscillator signal generator have been explained. NMOS inverters, CMOS inverters, and logic gates were also investigated. Lab specification required that the signal generator have a frequency of approximately 20kHz, a duty-cycle of approximately 50%, and an amplitude of 5V. The signal generator takes an input DC voltage and creates an sinusoidal waveform at the output. The signal generator circuit was constructed using the following parts: three 8.2nF capacitors, a 4.7nF capacitor; and finally a CD4007 CMOS integrated circuit with 5V supply voltages. The frequency was 19.8kHz, with a duty-cycle of 51%, and an amplitude of 4.9V. An important lesson about the behavior real logic circuits was learned. Real digital circuits have measurable electrical characteristics and do not behave ideally.

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