Task 3: MOSFET Based Logic Gates and Digital Oscillator

Optical Uplink

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Abstract

The design, simulation, and construction of a signal generator using MOSFET based logic gates are described. In task 3 of the optical uplink project, several inverting circuits are explored using NMOS and CMOS MOSFETS. An inverter based ring oscillator was simulated and constructed using the CD4007 CMOS integrated circuit. Simulations were also conducted using various configurations of NMOS and PMOS inverters, which are described in this report. The ring oscillator was chosen to be the signal generator for the optical uplink project. The required output of the CMOS ring oscillator for the use in the optical uplink project are a frequency of 20kHz, a 50% duty-cycle, and a $5V_{pp}$ amplitude. The final design featured a sinusoidal wave form, at a frequency of 19.8kHz, a duty cycle of 51% and $4.9V_{pp}$ amplitude. .

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Contents

List of Figures

List of Tables

1 Introduction

This report describes the design, implementation and test of a signal generator using various NMOS and CMOS inverter designs. Two different signal generators were designed, an astable multivibrator and a ring oscillator. Notably, negative metal oxide semiconducting field effect transistors (NMOS), complementary metal oxide semiconducting field effect transistors (CMOS), and finally the conjunction of the two to form an AND logic gate. Figure 1 demonstrates where in the optical uplink project the signal generator is placed. The signal generator creates the waveform that drives the LED that is detected by the photodetector.

Figure 1: Block diagram for optical uplink [1]

The output from the the signal generator is not a square wave, nor does it output enough current to drive the LED. The current driver will be created in a subsequent lab. The voltage transfer characteristics (VTC) of an ideal inverter is shown in Figure 2.

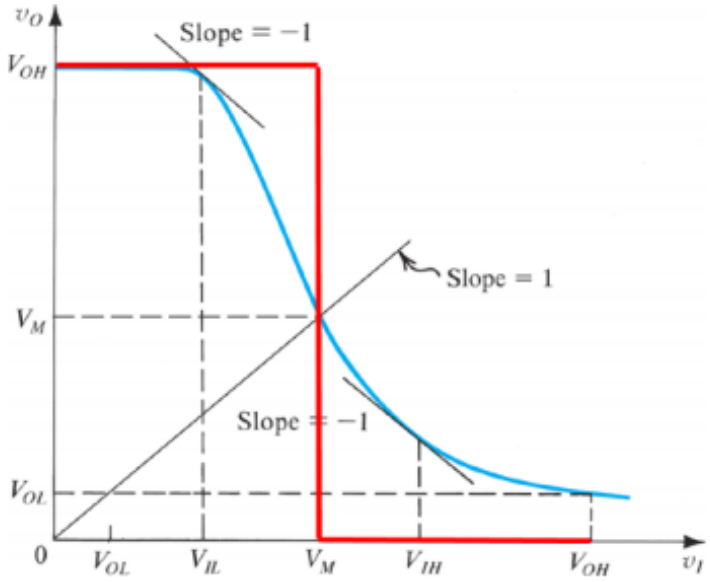

Figure 2: Ideal VTC of inverters [1]

Figure 2 describes the ideal VTC of an inverter, where the voltages for logic low and logic high are shown. Both the ring oscillator and the astable multivibrator are created by cascading several CMOS inverters together,

Section 2 of this report describes the design, and when relevant, the simulations of the NMOS, CMOS inverter, the AND gate, the ring oscillator, and finally the astable multivibrator. Experimental results are addressed in section 3. A discussion of the results, sources of error, and areas of possible improvement are outlined in section 4. Section 5 concludes this report.

2 Circuit Development

This section covers the design choices associated with the various circuits constructed. A common trait among all of the designs included is the use of MOSFETS. MOSFETS are silicon based components that take advantage of the semiconducting properties of silicon in order to behave as a switch. The ability for a MOSFET to transition from "open" to "closed" is the foundation for digital circuits. In digital circuits, voltages are not represented as analog continuous signals, but instead as discrete binary values, where 1 represents logic high and 0 represents logic low. One of the properties investigated in this report is the real electrical characteristics of these digital logic circuits. These circuits do not behave ideally and the real switching time of the circuits can lead to problems during circuit implementation.

The order in which the circuits are discussed is as follows: first, the resistively loaded NMOS, followed by the CMOS inverter, then the CMOS logic gate and finally the ring oscillator and the astable multivibrator.

2.1 NMOS inverter

The first inverter designed was the resistively loaded NMOS transitor. This designed features only one NMOS transistor in series with a resistor. The source is supplied some voltage and driven with a PWM source. The analysis of the NMOS circuit stems from two extreme cases: 1) the input V_{gate} is 0V and the voltage at the drain, $V_{drain} = V_{DD}$ and 2) input $V_{gate} = V_{DD}$ and output V_{drain}=0V. Case 1) describes the state in which no current is flowing through the MOSFET and the it is operating in cut-off. Case 2) described the state in which the transistor is operating in the triode region. The current through the MOSFET is described by Equation 1

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2], \tag{1}$$

where the drain current is found to be equal the hole mobility μ_n, the capacitance between the oxide terminals, the ratio of the width to the length of the channel, and V_t is the threshold voltage.

The design for resistively loaded followed by solving for an arbitrary input. For the purpose of this lab we are interested in V_{out}=2.5 when V_in=2.5 [2]. From these assumptions, it follows that $V_{GS} > V_t$ so the MOSFET is on, but somewhere in the triode to saturation range. It is known from $V_{DS} > V_{GS}$ that the MOSFET is in fact in saturation. Equation 1 simplifies to Equation 2

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_t)^2], \tag{2}$$

where the drain current now only depends on the gate voltage and the threshold voltage. For the CD4007, the k' parameter, seen in Equation 3

$$k' = \mu_n C_{ox} \frac{W}{L}, \tag{3}$$

where k' is equal to approximately $500\frac{\mu A}{V^2}$. From this current the load resistance can be found by application of Ohm's Law, which results in 4.4kΩ. The circuit was simulated using NGspice integrated with Matlab. The simulated circuit is shown in Figure 3.

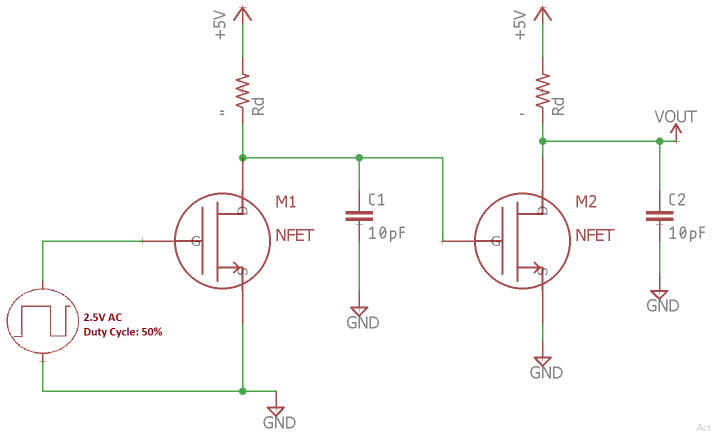

Figure 3: Simulated NMOS inverter

The parasitic capacitance of the breadboard was approximated by the inclusion of the 10pF capacitors at the outputs of the inverters. Figure 4 demonstrates the output voltage as a function of the load resistance. The output voltage was measured while performing a sweep of resistor values.

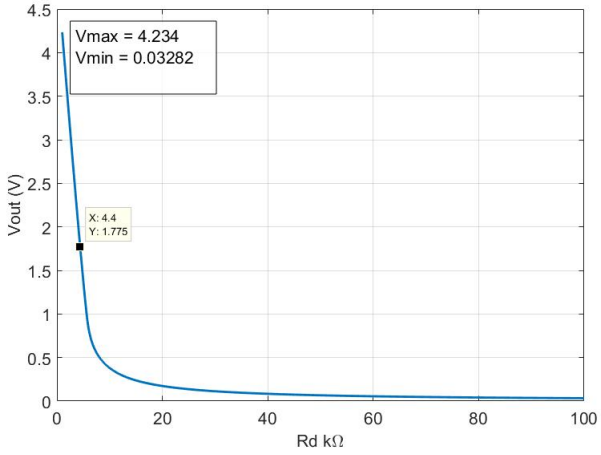

Figure 4: Simulated NMOS Vout vs R

The position of the calculated resistance in Figure 4 demonstrates the simulated output voltage at a 4.4kΩ value. Notably, the upper threshold of effective resistor values is around 9kΩ. The VTC of the NMOS inverter is shown in Figure 5 for three resistor values.

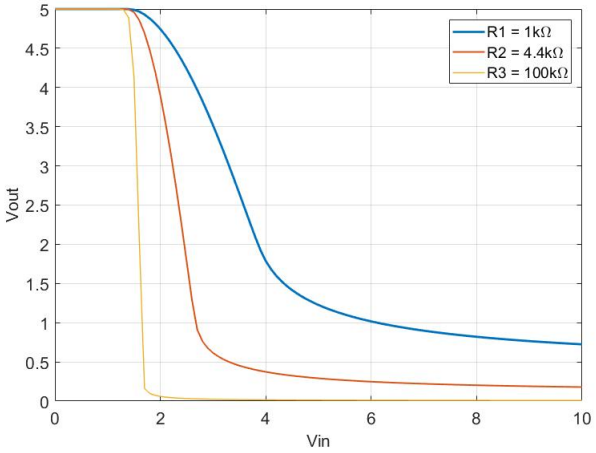

Figure 5: Simulated VTC of single NMOS inverter

The 100kΩ resistor features the most abrupt transition between logic states. The voltage at which it transitions, however, is below the supplied V_{in} of 2.5V, meaning this gate would subsequently change states at incorrect voltages. The 4.4kΩ resistor produces a transition at the voltage 2.5V, as calculated.

The transient analysis of the NMOS inverter was performed in NGSpice in conjunction with MATLAB. The time-domain graph of the inverter with a resistance of 1kΩ is shown in Figure 6.

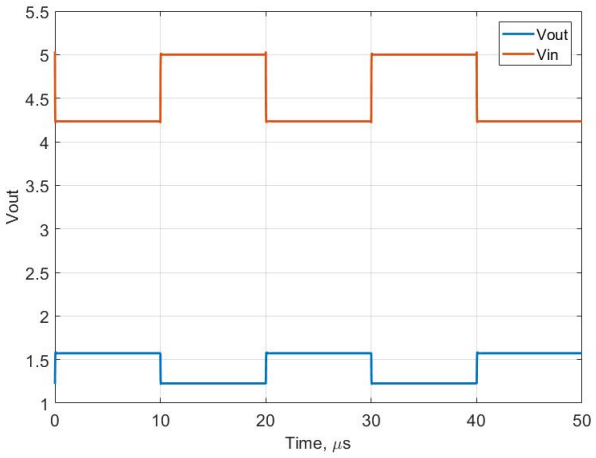

Figure 6: Simulated transient with 1k resistor

The output voltage is far below that of the input voltage in 6. The output waveform had a rise time of 129ns and a fall time of 122ns. The output waveform can then be contrasted with the output voltage calculated using a 4.4kΩ resistor seen in Figure 7.

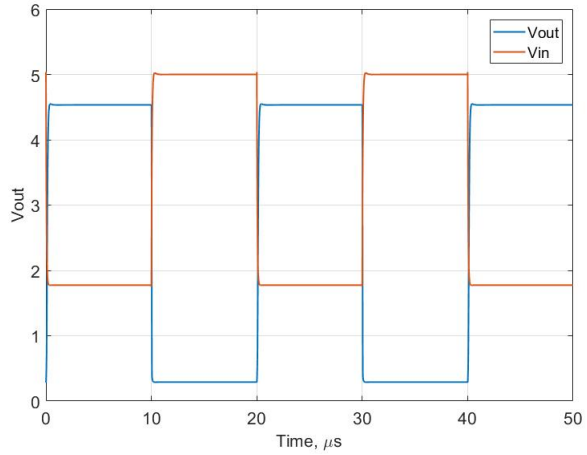

Figure 7: Simulated transient with 4.4k resistor

The output voltage, as seen in Figure 7, now outputs a voltage that is very nearly the supply voltage. The rise time was found to be 1.15 μs and the fall time was 133ns. The time-domain voltages for the 100kΩ resistor was also found, as shown in Figure 8.

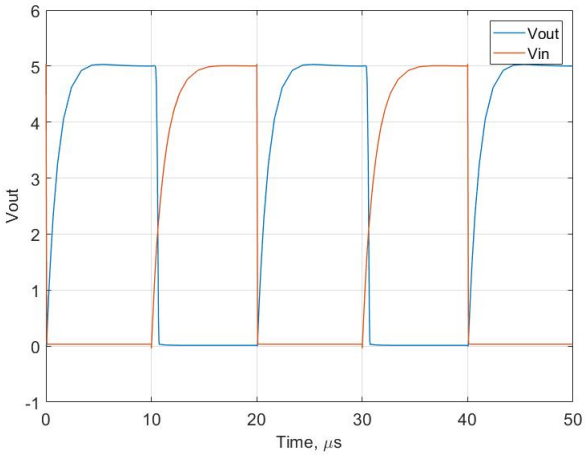

Figure 8: Simulated transient with 100k resistor

The introduction of the 100kΩ resistor dramatically increased the rise time of the output waveform. The rise time was found to be 12.1μs with a fall time of 1.19μs. The larger resistance increased the time constant of the equivalent RC circuit from the resistor and parasitic capacitance. The supply voltage was also increased in order to determine the effect on the inverter. Figure 9 shows the output voltage with a 10V supply and the 4.4kΩ resistor.

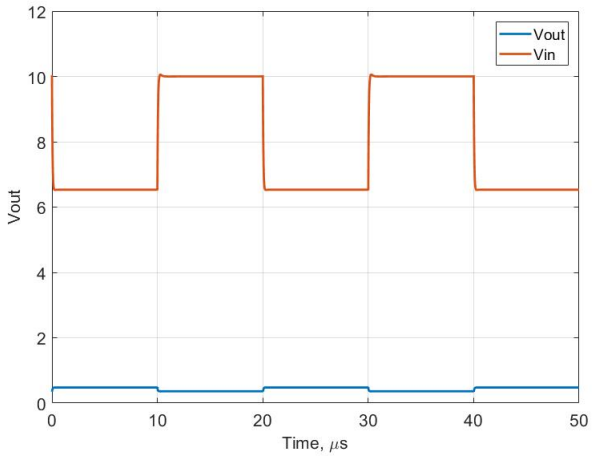

Figure 9: Simulated transient with 4.4k resistor and 10V supply

The output voltage decreases with the supply voltage, which agrees with Equation 2. The rise time was then found to be 1.11μs with a fall time of 185ns. The disparity between the supply voltage and the output voltage is seen when the supply is increased to 15V, as show in Figure 10.

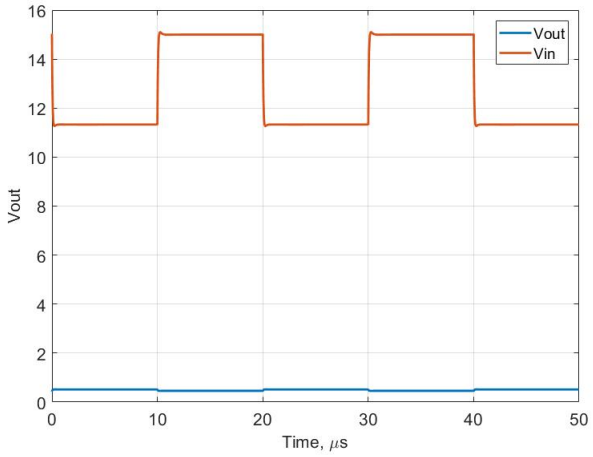

Figure 10: Simulated transient with 4.4k resistor and 15V supply

The rise and fall times were found to be 199ns and 195ns respectively. The supply voltage did not play a significant role in rise or fall times, but did dramatically alter the output voltage. Table 1 shows the simulated results for the NMOS inverter.

Table 1: NMOS simulated results

Values	Results
R	4.4kΩ
Min Power	69.5pW
Max Power	31.2mW
V_{max}	4.23V
V_{min}	32.8mV
Rise Time	129ns
Fall Time	122ns

The simulated results were in line with the theoretical values, the inverters operated as expected.

2.2 CMOS inverter

The CD4007UBE integrated circuit will be modeled using NGSpice in conjunction with MATLAB for this purposes of the simulations for the signal generator. In Figure 11, the pin connections for the IC as well as the internal design of the NMOS and PMOS MOSFETS connections.

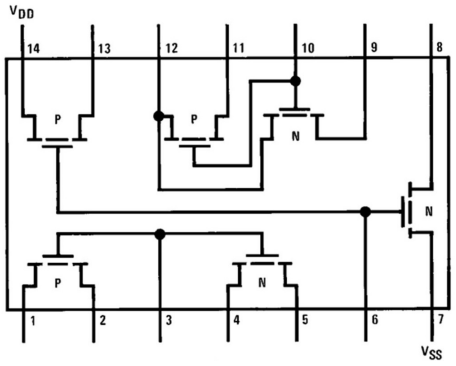

Figure 11: CD4007UBE internal schematic

There are two circuits that will be simulated. The first simulation is a CMOS inverter. The second simulated circuit will be a CMOS ring oscillator. Each of these simulations will be based on the design of the CD4007UBE IC. The CD4007UBE has three NMOS and PMOS transistors connected in pairs. The first two pairs have their gates connected to each other while the third pair have their gates and drains connected together. The third pair is best for implementing a single inverter due to it's connections.

2.2.1 CMOS inverter

The design of the CMOS inverter will consist of a pair of MOSFETS, one being a PMOS and one being an NMOS connected in series between V_{DD} and the reference, GND. The simulation schematic is shown in Figure 12 below.

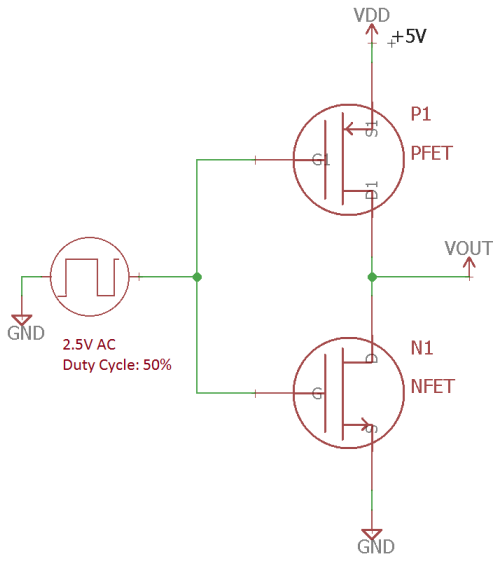

Figure 12: CMOS inverter schematic

Based on the characteristics of the CMOS inverter circuit, which contains a PMOS and NMOS, a load-line plot can be drawn representing the voltage transfer function characteristics, VTC. This graphical interpretation is shown below in Figure 13.

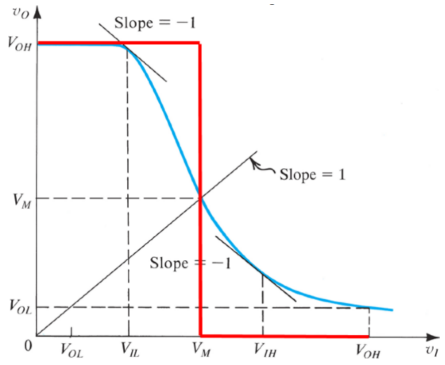

Figure 13: Voltage transfer function characteristics

In the first region of the VTC inverter graph, between 0 and before V_{IL}, known as the input voltage at the low logic state, the PMOS device is on. This is due to a low voltage being applied to it. The NMOS is essentially a large resistor because it has no use of free electrons, which disallows conduction. As a result, there is no current flowing through the inverter, so the output voltage is equivalent to supply voltage, V_{DD}, because there is no voltage drop across the PMOS. Once the voltage reaches V_{IL}, the NMOS is already on and saturated because of a large V_{DS} value.

At V_{IL}, the slope of the VTC is -1, which is the maximum input voltage in this state. Afterwards, there is a point in the VTC at V_M where $V_I = V_O$. This is the gate threshold voltage. At this time, the voltage dropped across the PMOS and NMOS are the same, and are both in a saturated state. In the area after the point V_M, the NMOS is conducting linearly, and the PMOS is being driven to saturation. The minimum voltage input at the high logic state occurs at V_{IH}, where the slope of VTC is once again -1 .

After V_{IH}, the NMOS will still technically be conducting, but the drain current is too small due to a small leakage current from the PMOS. In real world applications, this value is extremely small and negligible. In the case of CMOS inverters, $V_{OH} = V_{DD}$ at this stage. The simulated VTC matches the expected VTC graph as shown below in Figure 14.

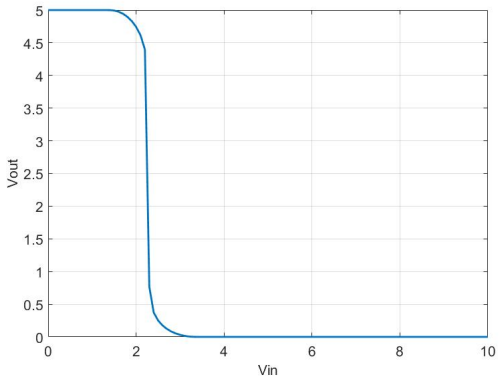

Figure 14: Voltage transfer characteristics - simulated

The simulated VTC graph shows voltage input at the low logic state, $V_{IL} \approx 0V$ and the input at high logic state, $V_{OH} \approx 5V$. The voltage output is essentially the same as the voltage input to the gate except it is inverted. This means that when the input is high, the output will be low and when the input is low, the output will be high. However, the input pulse wave has virtually no rise and fall time for the purposes of this simulation. The output, due to constraints places on it by the characteristics of MOSFETS, will have a rise and fall time for each pulsed wave. These can be seen in Figure 15.

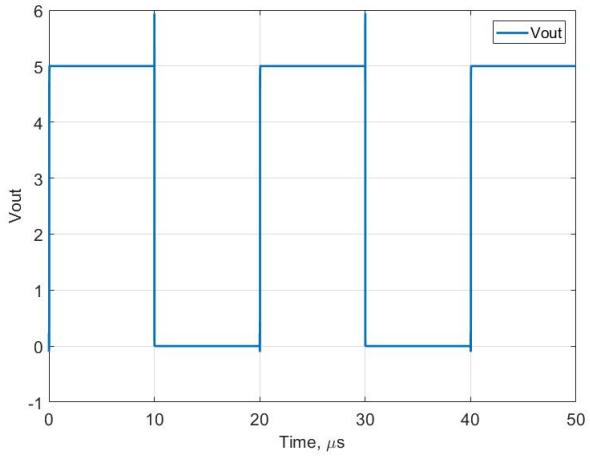

Figure 15: CMOS inverter voltage output

From the graph, the rise time is calculated as 142ns, while the fall time is calculated at 114ns.

2.2.2 CMOS astable multivibrator

The astable multivibrator is another circuit providing an oscillating output. The unique quality that this circuit has, compared to others, is that it has no stable state. Instead, it is in a continuously switching state. This is due to the feedback network which returns the output voltage to the gate of the first inverter, which in turn, causes the state of the input to switch. The oscillation frequency can be altered by the charge and discharge rates of the RC circuit. The operating frequency for the astable multivibrator is described by Equation 4 [3]

$$f = \frac{1.44}{RC}, \tag{4}$$

where the frequency is inversely proportional to resistance and capacitance. The constant 1.44 is a coefficient resulting from the derivation of Equation 4 [3]. The resistance can then be solved for in Equation 4, with an additional factor of three being added, due to three stages, to result in Equation 5.

$$R = \frac{1.44}{3fC}, \tag{5}$$

R is found to be 24kΩ when C is set to 1nF. The schematic for the astable multivibrator using a CMOS is shown in Figure 16.

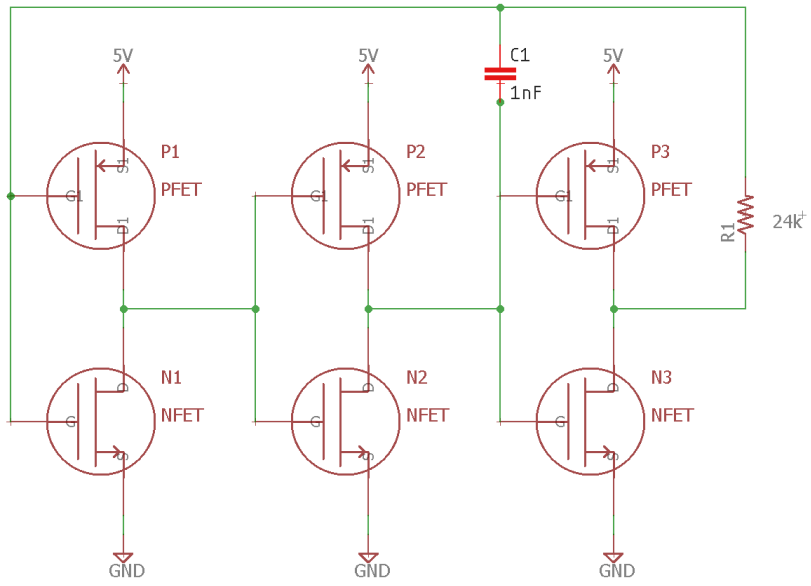

Figure 16: CMOS astable multivibrator schematic - simulated

The resulting waveform is found by using transient analysis in NGSpice, which is shown in Figure 17. The frequency was found to be approximately 19kHz. Subsequently, sensitivity testing was performed on the astable multivibrator using NGSpice.

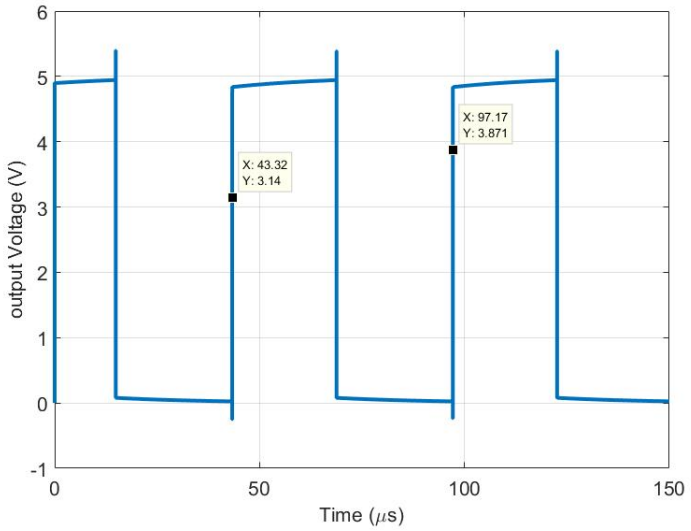

Figure 17: CMOS astable multivibrator output

Subsequently, sensitivity testing was performed on the astable multivibrator using NGSpice. First, 5% tolerance for capacitor values was simulated, and can be seen in Figure 18.

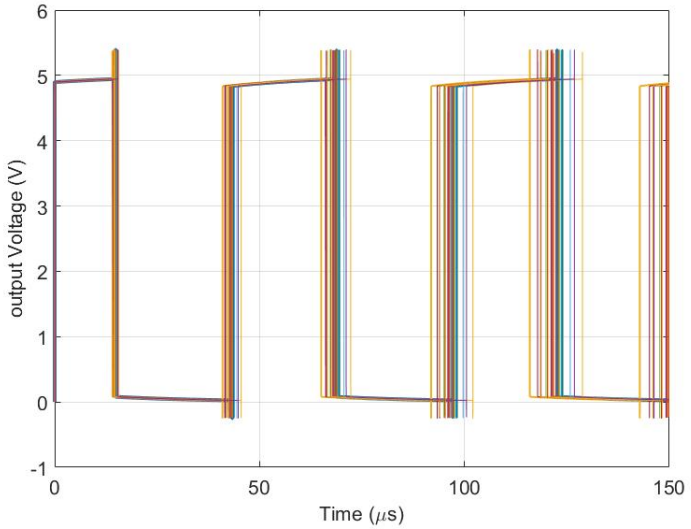

Figure 18: CMOS astable multivibrator - 5% tolerance simulated

This test was performed with 25 iterations, and the effect 5% tolerance had was significant. The effect, however, is even more dramatic when 10% tolerances are used. This can be seen in Figure 19.

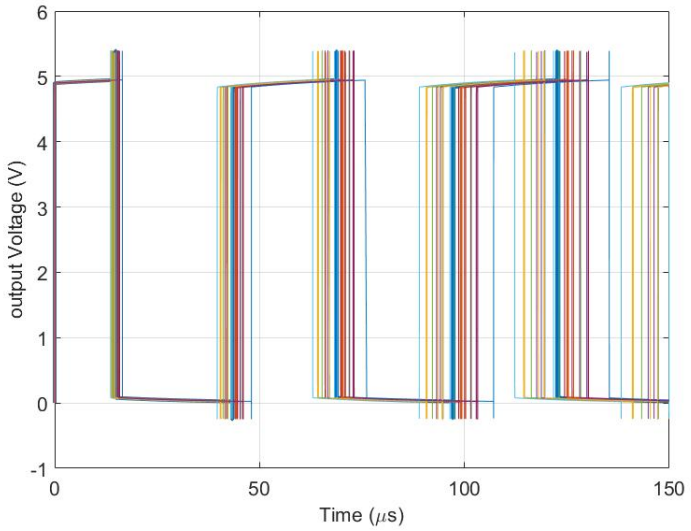

Figure 19: CMOS astable multivibrator - 10 % tolerance simulated

This test was performed with 25 iterations, and tolerances can play a key role in the operating frequency.

2.2.3 CMOS ring oscillator

The design of the CMOS ring oscillator will consist of three CMOS inverters connected in series with the output of the last inverter connected to the input of the first inverter. The ring oscillator will also have a capacitor at each output connected to ground. The schematic for the CMOS ring oscillator can be seen in Figure 20.

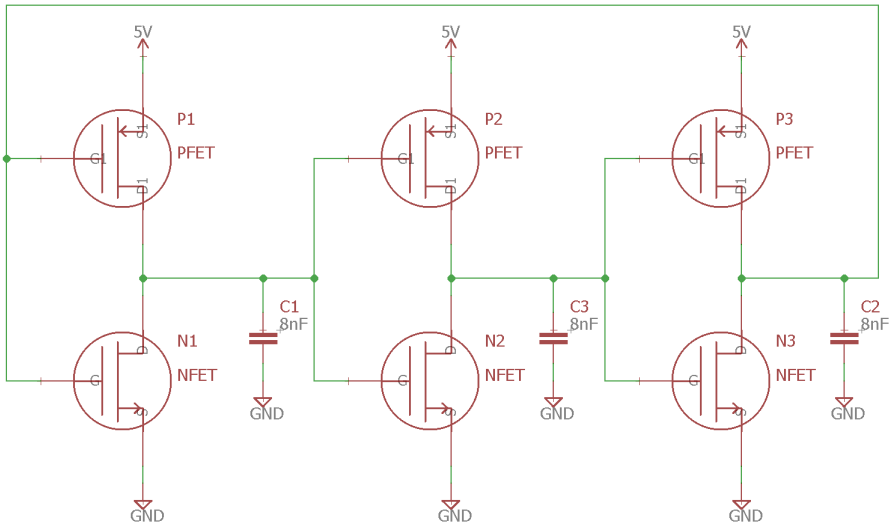

Figure 20: CD4007UBE ring oscillator

The operation of the ring oscillator uses a series of inverters. The output of one inverter inverts the input signal. Therefore, if there are a series of inverters, then each odd inverter will have the same inverted output as the first. In this instance, there are three stages of inverters used, with the output of the third inverter being fed back into the input of the first inverter. This feedback from the output to the input causes an oscillation. Based on this, it would be impossible to provide an oscillation using an even number of inverters connected in series.

The ring oscillator circuit requires only a DC power source with a threshold voltage above what is required of the MOSFETS, and the oscillations will occur. To increase the frequency, the DC supply can be increase, causing an increase in current as well as frequency.

The inverse of the oscillation frequency, the oscillation period, is based on the delay in each stage of the ring oscillator. The period is equivalent to double the sum of all propagation delays. These delays are caused by gates being unable to switch instantly in the real world. In this case, the gate capacitance must be charged before a connection is made between the source and the drain. Otherwise, current will be unable to flow between the source and the drain. The time it takes for the gate capacitance to reach the necessary charge adds a delay to the oscillator. Increasing the number of stages increases the delay time and reduces the frequency. The output waveform is shown in Figure 21.

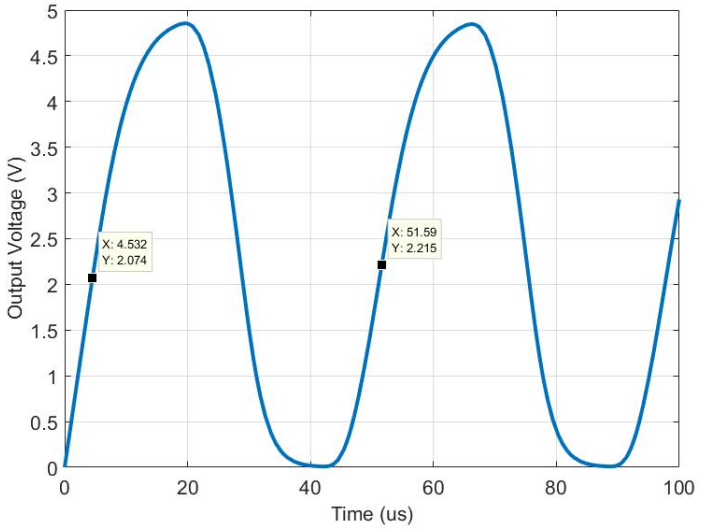

Figure 21: CD4007 ring oscillator output

The operating frequency was found to be approximately 20kHz. Sensitivity testing was performed on the circuit, as seen in Figure 22. The simulated output based on a tolerance of $\pm$ 5% in each of the capacitor values is shown.

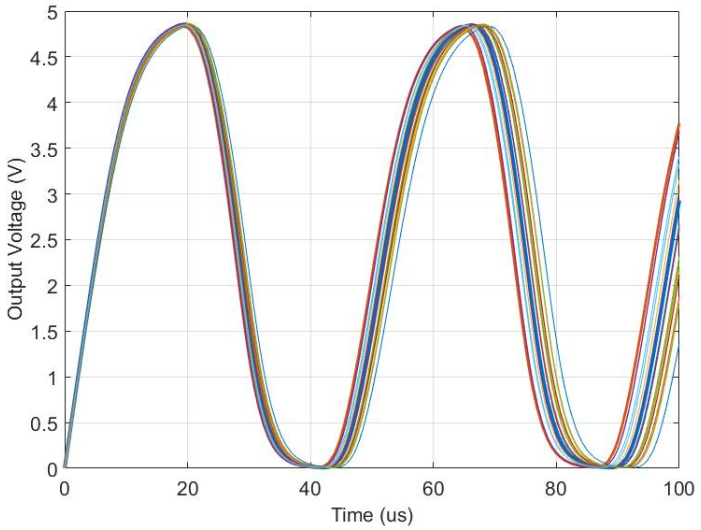

Figure 22: CD4007 ring oscillator - 5% tolerance simulation

As the simulation shows, this slight change in values has an undesired affect on the outputs. Despite only a small percentage change in capacitor values, the output of at 5% does not stray too far from the expected output at ideal values. The simulated output in Figure 23.

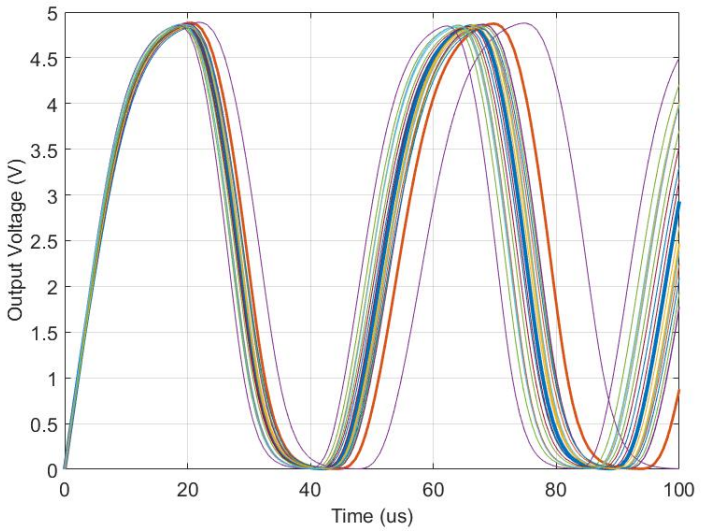

Figure 23: CD4007 ring oscillator - 10% tolerance

As the tolerance of the capacitors in the ring oscillator increase, it causes a larger discrepancy in the values. As time goes on there are variances of almost $10\mu s$ between simulated outputs. Based on these simulations the propagation delay caused by the gates is $\tau_P = 110ns$. The capacitor values were not calculated. Instead, the initial value of 1nF was chosen, then increased until a suitable output was found.

3 Experimental Implementation

The CD4007UBE is a model featuring four on board CMOS circuits tied together. The various circuits were constructed by utilizing these onboard CMOS circuits. The experimental results will be discussed as follows: the NMOS inverter, the CMOS inverter, the AND logic gate, the ring oscillator, and finally the astable multivibrator.

3.1 NMOS inverter

The only change required by the NMOS inverter is that the 4.4kΩ resistor was switched to a 4.3kΩ resistor due to the lack of the availability of the 4.4kΩ resistor. The substitution of a 4.3kΩ in series with a 100Ω with 5% tolerances would introduce too much error into the design.

The VTC of the NMOS inverter is shown in Figure 24.

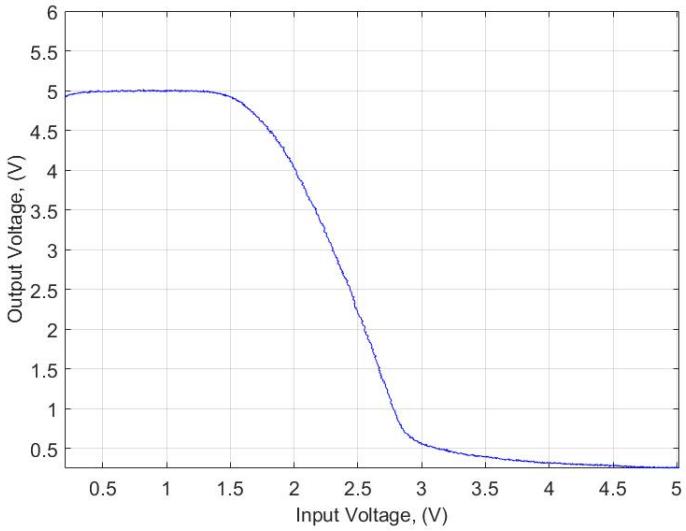

Figure 24: Experimental VTC NMOS

The respective voltages for logic low versus logic high are shown. As expected from simulations, the low logic is not 0V, but instead a rather significant voltage. This accounts for the comparatively significant power consumption used by the NMOS inverter. The power consumption was found to be 5.8mW for logic high and 37μW for logic low. The output waveform is shown in Figure 25

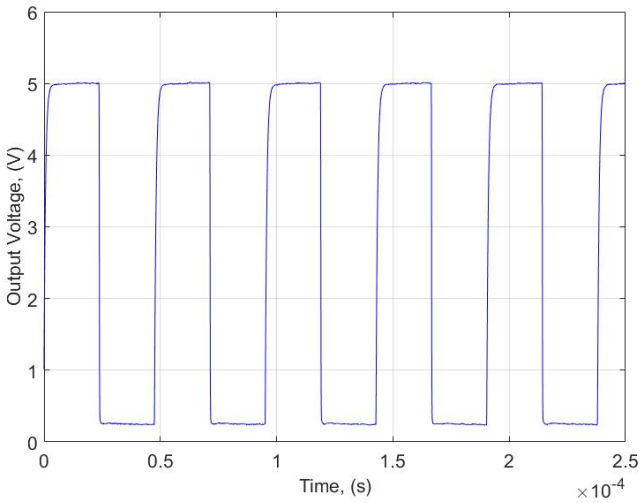

Figure 25: Measured output of NMOS inverter

The rise and fall times were found by the Digilent scope, the rise time was 11.4μs, and the fall time was 1.22μs. The experimental values for the NMOS inverter is shown in Table 2.

Table 2: Experimental values

Experiment Values	Results
R	4.3kΩ
Min Power	37μW
Max Power	5.8mW
V_{max}	5V
V_{min}	400mV
Rise Time	11.4μs
Fall Time	1.22μs

The experiment values that are expressed in Table 2 are different than the simulated due to real world parasitic capacitance and limitations of the breadboard at higher frequencies. The experimental results are as follows: the output voltage, which did not saturate; the frequency response, with a center frequency of 20.2kHz; and the bench test, where the specifications were met.

3.2 CMOS inverter

The only change required for implementation was that all three CMOS inverters were wired together in order to create three inverters in series as opposed to the only simulated two. The measurements were still taken from the output of the first stage. The VTC from the first stage is shown in Figure 26

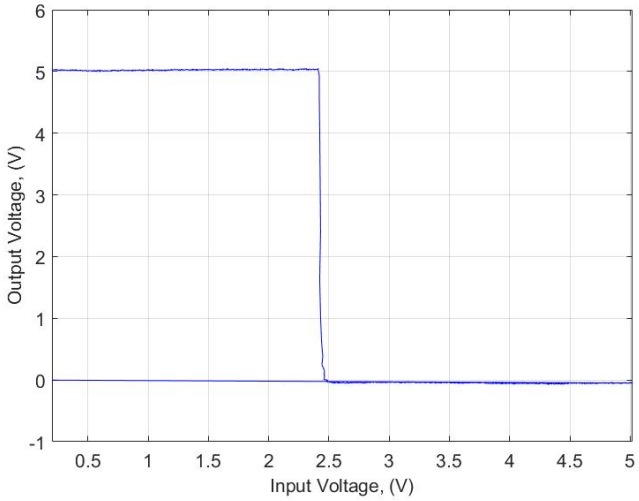

Figure 26: Measured VTC of CMOS inverter

The VTC, as seen in Figure 26, represents logic low as 0V, and improvement over the 400mV of the NMOS inverter. The CMOS inverter also features $0V_{DC}$ power consumption opposed to the NMOS inverter. The output waveform for the CMOS is shown in Figure 27.

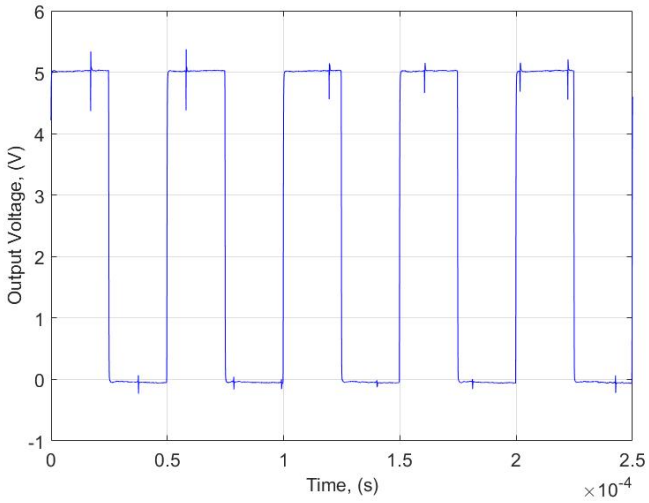

Figure 27: Measured output of CMOS inverter

The subsequent rise and fall times were measured using the Digilent and were found to be 235ns for rise time and 177ns for the fall time. These are greater than those of the simulation, but is not unexpected due to parasitic capacitances and inductances from the jumper wires.

3.3 AND gate

The AND gate was created using all three CMOS circuits on the chip. A NAND gate was constructed using the first two on board CMOS circuits which were then inputed to a CMOS inverter. Figure 28 shows the pinout for an AND gate using the CD4007 IC.

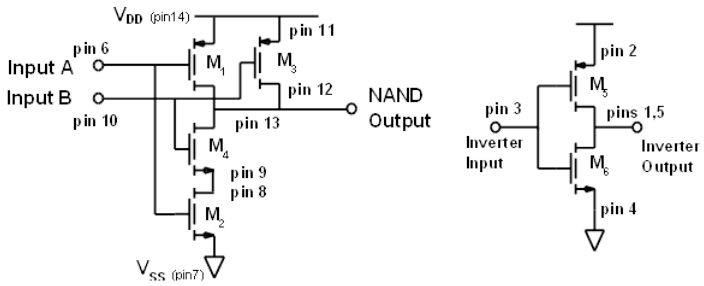

Figure 28: Pinout for AND gate

The output from the NAND gate but before the inverter is expressed in Table 3.

Table 3: Truth Table: NAND

Inputs		Output
A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

The inputs A and B were created by using the Digilent wave generator set to the DC setting, a logic 1 was 2.5V and logic 0 was 0V. The final output after the inverter is expressed in Table 4.

Table 4: Truth Table: AND

Inputs		Output
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

The time-domain graphs for these outputs are of little value, as they express simply a DC voltage at either 2.5V or 0V.

3.4 Ring oscillator

The experimental oscillator required several changes. 8.2nF capacitors were the closest value available to the calculated 8nF. The circuit built with the 8.2nF operated at a frequency of 22.8kHz, which is not within specifications, that frequency is too far outside the bandwidth of the MFBP filter from the previous lab. An additional 4.7nF capacitor was added in parallel with the second stage of the oscillator, resulting in the final circuit is shown in Figure 29.

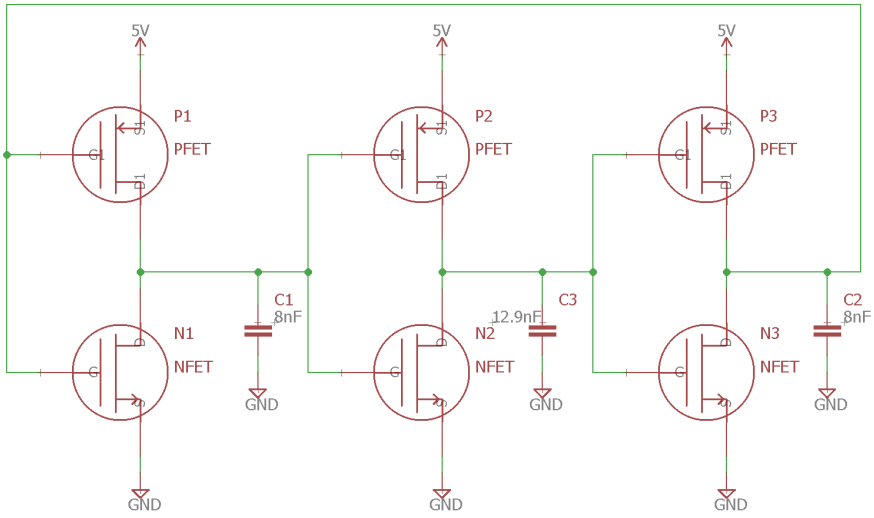

Figure 29: Experimental ring oscillator circuit

The transient analysis was performed on the circuit using the Digilent Scope function. The output waveform is shown in Figure 30.

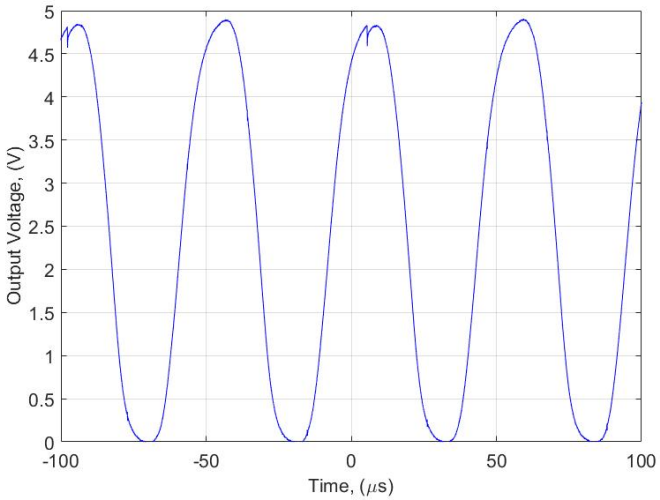

Figure 30: Experimental transient analysis

The frequency was found to be 19.8kHz, a 51% duty-cycle, with a 4.9V peak to peak amplitude. This frequency falls well within the bandwidth of the MFBP filter.

The final experimental results are summarized in Table 5.

Table 5: Experimental results

Value	Experimental
Center Frequency	19.8 kHz
Duty-cycle	51%
Amplitude	4.9V

The experimental results fall within the lab specifications outlined.

4 Discussion

This lab served as introduction to MOSFETS and implementation of digital logic. When using transistors to create digital devices, it is often assumed that the device behaves ideally. When the device is logic high, it is one voltage, and when it is logic low it is another. Based on this logic, it is assumed that the switching on and off of the MOSFETS happen instantaneously. Based on the results of the ring oscillator and other inverter circuits, the MOSFETS do not switch instantaneously. Instead, power is consumed by the MOSFETS when they transition from one state to another. This consumption of power causes a small time delay. Each of the circuits described in this report are discussed in the following subsections, excluding the astable multivibrator. The astable multivibrator was not constructed during the experimental phase of this task.

4.1 NMOS inverter

The NMOS inverter worked as simulated and required no significant design changes in order to function. The measured power consumption was different from the simulated values, but it operated within a tighter band of values. The comparison of the NMOS with simulations is shown in Figure 6.

Table 6: Comparison of NMOS

Component Values	Simulated	Experimental
R	4.4kΩ	4.3kΩ
Max Power	31.2mW	5.8mW
Min Power	69.5pW	37μW
Rise Time	199ns	11μs
Fall Time	195ns	1.22μs

The rise and fall times were significantly greater as well. This can be accounted for by the fact the implemented circuit, in addition to board parasitic capacitance, also had capacitance from the jumpers connecting the pins of the device. Each jumper added capacitance to the circuit, which in turn increased the time constant for the circuit, which would account for the increased transition times.

4.2 CMOS inverter

The CMOS inverter required no changes from simulation. The circuit behaved as expected, with the VTC matching that of the simulations. One of the strengths of the CMOS is the faster transition between logic states. This is reflected in the slope of the experimental VTC. The CMOS also represents logic low with zero volts, as opposed to the NMOS were logic low was still some positive voltage. The DC power consumption of the CMOS was also negligible compared to that of the NMOS. Table 7 shows the differences between the simulated and measured CMOS circuit.

Table 7: CMOS inverter comparison

Component Values	Simulated	Experimental
Rise Time	142ns	235ns
Fall Time	114ns	177ns
Power	0	5μW

The difference in rise and fall times can be ascribed to the parasitic capacitances from the board and jumper wires.

4.3 AND gate

The AND gate operated as expected. This lab served as an introduction to the use of transistors as logic devices. The use of binary logic is fundamental in the design of digital logic. The construction of a physical AND gate demonstrates the real device characteristics of logic circuits. The truth table for the constructed AND gate is shown in Table 8.

Table 8: Truth Table: AND

Inputs		Output
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

The AND gate, in addition to the OR gate, are the fundemental building blocks for digital logic, and thus are of the utmost importance.

4.4 Ring oscillator

The ring oscillator circuit designed with the CMOS did not initially meet the specifications required in the lab. The simulations were accurate, but real-world parasitic capacitances from the board and jumper wires impacted the circuit. To remedy the situation, a capacitor of 4.7 nF was added in parallel after the second inverting gate. By increasing the capacitance the frequency was lowered from 22.8 kHz to 19.8 kHz. The comparison between the simulated results and experimental is expressed in Table 9

Table 9: Comparison of ring oscillator results

Component Values	Simulated	Experimental
C_1	8nF	8.2nF
C_2	8nF	13.9nF
C_3	8nF	8.2nF
Frequency	20.1kHz	19.8kHz
Amplitude	5V	4.9V

The reason this oscillator is chosen over the astable multivibrator as the signal generator is mostly arbitrary and simply design choice for the optical uplink project [4]. Although one of the benefits of the ring oscillator is that from the sensitivity testing it is less affected by component tolerances than the astable multivibrator. This is significant since the capacitors available for circuit construction are 10% tolerances.

5 Conclusion

The design, simulation, and implementation of the ring oscillator signal generator have been explained. NMOS inverters, CMOS inverters, and logic gates were also investigated. Lab specification required that the signal generator have a frequency of approximately 20kHz, a duty-cycle of approximately 50%, and an amplitude of 5V. The signal generator takes an input DC voltage and creates an sinusoidal waveform at the output. The signal generator circuit was constructed using the following parts: three 8.2nF capacitors, a 4.7nF capacitor; and finally a CD4007 CMOS integrated circuit with 5V supply voltages. The frequency was 19.8kHz, with a duty-cycle of 51%, and an amplitude of 4.9V. An important lesson about the behavior real logic circuits was learned. Real digital circuits have measurable electrical characteristics and do not behave ideally.

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