Task 4: Operational Amplifier

Discrete Amplifier

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Abstract

The design, simulation, and construction of experiments to measure the performance of an operation amplifier is explored. The operational amplifier consists of four discrete stages: a cascoded current mirror, an actively loaded differential pair, a common source amplifier, and finally a Bipolar Junction Transistor class B amplifier. The operational amplifier was designed to operate with a bias current of 400μA using the ALD1106 and ALD1107 series MOSFETS. The common mode rejection ratio was 75 dB, the common mode gain, Acm, for 100mV input was -10 dB, the Acm for 1 V input was -9 dB and differential gain, Ad, was found to be 67 dB.

DC node voltage/current measurement comparison table to discussion, will help identify source of error

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1 Introduction

This report describes the design, construction, and analysis of a discrete component operational amplifier. The topology chosen includes a cascoded current mirror that sinks current to an actively loaded differential pair amplifier which outputs single-endedly to a common source amplifier stage. This common source stage is then passed to an output Bipolar Junction Transistor (BJT) amplifier stage. The metal oxide semiconducting field effect transistors (MOSFET) in use are the ALD1106 for NMOS and the ALD1107 for PMOS. The general schematic for a generic op amp is shown in Figure 1.

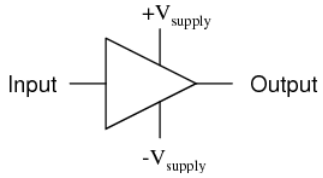

Figure 1: General operational amplifier symbol [1]

Operational amplifiers serve an integral building block for modern electronics. Op amps provide large gain with various configuration schema. This allows the circuit designer to use the op amp in different topologies and achieve different results, all without modifying the op amp circuit itself. In addition, an op amp provides significant gain while maintaining stability. The objective of this lab is to create an op amp out of discrete components that achieves the specifications as seen in Table 1.

Table 1: Specifications

Specifications	
Power	$\pm$5V
Bias Current	500 μA
Overall Voltage Gain	200V/V (46 dB)
CMRR	$\geq$ 60dB
Output Voltage Swing	$\geq \pm$ 2V

The input stage of an operational amplifier consists of a differential amplifier. Differential amplifiers are desirable for their increased immunity to noise and that DC coupling of stages is possible without disturbing bias conditions. Each one of these designs will have some advantage as well as some disadvantage over the other circuits. The primary function of the input differential pair will be to provide a high common mode rejection ratio (CMRR). The differential gain, A_d, need not be high, as long as the common mode gain, A_{cm}, is very small. This in turn is passed to an active load differential pair where the bulk of the differential gain will be achieved single endedly. The common source provides a final gain stage while reducing the effects of the output impedence of active load stage.

Section 2 of this report describes the design, and when relevant, the simulations of the experiments. Experimental results and implementation are addressed in Section 3, including reasoning as to why a different circuit than the one outlined previously was constructed. A discussion of the results, sources of error, and areas of possible improvement are outlined in Section 4. Section 5 concludes this report.

2 Circuit Development

Three different op amp topologies were provided as part of the lab. The chosen circuit can be seen in can be seen in Figure 2.

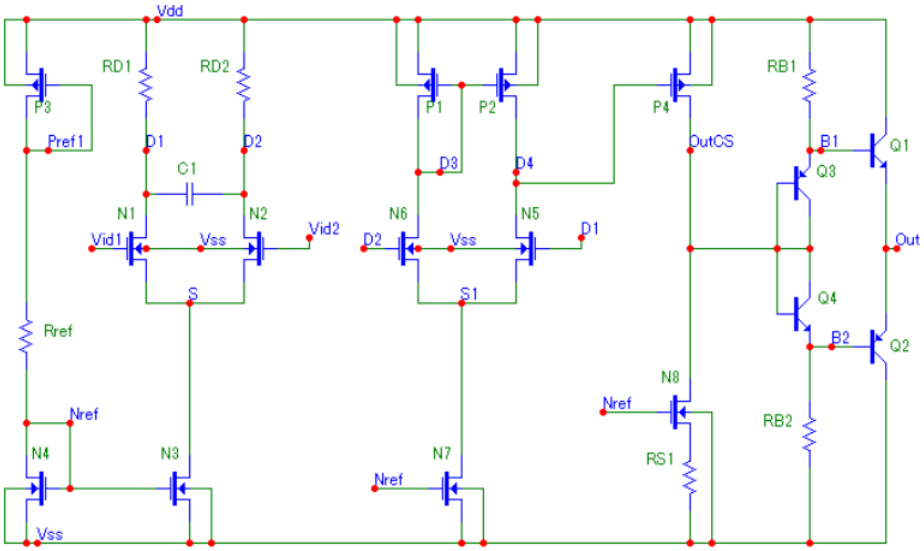

Figure 2: Generic schematic for chosen topology [2]

This design was chosen due to the fact that every stage, with the exclusion of the output stage, was designed as part of lab 2 and 3. The stages can be broken down as such: a simple current mirror, a resistively loaded differential pair, an active loaded differential pair, an active load common source amplifier and finally a BJT amplifier output stage. The final simulated circuit can be seen in Figure 3.

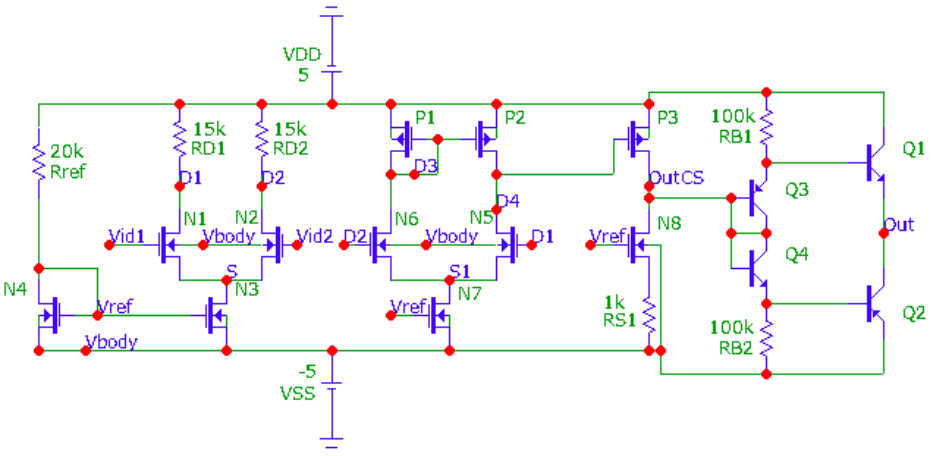

Figure 3: Simulated op amp circuit

The circuits will be simulated in MicroCap 11. The values for the components will initially be the values calculated in circuit development. The generic bias conditions for the ALD1106 and 1107 are summarized in Table 4.

I_{DS}	ALD1106				ALD1107			
	V_{OV}	V_{GS}	g_m	r_o	$\|V_{OV}\|$	V_{GS}	g_m	r_o
100 µA	0.63	1.43	3.16E-04	333 kΩ	1.00	-1.80	2.00E-04	333 kΩ
200 µA	0.89	1.69	4.47E-04	167 kΩ	1.41	-2.21	2.83E-04	167 kΩ
400 µA	1.26	2.06	6.32E-04	83.3 kΩ	2.00	-2.80	4.00E-04	83.3 kΩ
500 µA	1.41	2.21	7.07E-04	66.7 kΩ	2.24	-3.04	4.47E-04	66.7 kΩ
1 mA	2.00	2.80	1.00E-03	33.3 kΩ	3.16	-3.96	6.32E-04	33.3 kΩ
2 mA	2.83	3.63	1.41E-03	16.7 kΩ	4.47	-5.27	8.94E-04	16.7 kΩ

Figure 4: Typical ALD bias conditions [3]

Here the typical bias conditions for the constraining MOSFETs can be seen. For the purposes of this lab, the bias current of 400 μA was chosen.

2.1 Resistively Loaded Differential Amplifier

The resistively loaded amplifier stage requires a current mirror in order to generate the chosen bias current of 400 μA. This was achieved by applying Ohm's Law. The V_{gs} of the simple current mirror needs to be -3V. In order to have the correct current R_{ref} was set to 20kΩ. The simulated resistive load differential pair can be seen in Figure 5.

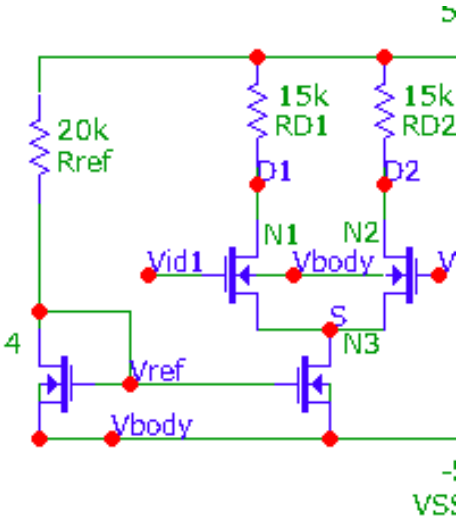

Figure 5: Simulated resistive load differential amplifier

In addition, the current through the load resistors needs to be half of the bias current. As a result, the resistance values can be found by applying KVL which can be seen in Equation 1

$$V_{o_1} = V_{DD} - \frac{1}{2} I_{bias} R_d, \tag{1}$$

where V_{DD} is the supply voltage. This leads to R_{drain} of 15kΩ. The differential gain of the circuit can be found by Equation 2

$$A_d = g_m R_d, \tag{2}$$

where g_m is the transconductance of the amplifying NMOS and R_d is the drain resistance and was calculated to be 16 dB. The output is double ended due to it feeding another amplifier stage. The simulated gain can be seen in Figure 6.

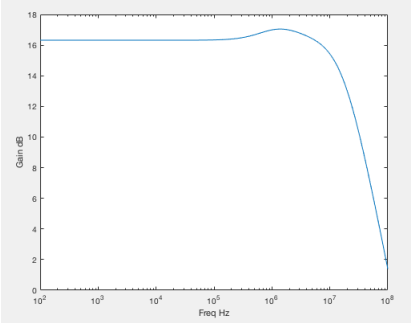

Figure 6: Simulated resistive load differential gain

This was measured by performing an AC analysis in Microcap from 100Hz to 1MHz. This was performed by grounding one of the inputs whilest measuring the voltage differentially from the output nodes. The simulated value was marginally higher at 16.2 dB. The simulated phase can be seen in Figure 7.

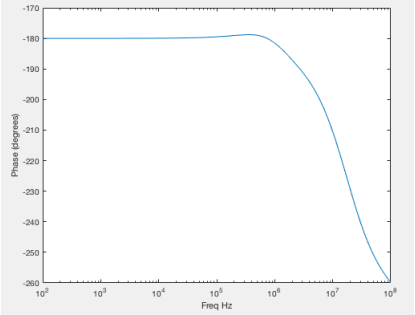

Figure 7: Simulated resistive load differential phase

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The phase can be seen to be 180 degrees stable until 1 MHz. This is desirable for an input stage, which is why the differential pair was chosen as the first stage. This stage was then cascaded with an active load differential pair.

2.2 Active Load Differential Pair

The next stage of op amp is the active load differential pair. This circuit is identical to that designed in Task 3. This circuit can be seen in Figure 8. This modification allows for the single ended output to achieve gain that is comparable to that of the active load with a double ended output.

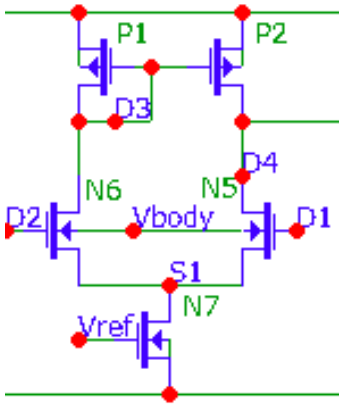


Figure 8: Simulated active load differential amplifier

The differential gain for an actively loaded differential pair can be seen with Equation **??**

$$A_d = g_{m_N}(r_{o_P}||r_{o_N}), \tag{3}$$

where r_o is the small signal output resistance of a MOSFET which is found by the Equation **??**

$$r_o = \frac{1}{\lambda I_{DS}}, \tag{4}$$

where λ is the channel length modulation parameter. The output resistance for NMOS is found to be 172kΩ and PMOS is found to be 162kΩ. he differential gain was calculated to be 35 dB. The simulated differential gain for the active load can be seen in Figure 9.

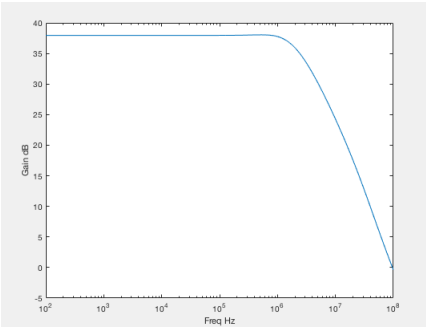


Figure 9: Simulated active load differential gain

This simulation was performed in the same manner as the resistive load. The differential gain is found to be much high than resistive load at 38 dB and consistent with the calculated value of 35 dB. The phase of the active load can be seen in Figure 10.

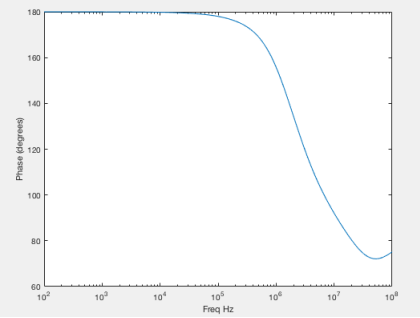


Figure 10: Simulated active load differential phase

This stage can be seen to only be 180 degree stable until 100 kHz. This is the minimum required by the lab specifications. This stage is then passed to an active loaded common source stage.

2.3 Common Source Amplifier

The common source amplifier features an active load which serves as a biasing network. The common source allows for the output loading effects of the active load to be ignored due to the near infinite input impedence seen at the gate of the common source. The simulated circuit can be seen in Figure 11.

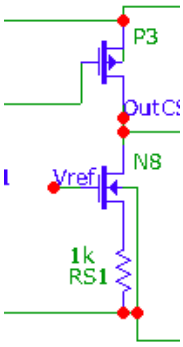


Figure 11: Simulated common source amplifier

The voltage gain of a common source amplifier can be expressed in Equation 5

$$A_{vo} = -\frac{g_m R_d}{1 + g_m R_s}, \tag{5}$$

where R_s is the resistance seen at the source of the amplfying transistor which in this case is the r_o of the

active load. The gain can be calculated to be 23 dB. The active load features source degeneration, this resistor value should be large enough to ensure that with grounded inputs the common source output node is 0V. The resistor that achieved this is 1 kΩ. The simulated gain can be seen in Figure 12.

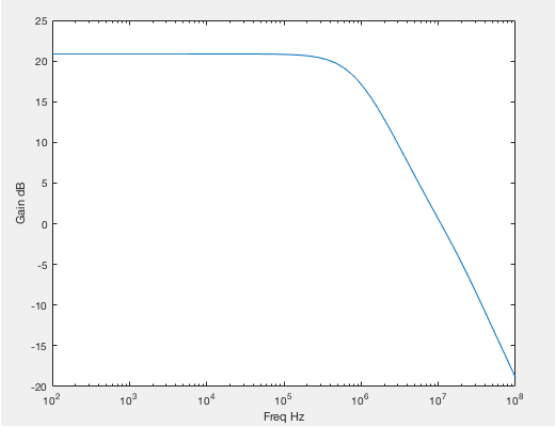


Figure 12: Simulated common source amplifier gain

The gain is slightly less than the calculated 23 dB at 20.5 dB. The phase the common source stage can be seen in Figure 13.

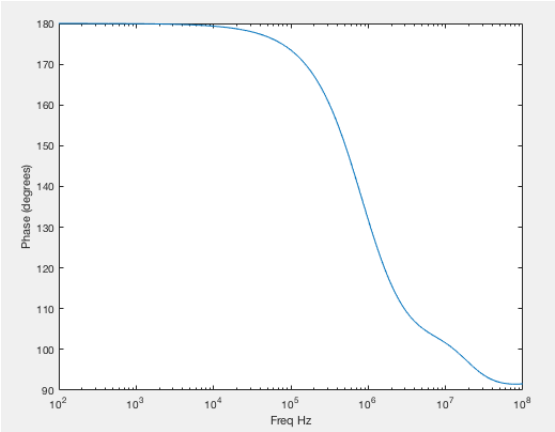


Figure 13: Simulated common source amplifier phase

The common source, similar to that of the active load, is 180 degree stable until 100 kHz. The common source is then fed to an output stage. The output stage will be covered in more detail in a later task. For the purposes of this lab the output stage can be treated as an emitter follower.

2.4 Output Stage

Due to the design of this stage being mostly beyond the scope of this task; the largest design consideration was choosing resistors values great enough to ensure that the base emitter voltages of remain less than 0.7V. These values were changed in Microcap until the correct bias conditions were found. The resistor values were found to be 100 kΩ. The output gain can be expressed through Equation 6

$$A_{vo} = \frac{g_m R_E}{g_m R_E + 1}, \tag{6}$$

where R_E is the resistance seen at the emitter of the BJT and g_m is the transconductance on the BJT. The gain can be calculated to be 0.96 V/V. The simulated gain can be seen in Figure 14.

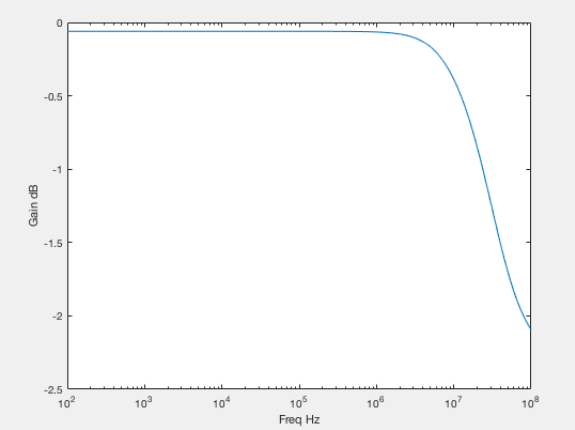


Figure 14: Simulated output stage gain

The gain can be seen to be a little less than one, this is expected by the emitter follower nature of the stage. The Ideal emitter follower has a voltage gain of 1 V/V. The simulated phase can be seen in Figure 15.

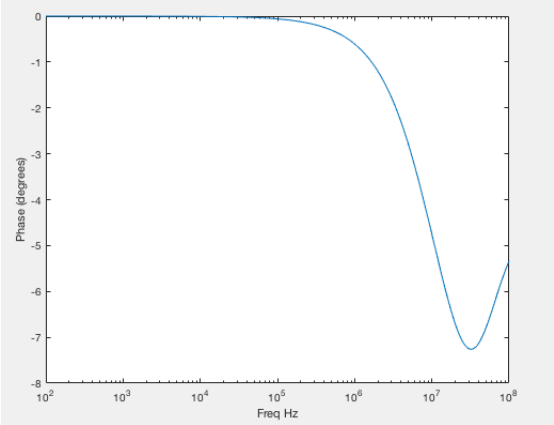


Figure 15: Simulated output stage phase

The output stage remains 180 degree stable until 1 MHz, which is a decade higher than the previous two stages. The overall gain of the circuit can be seen in Figure 16.

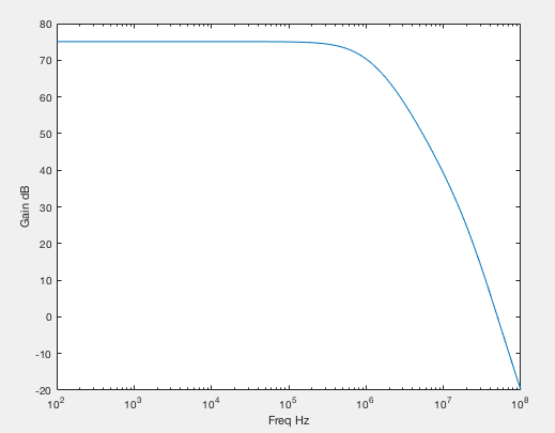


Figure 16: Simulated overall gain

The gain can be seen to be much greater than the required 46 dB at 75 dB. Care is necessary when building this circuit as very little input could result in a railed output. The final phase can be seen in Figure 17.

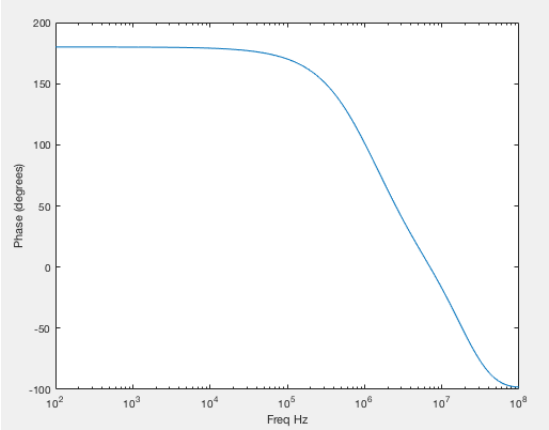


Figure 17: Simulated overall phase

The final output can be seen to be 180 degree stable until 100 kHz, which is required by the specifications. The DC bias conditions measured in Microcap can be seen in Table 2.

Table 2: DC bias values

Simulated Values	
Vref	-3.003V
D1	1.284V
D2	1.284V
D3	2.78V
D4	2.78V
S	.972V
S1	-1.34V
OutCS	-82mV
Out	-11.4mV
A_d First Stage	16.2 dB
A_d Second Stage	38 dB
A_{vo} Common source	20.5 dB
A_{vo} Output Stage	-.1 dB
A_d Final	75dB

The DC bias conditions match that of this found in previous tasks. Notably the output of both the CS and final stage is not 0V. This is due to body effect and channel length modulation effects, this voltage is known as the offset voltage.

3 Experimental Implementation

This section details the experimental implementation of the two differential amplifiers, the resistively loaded and active loaded. The power supplies and analysis were implemented using the Digilent Analog Discovery kit. The experimental circuit can be seen Figure 18.

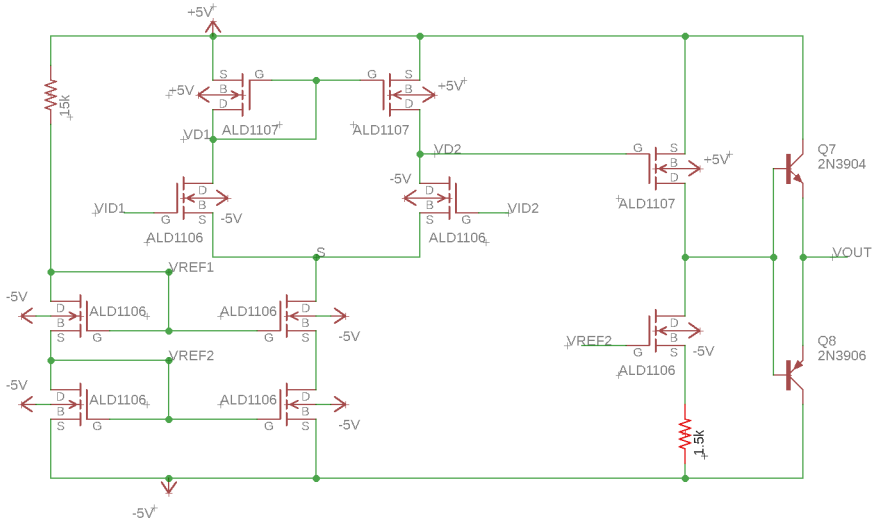


Figure 18: Experimental operational amplifier

The simulated circuit, when constructed, failed to meet both the final differential gain output of 46 dB as well as the CMRR of 60 dB. As a result the final circuit design was changed to the op amp design #1, which can be seen in Figure 18. Further details on why design was changed can be found in the Discussion section.

The DC bias conditions were measured using a DT830B DVM. Nodal voltages were measured in reference to ground and current was measured by wiring the DVM in series while in ammeter mode. The bias conditions were measured while both input nodes to the circuit were grounded. The final measured values can be seen in Table 3.

Table 3: Experimental DC values

DC Bias Conditions	
Vref	-2.97V
Iref	396μA
D1	2.01V
D2	1.99V
S	-2.04V
OutCS	100mV

Notably, the voltage at the "OutCS" node should be zero. In the default state, the offset at that node was measured to be 2.5V. A potentiometer was used as the source degeneration resistance for the common source amplifier. This pot was varied until the offset was nulled out and the final resistance value required was found to be 1.5kΩ. The range of operation for the circuit can be seen in Figure 19.

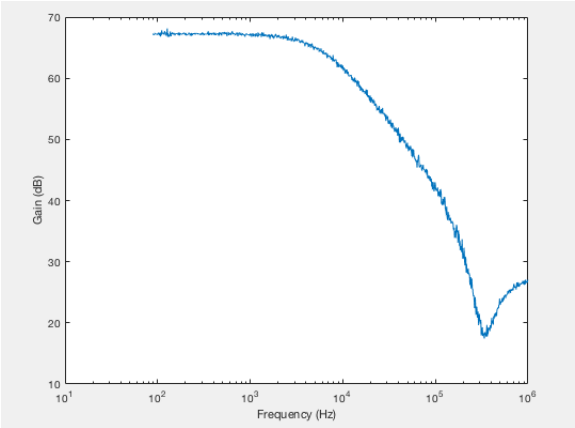


Figure 19: Experimental range of operation

The range of operation is extremely narrow. This, however, is expected due to the limits imposed by the use of a cascode current mirror. The cascode affords more gain at the expense of voltage range. This was explored in more depth in Task 3. In order to prevent the op amp from saturating, a 1000:1 voltage divider was added at the signal input. The channel 1 probe was connected after the voltage divider to compensate for the 60dB drop from the voltage divider. Channel 2 was connected at the final output of the operational amplifier. The final differential gain can be seen in Figure 20.

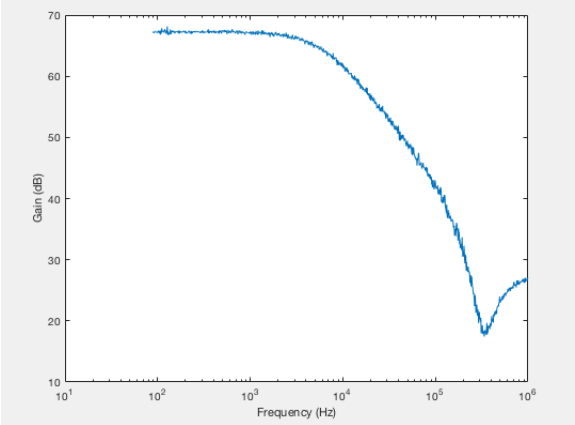


Figure 20: Experimental differential gain

The max differential gain can be seen to be 67 dB. This is more than 20 dB greater than the minimum specification. Even more noteworthy, however, is the fact that the gain is not unity gain stable. The gain plot, at least within the range of 100 Hz to 1MHz, never crosses the 0 dB point. As a result, the amplifier is said to not be unity gain stable. This can be remedied by including a capacitor at the output stage and will be done during Task 5. The phase of the differential gain phase can be seen in Figure 21.

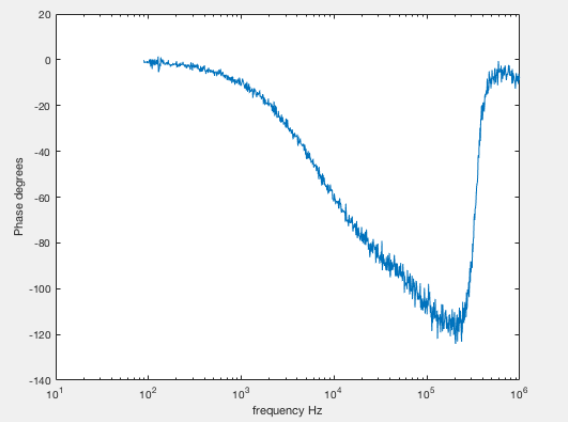
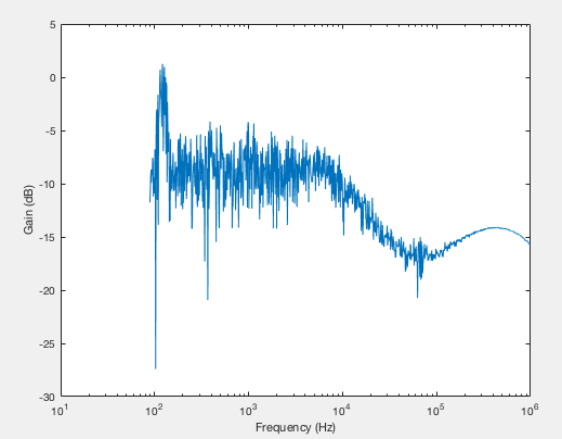
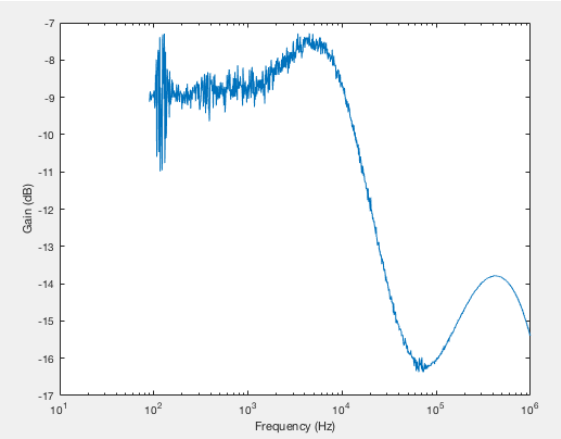


Figure 21: Experimental differential gain phase

The phase can be seen to return to unity after 100kHz. This is also a result of the lack of frequency compensation. Notably, the phase mirrored that of the simulated design quite well. The final design spec is that the circuit must achieve a CMRR of at least 60 dB. In order to find the CMRR the common mode gain must be found by applying a signal to both inputs while measuring the output gain via the Analog Discoveries Network analyzer mode. The common mode gain for both 100mV and 1V can be seen in Figure 22.



(a) Common mode gain, Acm at 100mV



(b) Acm, single ended

Figure 22: Common mode gain, Acm at 1V

The common mode gain is still negative, which is desired. The Acm is -10dB this is, however, much lower than what was found in Task 3, which was found to be on the order of -60 dB. This is mostly due to the fact that a significant portion of the op amps gain is now coming from the common source stage and not just the active load differential pair. The CMRR is then found by finding the difference between the differential gain and the common mode gain in Matlab.

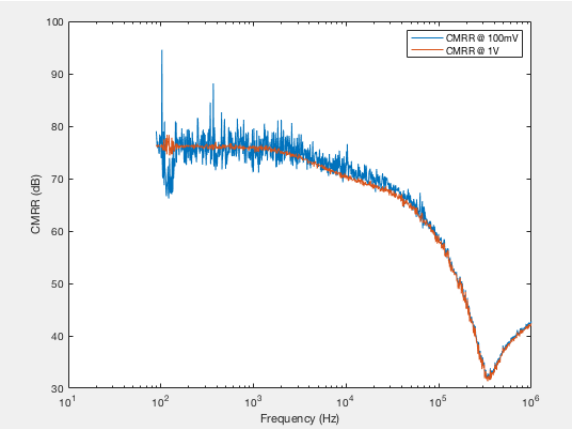


Figure 23: Experimental common mode rejection ratio

As expected, the CMRR was much cleaner when the input signal was 1V as opposed to a 100mV signal. The measured value was 75 dB, which is greater than the minimum specification of 60 dB. The summary of experimental values can be seen in Table 4.

Table 4: Final experimental values

Experimental Values	
Ad	67dB
Acm	-10dB
CMRR	75 dB

The experimental values all met specifications. Further discussion of the op amp and why the changes were made between the design's can be found in the Discussion section.

4 Discussion

This lab served as the culmination of all prior tasks. The operation amplifier includes a current mirror, both types of differential pairs active and resistive as well as a common source amplifier. The final values can be seen in Table 5 below.

Table 5: Final values for operational amplifier

Operational Amplifier Results		
Values	Simulated	Experimental
V_{ref}	-3.003 V	-2.97V
I_{bias}	400μA	396μA μA
R_{ref}	20kΩ	15kΩ
R_{D_1}	15kΩ	N/A
R_{D_2}	15kΩ	N/A
Ad	75 dB	67dB
S node	1V	-2.04V
D1	2.78V	2.01V
D2	2.78V	1.99V
Ad	75 dB	67 dB
CMRR	N/A	75dB

The final experimental circuit required a different op amp design. The simulated circuit failed to meet specifications despite many minor alterations. A problem encountered with the simulated design was that due to mismatch in both resistors and transistors, the gain was did not meet spec. The discrepency between resistor values resulted in a consistently positive Acm, which always led to a CMRR that failed to meet the final specifications. In addition, due to consistantly mismatched transistors the final differential gain could only achieve at most 30 dB. Because of these reasons the design was switched to the active load with a cascoded current mirror.

The cascode + active load design featured several advantages over the orginal design. The experimental was able to achieve 67 dB of differential gain, which is more than 20 dB greater than the specification. This is because the cascoded current mirror affords more amplification at the expense of operation range. In addition, the lack of resistors meant that the Acm was no longer vulnerable to resistor mismatch. This can be seen by the Acm of the final circuit being a negative value, which resulted in a CMRR that was 10dB higher than the specification of 60 dB.

A problem that was encountered is that the final circuit is not unity gain stable. This because of the fact

final output stage was implemented without the required capacitor. This will be remedied in Task 5. The solution is to find the node that is contributing the smallest pole frequency. After this is found the unity gain frequency should be set to the second pole frequency via choice placement of a capacitor. This modification will ensure that the amplifier remains unity gain stable. It should be noted however that the implemented amplifier provides gain until past 150kHz, thus meeting the specification required by the lab.

5 Conclusion

The design, simulation, and construction of experiments to measure the performance of an operational amplifier was explored. The amplifier consisted of three discrete stages, an actively loaded differential pair, a common source amplifier, and a BJT output stage. This circuit will serve as the foundation for the final design of the operational amplifier in task 6. The operational amplifier still requires frequency compensation in order to maintain stability. An important lesson learned during this lab was that simply achieving a high gain is not enough for a circuit to be considered operational. Whether or not the op amp is stable is as important as the final gain value.

References

[1] All About Circuits. (2018) Single-ended differential amplifiers [Online]: https://www.allaboutcircuits.com/textbook/semiconductors/chpt-8/single-ended-differential-amplifiers/

[2] N. W. Emanatoglu. (2018) Task 4 [Online]

[3] N. W. Emanatoglu. (2018) Task 4 briefing [Online]