# Task 5: Operational Amplifiers: Feedback and Stability

**Optical Uplink**

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**Abstract**

The design, simulation and construction of a differential amplifier circuit (developed in task 4) with feedback is described. In this task a multistage op-amp with a class B output amplifier will be developed, simulated and constructed. The required differential voltage gain for this circuit is 200 $\frac{V}{V}$ while driving the smallest load possible. The uncompensated unity gain is required to be larger than 150 kHz. The gain was measured at 63.3 dB while unloaded. The smallest value for the load resistor which caused a 3 dB drop in gain was found to be 500 $\Omega$, with a gain measured at 66.33 dB. The unity gain uncompensated unity gain frequency was measured at 170 kHz.

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# 1 Introduction

This report describes the design, construction, and analysis of negative feedback for an operational amplifier. This is achieved using resistors attached to and across certain nodes in the op amp in Figure 1

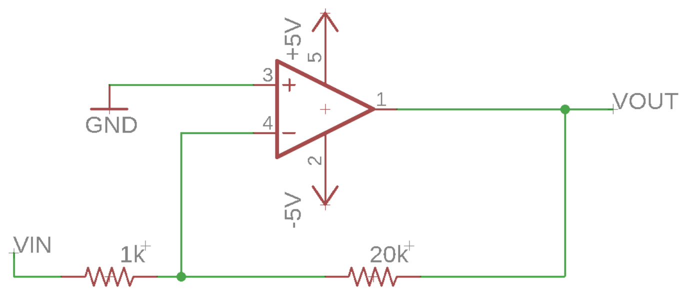



Figure 1: Sample experimental circuit demonstrating feedback

Operational amplifiers serve an integral building block for modern electronics. Op amps provide large gain with various configuration schema. This allows the circuit designer to use the op amp in different topologies and achieve different results, all without modifying the op amp circuit itself. In addition, an op amp provides significant gain while maintaining stability, this is where the output stage comes in. The output stage allows design to accommodate for non-controllable factors such as transistor mismatch and temperature variation. The objective of this lab is to apply feedback to the op amp so that the op amp achieves the specifications as seen in Table 1

Table 1: Task 5 Specifications

| **Specifications** | |
|---|---|
| Power | $\pm$5V |
| Output Stage | $\geq$ 500$\Omega$ |
| Bias Current | 400 $\mu$A |
| Overall Voltage Gain | $\geq$200V/V (46 dB) |
| CMRR | $\geq$ 60dB |
| Output Voltage Swing | $\geq \pm$ 2V |

Section 2 of this report describes the design, and when relevant, the simulations of the experiments. Experimental results and implementation are addressed in Section 3, including reasoning as to why a different circuit than the one outlined previously was constructed. A discussion of the results, sources of error, and areas of possible improvement are outlined in Section 4. Section 5 concludes this report.

# 2 Circuit Development

This section covers the design choices associated with the actively loaded differential amplifier with cascoded current mirror and a class B amplifier for an output stage. Frequency compensation will also be considered in the development to ensure stability.

The circuit that was developed in task 4 will be used for the purposes of this circuit development section. The output stage will be added in this task which will be a class B amplifier. The class B amplifier will consist of a 2n3904 NPN BJT and a 2n3906 PNP BJT. The simulations were conducted in Microcap 10. As these schematics are difficult to read, a set of schematics with identical values and components were created in Eagle by Autodesk. The simulated schematic can be seen in Figure 2 below.

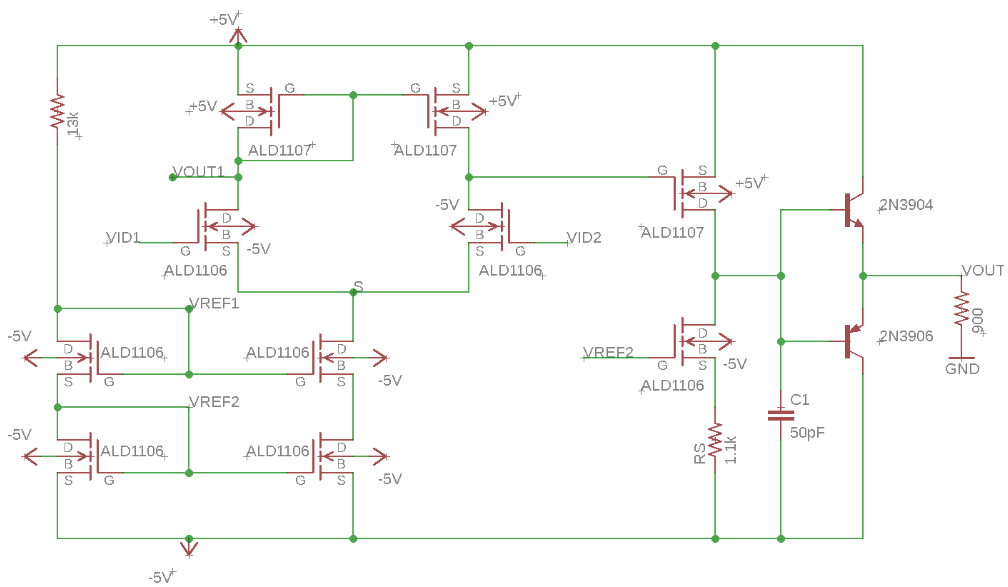



Figure 2: Simulated Circuit

The value of 13 kΩ was taken from the previous lab which gave a reference current of 401 $\mu$A. There are several specifications to meet, or at least come near for the completion of this task. The unity gain frequency should be above 150 kHz. A small load resistance of 500 Ω or less should cause a drop of 3 dB from the unloaded gain. Lastly, the gain needs to be high than 200 $\frac{V}{V}$ or 46 dB. The equation for closed loop gain is shown below in equation 1.

$$A_f(j\omega) = \frac{x_o}{x_i} = \frac{A_f(j\omega)}{1 + A_f(j\omega)\beta} \tag{1}$$

The part of the denominator, $A_f(j\omega)\beta$ is the actual loop gain for the amplifier, which it is much greater than one, then the closed loop gain is approximately $\frac{1}{\beta}$. The value of $\beta$ in this case was found to be $21\frac{V}{V}$. The value for the resistor at the source of the ALD1106 NMOS, RS, was found to be 1.1k in the previous lab, and yielded similar results for this simulation, as it gave the appropriate offset nulling at the base of the BJTs at approximately zero volts. This will allow the amplifier to have it's maximum amount of gain.

The output of the amplifier met the specifications as it was simulated to have a 63.3 dB gain. To find the smallest load resistor that the amplifier could drive, Microcap 11 was used to do a sweep of load resistor values from 250 Ω to 2.5 kΩ. The goal is to find the load resistor value that will cause a 3 dB drop from the unloaded gain, which would be 60.3 dB, or at least a value close to that. The result can be seen in Figure 3 below.

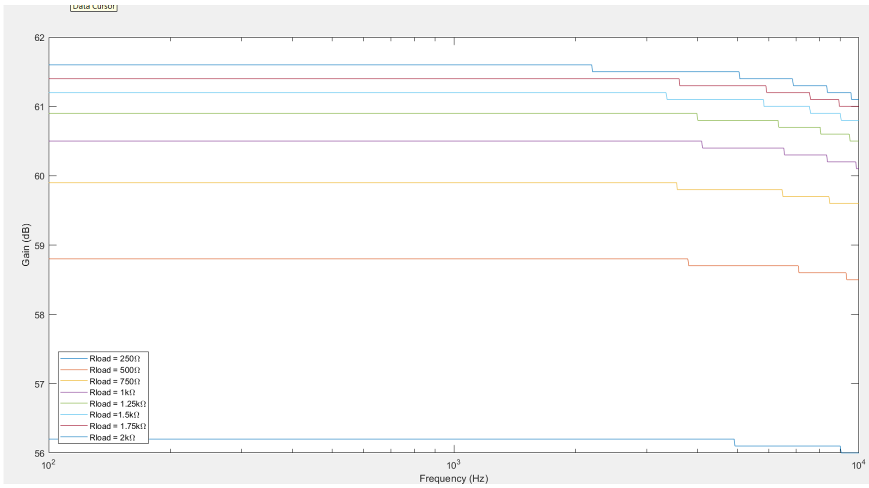



Figure 3: Sweep values of load resistor vs gain

It was found that the load of approximately 900 Ω caused a 3 dB drop in gain. A load of 500 Ω caused a 6 dB drop. Therefore, 900 is the smallest load the circuit can drive according to the simulation. Using this value for the load, a simulation was conducted and the resulting data was exported to Matlab to plot. The gain verses frequency plot at a 900 Ω load resistance is seen below in Figure 4. During this simulation, the capacitor at the collector of the 2n3906 (used for frequency compensation) was found to work at any value below 500 pF.

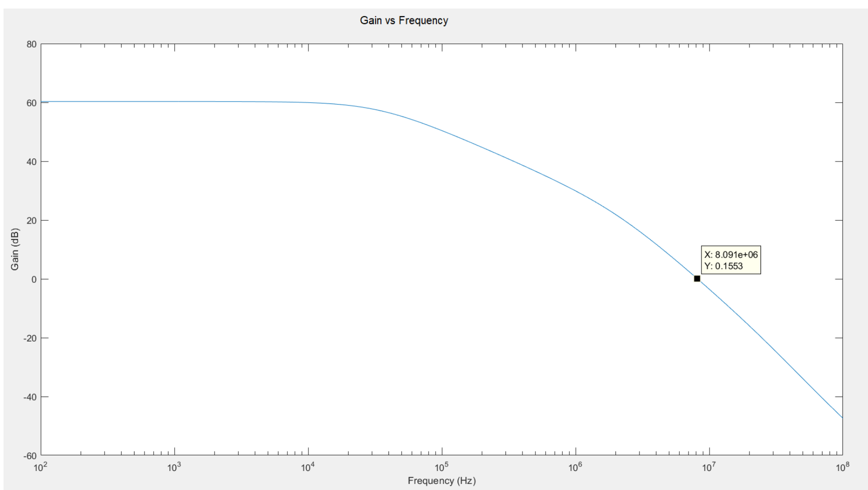



Figure 4: Gain with 900 Ω load resistance

As seen, the gain is valued at just over 60 dB, which meets the 3 dB drop in gain requirement at 900 Ω load. The zero crossing for the gain was found to be approximately 8 MHz. In order to be a stable amplifier, the phase shift should not change more than 180 degrees before the zero crossing of the gain. The resultant phase plot from simulations is see in Figure 5 below.

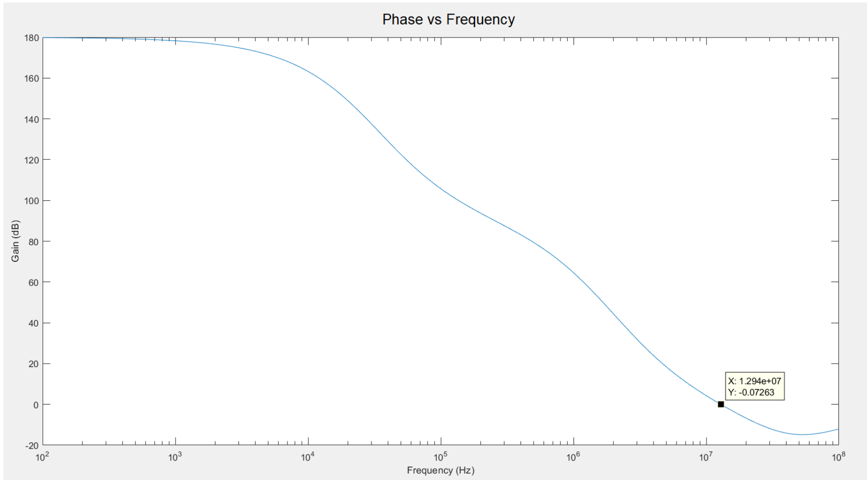



Figure 5: Phase plot with 900 Ω load resistance

The value for an 180 degree phase shift was found to be approximately 12.9 MHz from the simulations. This is well beyond the required 8.9 MHz found from the plot of the gain in Figure 4. All of the nodal voltages and currents were found during the simulation using dynamic DC analysis in Microcap 11. The current values are shown in Table 2 AC analysis was used in order to simulate the gain and phase.

Table 2: Current values from simulated circuit

| Simulated current values | |
|---|---|
| $I_{Ref}$ | 410.8 $\mu$A |
| $I_{D_1}$ | 204.4 $\mu$A |
| $I_{D_2}$ | 204.4 $\mu$A |
| $I_{CS}$ | $\approx$ 227 $\mu$A |
| $I_C$ | $\approx$ 2 $\mu$A |

The voltage values are seen in Table 3 below.

Table 3: Current values from simulated circuit

| Simulated voltage values | |
|---|---|
| $V_{Ref_2}$ | -340 mV |
| $V_{Ref_1}$ | -2.987 V |
| $V_{D_1}$ | 2.796 V |
| $V_{D_2}$ | 2.796 V |
| $V_{Base}$ | 9.7 $\mu$V |
| $V_{out}$ | $\approx$ 0 V |

This concludes the section on circuit development for task 5.

# 3 Experimental Implementation

This section details the experimental implementation of an actively loaded differential amplifier with a common source output, cascoded current mirror and a class B amplifier stage at the output. These also include components for frequency compensation and a load.The power supplies and analysis were implemented using the Digilent Analog Discovery kit. The experimental circuit can be seen Figure 6.

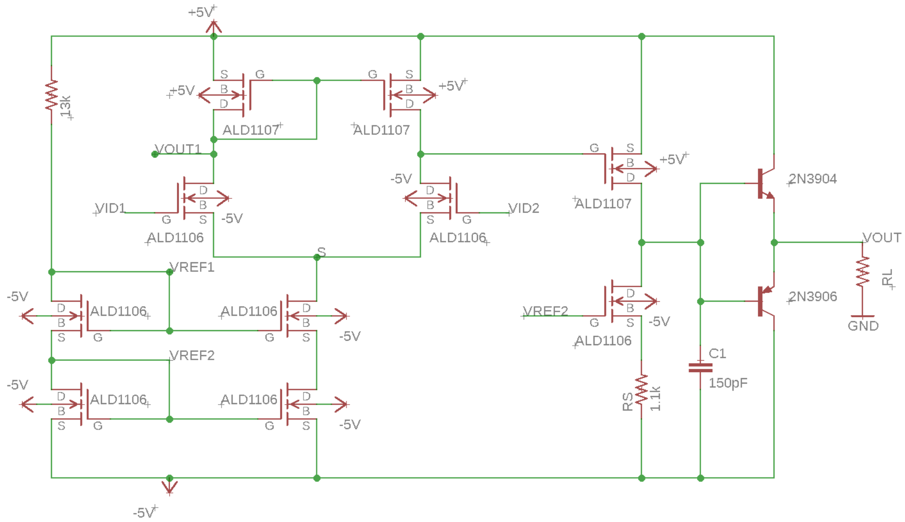



Figure 6: Experimental range of operation

The DC bias conditions were measured using a DT830B DVM. Nodal voltages were measured in reference to ground and current was measured by wiring the DVM in series while in ammeter mode. The bias conditions were measured while both input nodes to the circuit were grounded. The final measured values can be seen in Table 4.

Table 4: Experimental DC values

| **DC Bias Conditions** | |
|---|---|
| $V_{Ref_1}$ | -3.01 V |
| $V_{Ref_2}$ | -403 mV |
| D1 | 2.82 V |
| D2 | 2.84 V |
| S | 2 V |
| OutCS | .09mV |
| $I_{Ref}$ | 387 $\mu$A |
| $I_{D_1}$ | 193.7 $\mu$A |
| $I_{D_2}$ | 194 $\mu$A |
| $I_{CS}$ (CS stage) | 217 $\mu$A |
| $I_C$ Collector | 2.23 $\mu$A |

Notably, the voltage at the "OutCS" node should be zero. In the default state, the offset at that node was measured to be 2.5V. A potentiometer was used as the source degeneration resistance for the common source amplifier. This pot was varied until the offset was nulled out and the final resistance value required was found to be 1.1kΩ. The range of operation for the circuit can be seen in Figure 7.

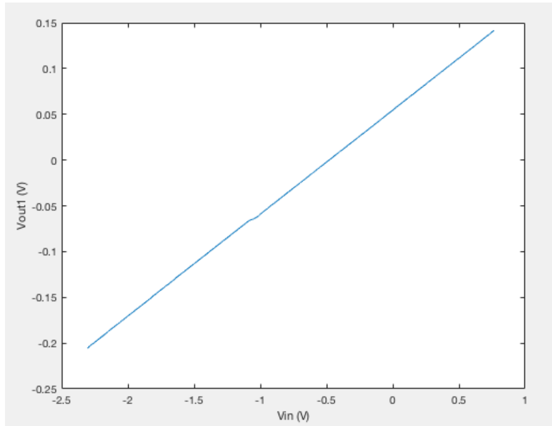
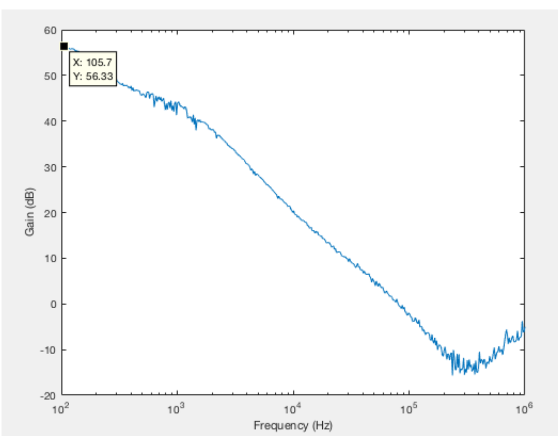
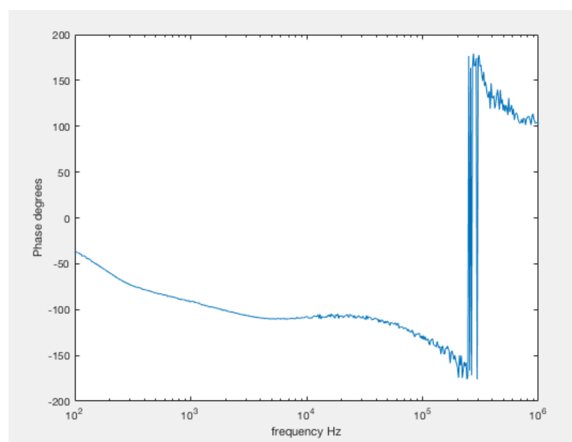



Figure 7: Experimental range of operation

The range of operation is extremely narrow. This, however, is expected due to the limits imposed by the use of a cascode current mirror. The cascode affords more gain at the expense of voltage range. This was explored in more depth in Task 3. In order to prevent the op amp from saturating, a 1000:1 voltage divider was added at the signal input. The channel 1 probe was connected after the voltage divider to compensate for the 60dB drop from the voltage divider. Channel 2 was connected at the final output of the operational amplifier.




(a) Gain of loaded amplifier

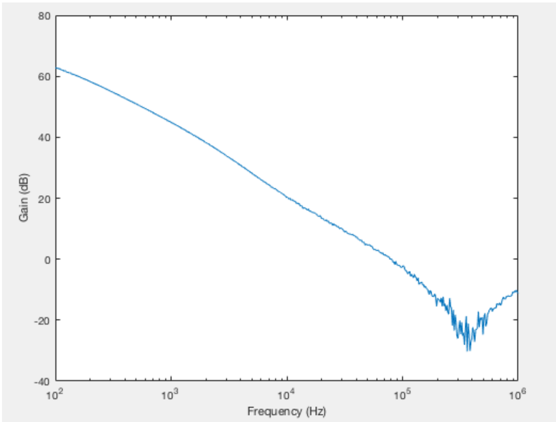



(b) Phase plot of loaded amplifier

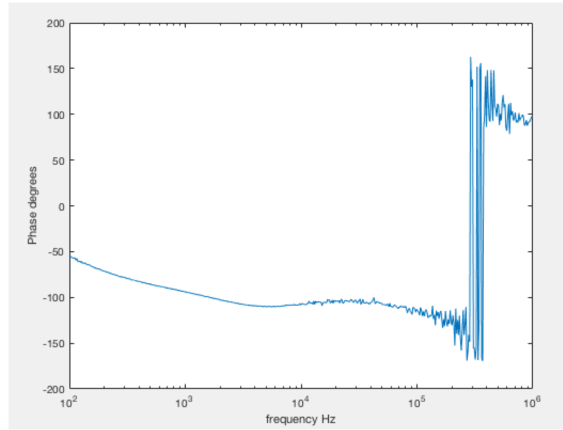
Figure 8: Gain and phase of loaded amplifier

Figure 8 shows the gain vs frequency as well as the phase vs frequency plots of the loaded op amp, the loaded op amp is stable past the required 150kHz mark and demonstrates the loaded gain to be 56.33 dB.

Figure 9 below shows the same op amp as Figure 8 but with frequency compensation applied to ensure the amplifier is unity gain stable at the desired frequencies.



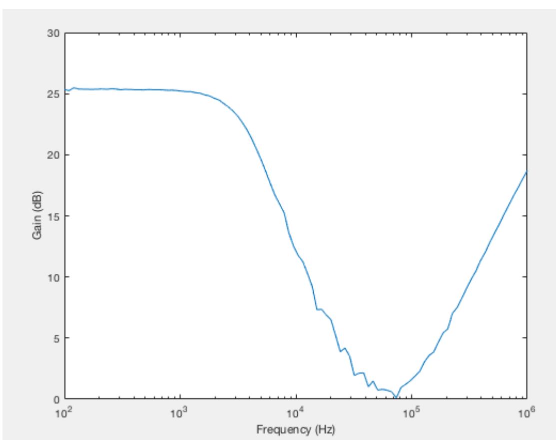

(a) Gain plot of loaded amplifier and frequency compensation



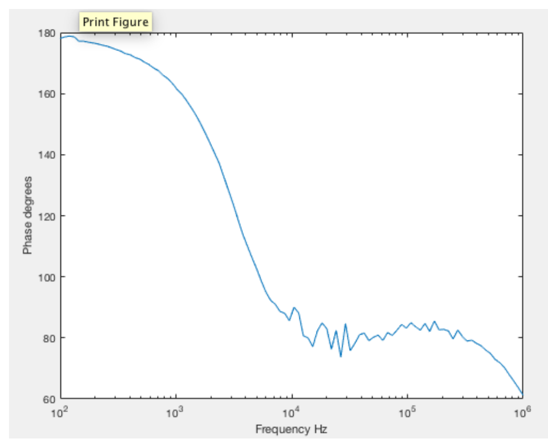

(b) Phase plot of loaded amplifier with frequency compensation

Figure 9: Gain and phase of loaded amplifier with frequency compensation

Below in Figure 10 are the gain and phase plots of the inverting amplifier. The plots show the desired outputs from this op amp.



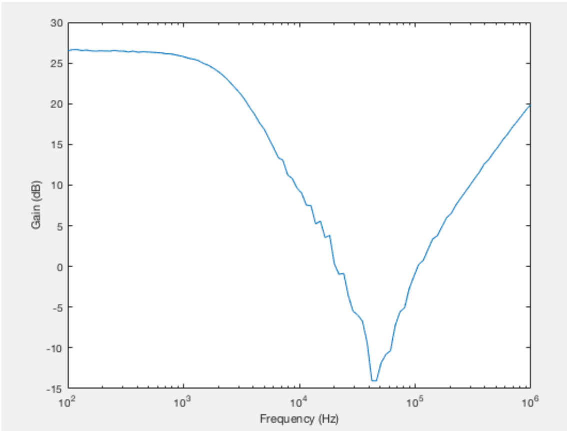

(a) Gain of inverting amplifier



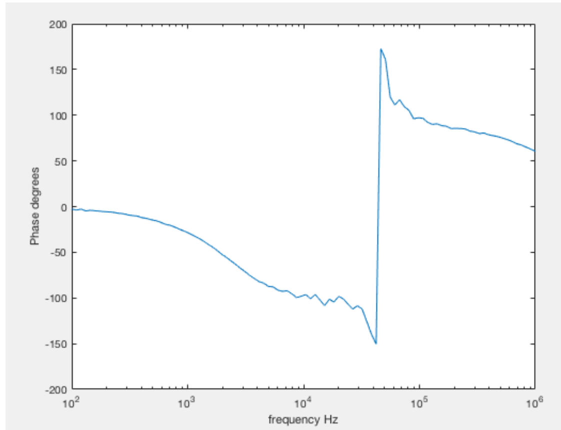

(b) Phase plot of inverting amplifier

Figure 10: Gain and phase of inverting amplifier

Figure 11 shows the non inverting op amp's gain and phase plots, notably the phase plot shows the desired 180 degree phase shift that one would expect.




(a) Gain of non-inverting amplifier




(b) Phase plot of non-inverting amplifier

Figure 11: Gain and phase of inverting amplifier

The total harmonic distortion (THD) is shown below in Figure 12 and appears to be minimal for the op amp designed.

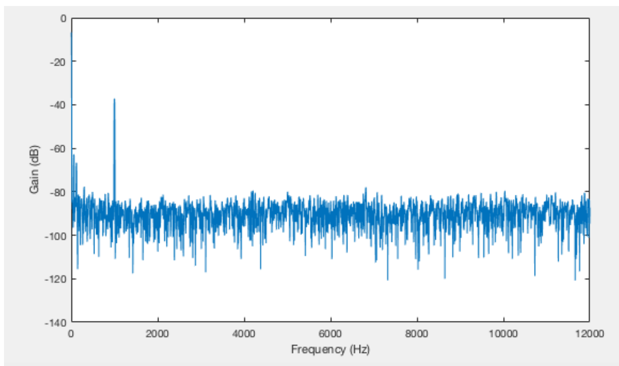



Figure 12: Harmonic spectrum of amplifier

# 4 Discussion

After several minor changes, the op amp operated correctly. This lab served as introduction to feedback applications of operational amplifeirs. The two types of feedback were explored. The specifications are outlined in Table 5.

Table 5: Current and voltage values from simulated vs experimental circuit

| Simulated current values | | |
|---|---|---|
| **DC Bias Conditions** | Simulated | Experimental |
| $V_{Ref_2}$ | -340 mV | -403 mV |
| $V_{Ref_1}$ | -2.987 V | -3.01 V |
| $V_{D_1}$ | 2.796 V | 2.82 V |
| $V_{D_2}$ | 2.796 V | 2.84 V |
| $V_{out}$ | $\approx$ 0 V | .09mV |
| $I_{Ref}$ | 410.8 $\mu$A | 387 $\mu$A |
| $I_{D_1}$ | 204.4 $\mu$A | 193.7 $\mu$A |
| $I_{D_2}$ | 204.4 $\mu$A | 194 $\mu$A |
| $I_{CS}$ | $\approx$ 227 $\mu$A | 217 $\mu$A |
| $I_C$ | $\approx$ 2 $\mu$A | 2.23 $\mu$A |

The final circuits fell well within specifications and operated correctly after minor component alterations.

# 5 Conclusion

The design, simulation, and construction of experiments to measure the performance of feedback to the op amp. The gain was measured at 63.3 dB while unloaded. The smallest value for the load resistor which caused a 3 dB drop in gain was found to be 500 Ω, with a gain measured at 66.33 dB. The unity gain uncompensated unity gain frequency was measured at 170 kHz. This circuit will help the circuit achieve and maintain stability of the operational amplifier in task 6. An important lesson learned during this lab was that achieving a gain too high over specification is not helpful when trying to measure values and achieving stability, which is as important as the final gain value.

# References

[1] D.E. Kotecki Lab.(2017) Lab #5 Voltage Amplifier [Online]. Available: http://davidkotecki.com/ECE342/labs/ECE342_2017_Lab5.pdf

[2] ON Semiconductor. (2017) 2N7000 [Online]. Available: http://www.onsemi.com/PowerSolutions/supportDoc.do?type=models&rpn=2N7000