Task 5: Voltage Amplifier

Optical Uplink

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Abstract

The design, simulation and construction of an amplifier circuit are described. In task 5 of the optical uplink project, a voltage amplifier will increase the signal from the active bandpass filter from a low voltage range, possibly in mV, to 5V. Two ways are explored to accomplish this task. The first is using a common source NMOS circuit. The second is using a NPN BJT common emitter circuit.

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1 Introduction

This report describes design, implementation and test of two voltage amplifiers. One consisting of negative metal oxide semconducting field effect transistors (NMOS). The other comprised of bipolar junction transistors. Figure 1 demonstrates where in the optical uplink project the voltage amplifier is placed.

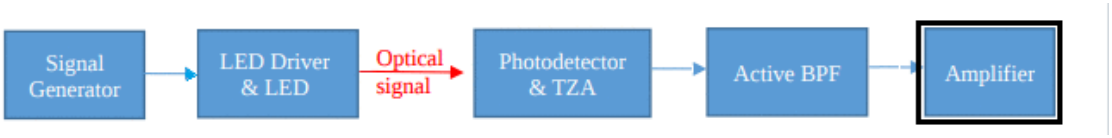

Figure 1: Block diagram for optical uplink [1]

The voltage amplifier is required by the optical uplink project. The output signal from the multi-feedback bandpass filter (MFBP) is in the hundreds of millivolt range. In order to make a more easily detectable signal, a voltage amplifier is required. This can achieved through the use of either a common source or common emitter amplifier. The specifications for this lab are summarized in Table 1.

Table 1: Voltage amplifier specifications

Specifications	Required
Peak gain, with load	21 dB ± 1dB%
Bias current for N_1	1mA
Lower cut-off frequency	≥100 mA
Upper cut-off frequency	at least 200 kHz
R_in, small signal	at least 1 MΩ
R_out, small signal	at least 3 kΩ
$2^(nd)$ Harmonic distortion @ 1kHz	¡2%
Supply voltages	±12 V

The voltage amplifier circuit receives the voltage signal from the MFBP and increases the amplitude of the voltage wavefrom. The desired final output being 5 V. This is achieved with either the use of a NMOS common source amplifier or an NPN BJT common emitter amplifier.

Section 2 of this report describes the design and simulations of the common source amplifier and the common emitter amplifier. Experimental results are addressed in section 3. A discussion of the results, sources of error, and areas of possible improvement are outlined in section 4. Section 5 concludes this report.

2 Circuit Development

This section covers the design choices associated with the various circuits constructed. Both a NMOS common source amplifier and BJT common emitter amplifier. Only the NMOS circuit required design choices as the BJT component values were provided as part of the lab.

The order in which the circuits are discussed is as follows: first the NMOS amplifier followed by the BJT amplifier.

2.1 NMOS common source

The NMOS common source amplifer for this lab was constructed using 2N7000 NMOS transistors. The circuit essentially consists of two parts, the voltage amplifier stage and the current mirror. The generic circuit for the current driver is shown in Figure 2.

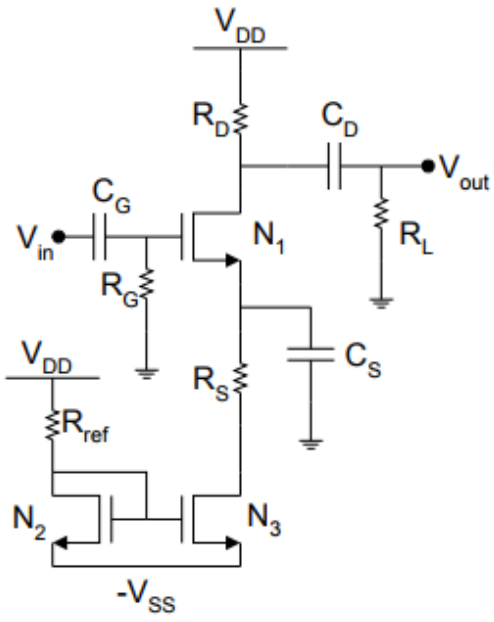

Figure 2: Generic common source amplifier circuit [1]

In order to understand the operation of the circuit, DC analysis of the circuit is required. At DC all the capacitors behave as shorts. It is known that the current through a MOSFET is seen in Equation 1

$$I_D = k(V_{gs} - V_t)^2, \tag{1}$$

Where k is the transconductance parameter, V_{gs} is the gate-source voltage and V_T is the threshold voltage. From the datasheet [2], I_D is 75 mA when V_{gs} is 4.5 V. From Equation 1 k can be found to be 8.5 mA/V. Again using Equation 1, the corresponding V_{gs} for a bias current of 1 mA is found to be 1.85 V. Upon finding the voltage drop over the NMOS, the source resistance can then be found by KCL across the amplifier NMOS. R_s is found to be 8.3 kΩ, R_{ref} can found to be 22.2 kΩ. The capacitor values are chosen such that their impendence is less than their corresponding resistor values. The impendence of the capacitor can be found by Equation 2

$$Z_c = \frac{1}{j\omega C}, \tag{2}$$

where ω is the angular frequency of the input signal in rad/s. By setting Z_c to be less than the corresponding R values, C can be solved to be 4.7 μF.

AC analysis of the circuit is then required in order to find the drain resistance. Figure 3 shows the equivalent small signal model for the NMOS.

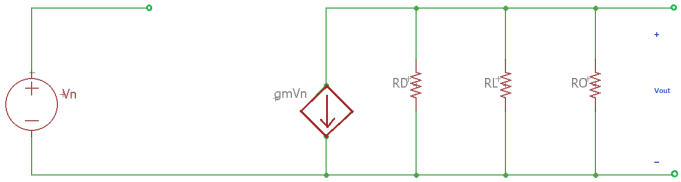

Figure 3: Equivalent small signal circuit

The transconductance of this circuit is defined as Equation 3

$$g_m = \frac{2I_D}{V_{ov}}, \tag{3}$$

where V_{ov} is the overdrive voltage. From this small signal transconductance is found to be 2.8 mA. The small signal r_0, defined as Equation 4

$$r_o = \frac{1}{\lambda I_{DS}}, \tag{4}$$

where λ is the body effect, and found from the datasheet [2] to be zero for the operating conditions. The open circuit gain can then be found by Equation 5

$$\frac{v_o}{v_{in}} = g_m R_o, \tag{5}$$

where R_o is the equivalent resistance of (R_D —— R_L). The load resistance is provided by the lab, but for this calculation can be assumed to nearly infinite, therefore R_D is found to be around 2 kΩ. The circuit was then simulated in NGSpice integrated with Matlab. The simulated circuit can be seen in Figure 4.

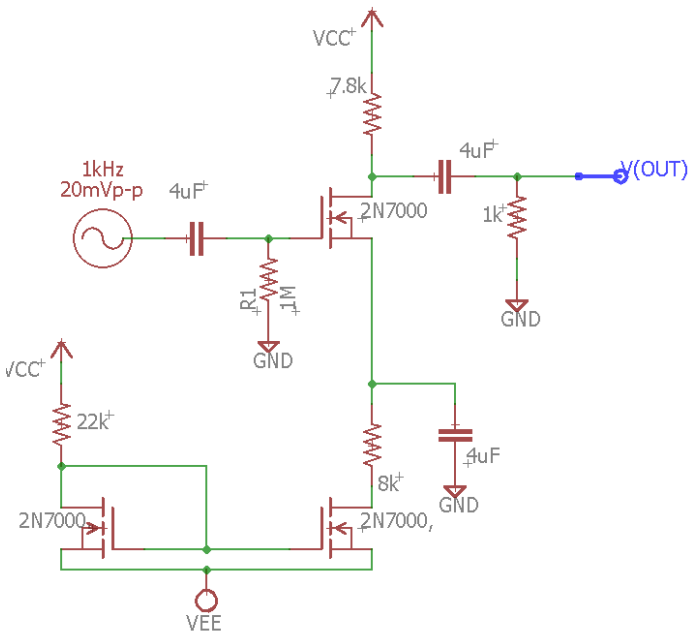

Figure 4: Simulated common source amplifier circuit

A significant change was required in order to meet specs, the R_D value calculated was off by a factor of 4. This is due to assumptions made during analysis, more detail is provided in discussion. In addition, the negative bias voltage was altered to -8 V in order to reduce harmonic distortion. The frequency of the NMOS is shown in Figure 5.

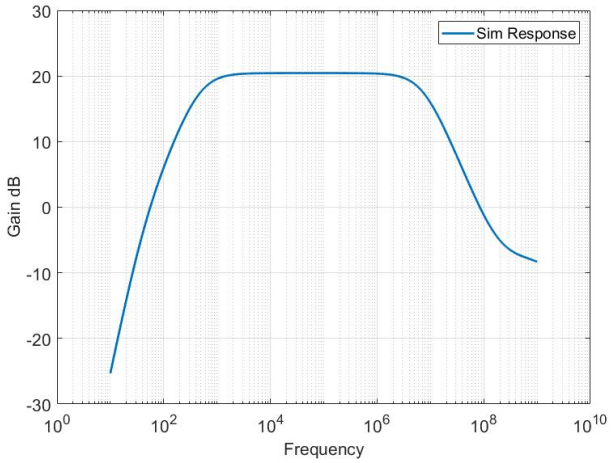

Figure 5: Simulated frequency response of NMOS amplifier

The NMOS met the specified gain at 21 dB with a 3dB lower cut off frequency well below the required 1 kHz. The FFT of NMOS can be seen in Figure 11.

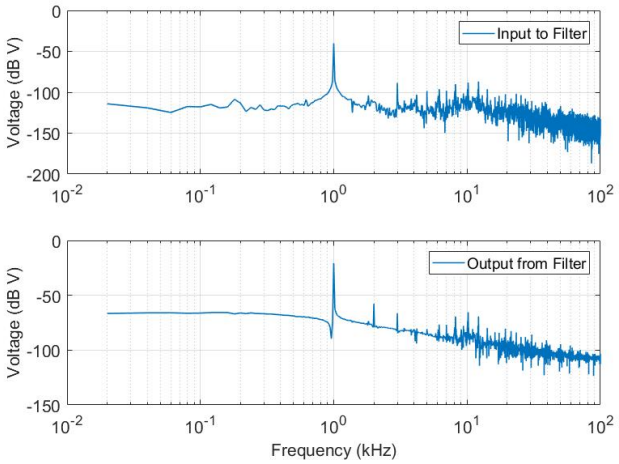

Figure 6: Simulated FFT of second harmonic distortion

This analysis was performed by inputting a 10 mV signal at 1 kHz. The measured distortion on the second harmonic is required to be less than 2%. By inspection the distortion is found to be 1.5%. Table 2 summarizes the NMOS simulation results.

Table 2: NMOS summary

Q_1, Q_2, Q_3	2N7000
R_ref	19.3 kΩ
R_D	7.8 kΩ
R_S	8 kΩ
R_G	1 MΩ
C_g, C_d, C_l	4.7 μF
Lower cutoff	500 Hz
Upper cutoff	10 MHz

After making slight alterations the circuit worked correctly in simulations.

2.2 BJT common emitter

The BJT operates similarly to the NMOS circuit. The difference being it is now an NPN transistor and is therefore a current controlled voltage source, as opposed to the NMOS which is a voltage controlled. The values for the BJT circuit were not solved for, but instead provided as part of the lab, which can be seen in Table **??**

Table 3: BJT experimental values

Q_1, Q_2, Q_3	2N3904
R_ref	19.3kΩ
R_C	4.7kΩ
R_B	10kΩ
R_E	3.3kΩ
R_L	1kΩ
C_B, C_C, C_E	500nF
Gain	30db
Lower cutoff	3 kHz
Upper cutoff	100 MHz

The simulations of the BJT follow and were performed in Matlab integrated with NGspice. The frequency response of the circuit can be seen in Figure **??**.

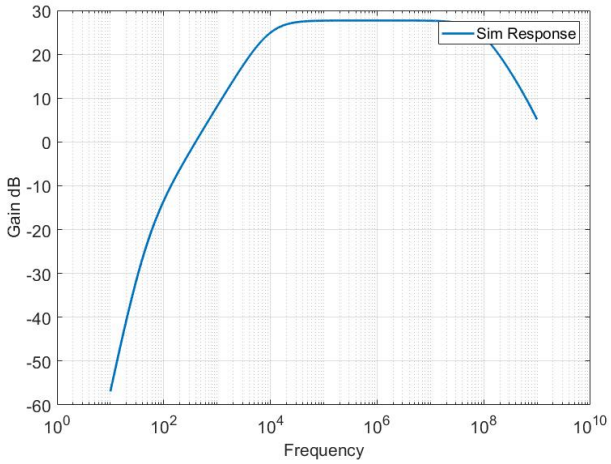

Figure 7: Simulated frequency response of BJT

Notably, the 3dB lower cutoff is greater than 1 kHz. The corresponding passband gain is significantly higher than 20 dB. This is not ideal, because the output could begin to saturate due to excessive gain. The FFT of the BJT can be seen in Figure **??**

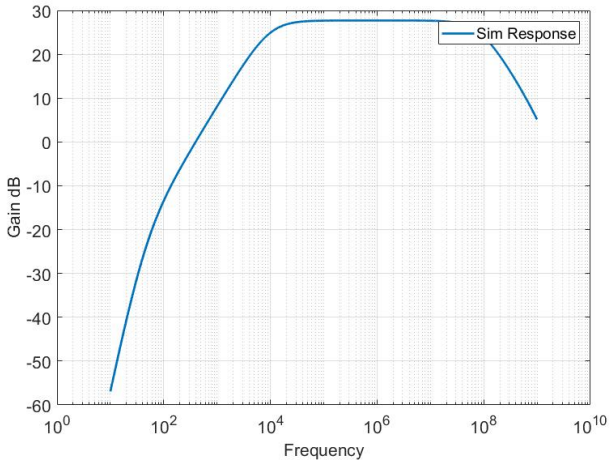

Figure 8: Simulated FFT BJT circuit

The BJT achieved a far smaller second harmonic distortion than the NMOS, with only a .25% distortion for the 2 kHz harmonic.

2.3 Simulated summary

The final simulated circuit is shown in Figure **??**.

The simulated circuit did require any changes from calculations. One of the most significant margins of error for simulations is that the operation of the simulations is quite dependent on which simulation model for the 2N3904 is used. The "SP3" model from ON Semiconductor was utilized for these simulations [**?**]. Different models are capable of behaving in unexpected ways due to their interaction with the NGSpice simulation software. The summary of simulated results from this circuit is shown in Table 4.

Table 4: Simulated Results

Component	Simulated Values
Conditioned Voltage	5V
Conditioned Frequency	20kHz
Conditioned Duty-Cycle	48%
Output Current	200mA
R_{sense}	12Ω

The simulated signal conditioner outputted only a 48% duty-cycle directly and is slightly less than the required 50%. However, the final waveform through the LED operated with a 50% duty-cycle as required by specifications. The simulated circuit operated as expected and provided enough current in order to drive the LED. The resulting waveform through the LED is the correct frequency and duty-cycle.

3 Experimental Implementation

The circuits required only minor changes from simulation to experimental implementation.

3.1 NMOS amplifier

The final circuit is shown in Figure **??**.

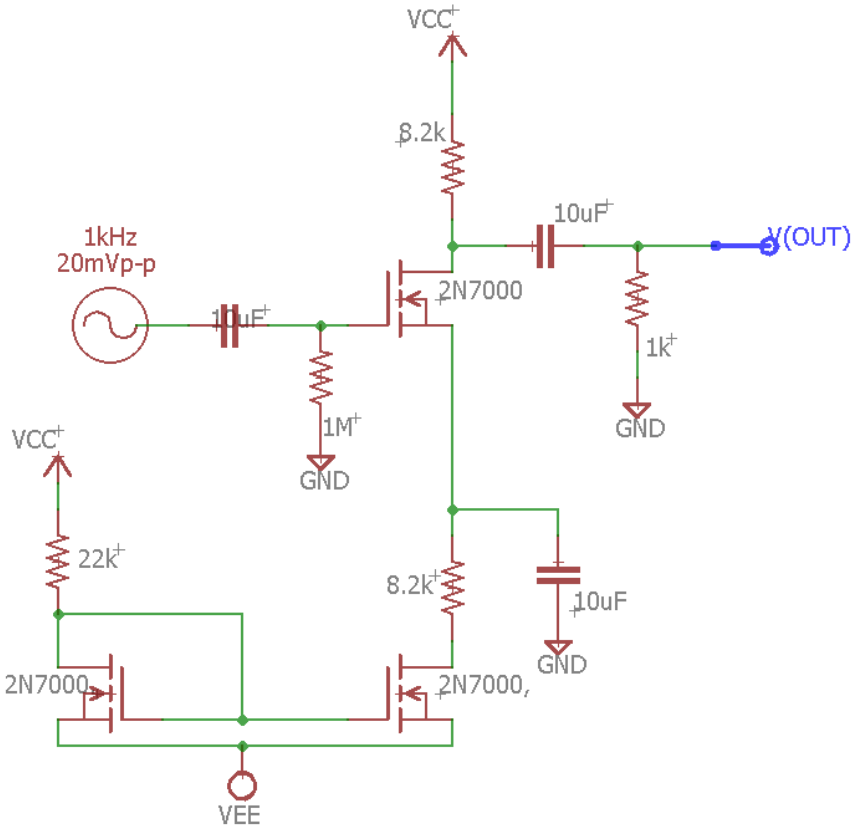

Figure 9: NMOS final circuit schematic

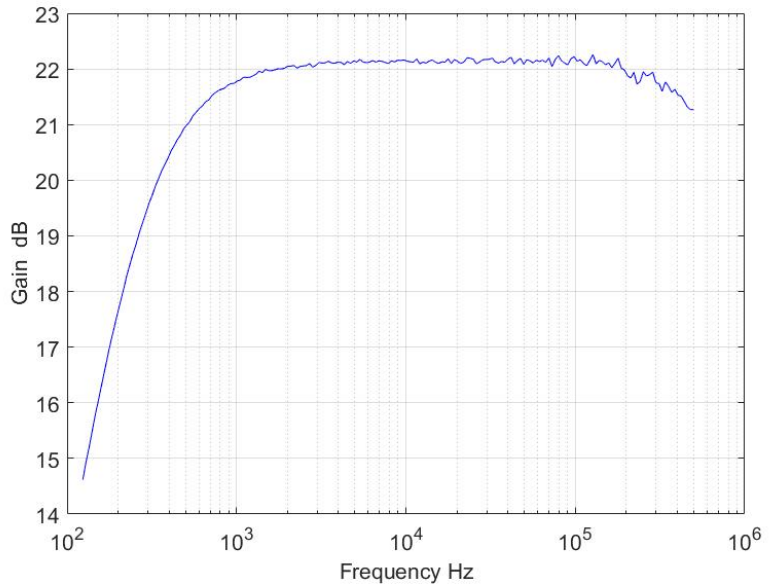

Figure 10: NMOS experimental frequency response

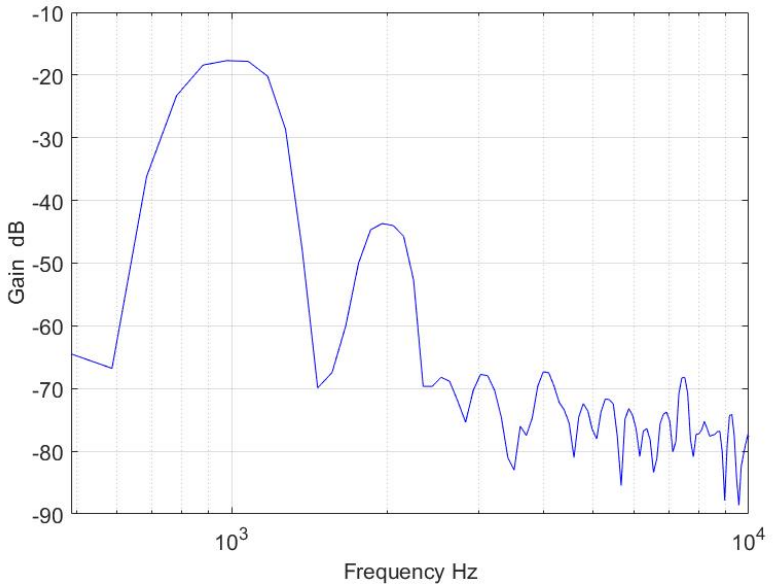

Figure 11: NMOS experimental FFT

Table 5: NMOS experimental values

Q_1, Q_2, Q_3	2N7000
R_ref	22 kΩ
R_g	1 MΩ
R_d	8.2 kΩ
R_s	8.2 kΩ
R_L	1kΩ
C_B, C_C, C_E	10 μF

3.2 BJT amplifier

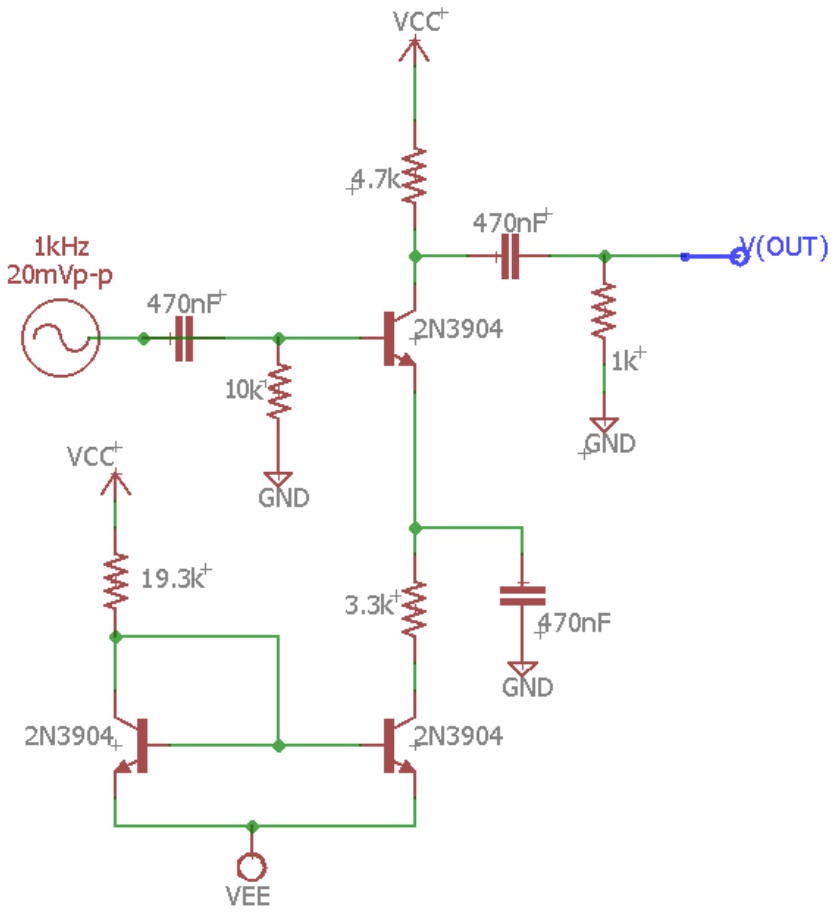

Figure 12: BJT final schematic

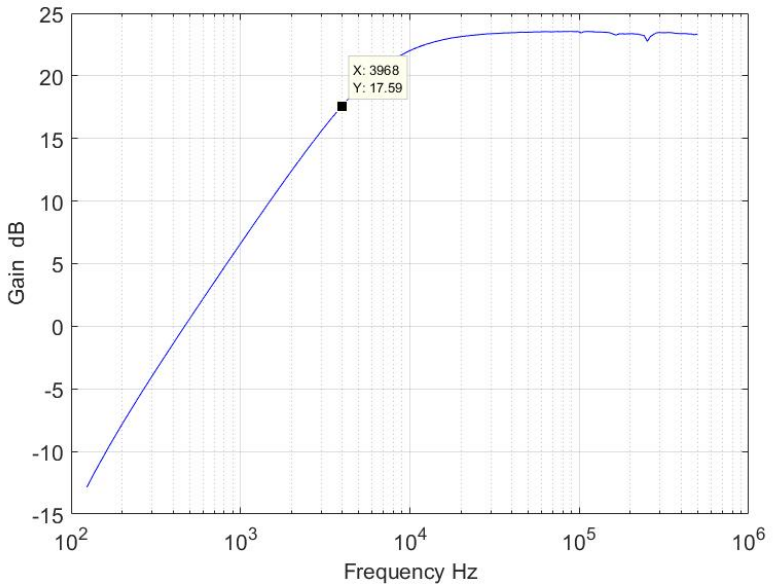

Figure 13: BJT experimental frequency response

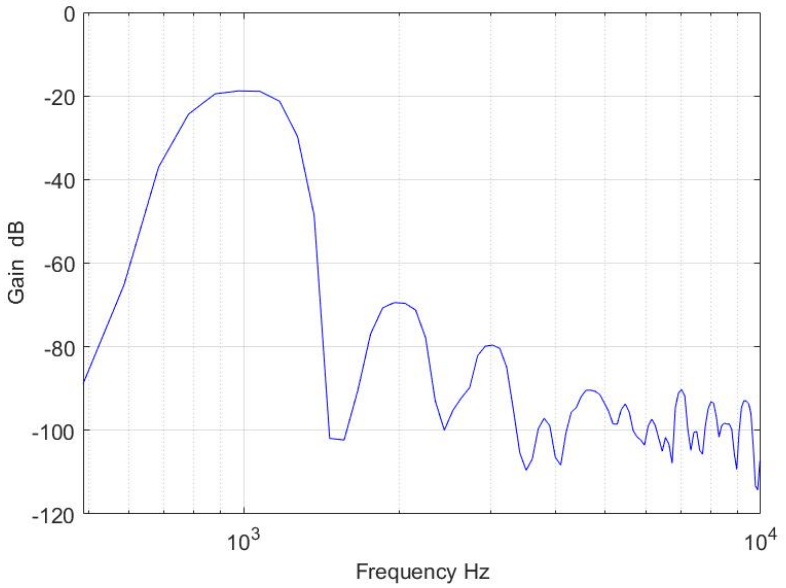

Figure 14: BJT experimental FFT

Table 6: BJT experimental values

Q_1, Q_2, Q_3	2N3904
R_ref	19.3kΩ
R_C	4.7kΩ
R_B	10kΩ
R_E	3.3kΩ
R_L	1kΩ
C_B, C_C, C_E	470nF

In order to meet specifications, several minor changes to all circuits were made. The individual changes are discussed in their respective subsection as follows, the signal conditioner then the current driver.

4 Discussion

After several minor changes, the circuit operated correctly. This lab served as introduction to circuits that include both transistors and op amps. The two types of components have been studied separately, but never in conjunction. The specifications are outlined in Table **??**.

Table 7: BJT and NMOS comparison

BJT	Values	NMOS	Values
Q_1, Q_2, Q_3	2N3904	N_1, N_2, N_3	2N7000
R_ref	19.3kΩ	R_Ref	22kΩ
R_C	4.7kΩ	R_D	8.2kΩ
R_B	10kΩ	R_G	1MΩ
R_E	3.3kΩ	R_S	8.2kΩ
R_L	1kΩ	R_L	1kΩ
C_B, C_C, C_E	470nF	C_G, C_S, C_D	10μF

Notably, the ring oscillator had to have the its output frequency increased. This was due, in part, because of parasitic inductances and capacitances from the board and jumper wires. The propagation of the signal from the oscillator to output resulted in a decrease of frequency. Therefore, increasing the input frequency resulted in a correct output of the LED driver.

Another factor that determined the operating frequency is the fact that most of the components are temperature dependent. The MCP6004 IC, with increasing temperature, has an increased frequency output. The voltage regulator's efficiency, however, decreases with increasing temperature. The current through the LED is also a function of temperature. The behavior of this circuit can be heavily dependent on ambient temperature. This is a vital stipulation as, depending on the bandwidth of the MFBP filter designed before, the LED signal may fall inside the stopband of the MFBP filter. The receiver would then fail to receive the LED signal and the optical uplink would not operate. The summary of the final results can be seen in Table 8.

Table 8: Simulated vs. experimental results

Component Values	Simulated	Experimental
Output Current	200mA	150mA
Output Frequency	20kHz	20.1kHz
Output Duty-cycle	48%	50.1%

The final circuit fell well within specifications and operated correctly after several component alterations.

5 Conclusion

The design, simulation, and implementation of the LED driver have been explained. Lab specification required that the signal generator have a frequency of approximately 20kHz, a duty-cycle of approximately 50%, and an amplitude of at least 100mA. The LED driver takes a sinuisoidal waveform of variable duty-cycle and outputs a 50% durt-cycle square wave. The waveform is then converted to a suffeciently large driving current by the current driver. The LED driver was constructed using the following parts: a 10kΩ, 100kΩ, 470Ω, 1kΩ, 12Ω and a 10kΩ potentiometer; a MCP6004 quadrature operation amplifier; an IR1503 LED; and finally a 2N3904 BJT. A 9V battery supply is stepped down to 5V with an LM7805 voltage regulator. The frequency was 20.1kHz, with a duty-cycle of 50.1%, and an amplitude of 150mA. An important lesson about the behavior circuits including both op amps and transistors was learned. The meshing of op amps and transistors provide novel solutions to real world problems

References

[1] D.E. Kotecki Lab.(2017) Lab #5 Voltage Amplifier [Online]. Available: http://davidkotecki.com/ECE342/labs/ECE342_2017_Lab5.pdf

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