

Task 5: Feedback and Stability

Operational Amplifier

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Abstract

The design, simulation and construction of a differential amplifier circuit (developed in Task 4) with feedback is described. In this task a multistage op-amp with a class B output amplifier will be developed, simulated and constructed. The required open loop voltage gain for this circuit is at least 46 dB. The uncompensated unity gain is required to be larger than 150 kHz. The gain was measured at 60 dB while unloaded. The smallest value for the load resistor which caused a 3 dB drop in gain was found to be $500\ \Omega$, with a gain measured at 56.33 dB. The amplifier with compensation was unity gain stable until 170kHz. The op amp while in inverting configuration produced a gain of -19.9 V/V with a total harmonic distortion of 1.41% while the non-inverting produced a gain 21.5 V/V.

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1 Introduction

This report describes the design, construction, and analysis of negative feedback for an operational amplifier. This is achieved using resistors attached to and across certain nodes in the op amp in Figure 1.

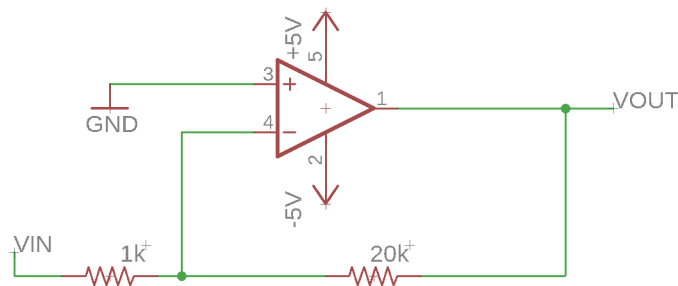


Figure 1: Sample experimental circuit demonstrating feedback

Operational amplifiers serve an integral building block for modern electronics. Op amps provide large gain with various configuration schema. This allows the circuit designer to use the op amp in different topologies and achieve different results, all without modifying the op amp circuit itself. In addition, an op amp provides significant gain while maintaining stability, this is where the output stage comes in. The output stage allows design to accommodate for non-controllable factors such as transistor mismatch and temperature variation. The objective of this lab is to apply feedback to the op amp so that the op amp achieves the specifications as seen in Table 1.

Table 1: Task 5 Specifications

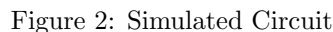
Specifications	
Power	$\pm 5\text{V}$
Output Stage	$\geq 500\Omega$
Bias Current	$400\ \mu\text{A}$
Overall Voltage Gain	$\geq 200\text{V/V}$ (46 dB)
CMRR	$\geq 60\text{dB}$
Output Voltage Swing	$\geq \pm 2\text{V}$

Section 2 of this report describes the design, and when relevant, the simulations of the experiments. Experimental results and implementation are addressed in Section 3, including reasoning as to why a different circuit than the one outlined previously was constructed. A discussion of the results, sources of error, and areas of possible improvement are outlined in Section 4. Section 5 concludes this report.

2 Circuit Development

This section covers the design choices associated with the actively loaded differential amplifier with cascoded current mirror and a class B amplifier for an output stage. Frequency compensation will also be

The circuit that was developed in Task 4 will be used for the purposes of this circuit development section. The output stage will be added in this task which will be a class B amplifier. The class B amplifier will consist of a 2n3904 NPN BJT and a 2n3906 PNP BJT. The simulations were conducted in Microcap 10. As these schematics are difficult to read, a set of schematics with identical values and components were created in Eagle by Autodesk. The simulated schematic can be seen in Figure 2 below.


$$A_f(j\omega) = \frac{x_o}{x_i} = \frac{A_f(j\omega)}{1 + A_f(j\omega)\beta} \quad (1)$$

The output of the amplifier met the specifications as it was simulated to have a 63.3 dB gain. To find the smallest load resistor that the amplifier could drive, Microcap 11 was used to do a sweep of load resistor values from 250 Ω to 2.5 k Ω . The goal is to find the load resistor value that will cause a 3 dB drop from the unloaded gain, which would be 60.3 dB, or at least a value close to that. The result can be seen in Figure 3 below.

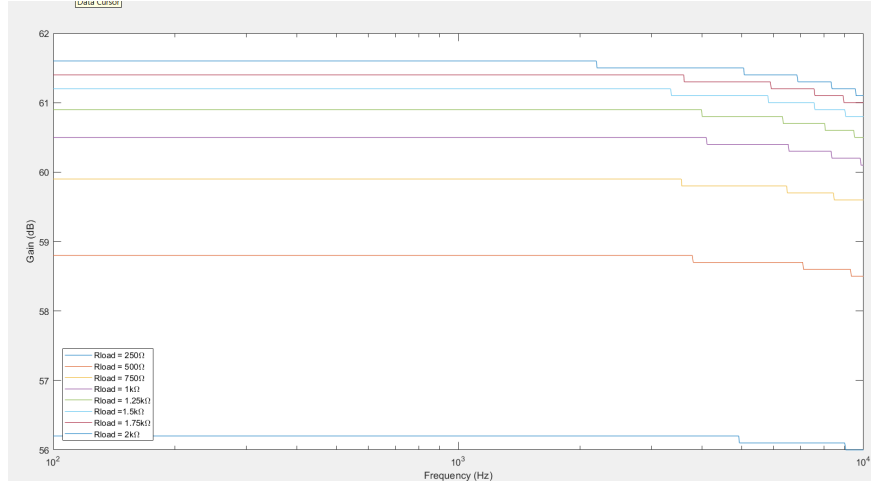


Figure 3: Sweep values of load resistor vs gain

It was found that the load of approximately $900\ \Omega$ caused a 3 dB drop in gain. A load of $500\ \Omega$ caused a 6 dB drop. Therefore, 900 is the smallest load the circuit can drive according to the simulation. Using this value for the load, a simulation was conducted and the resulting data was exported to Matlab to plot. The gain verses frequency plot at a $900\ \Omega$ load resistance is seen below in Figure 4. During this simulation, the capacitor at the collector of the 2n3906 (used for frequency compensation) was found to work at any value below 500 pF.

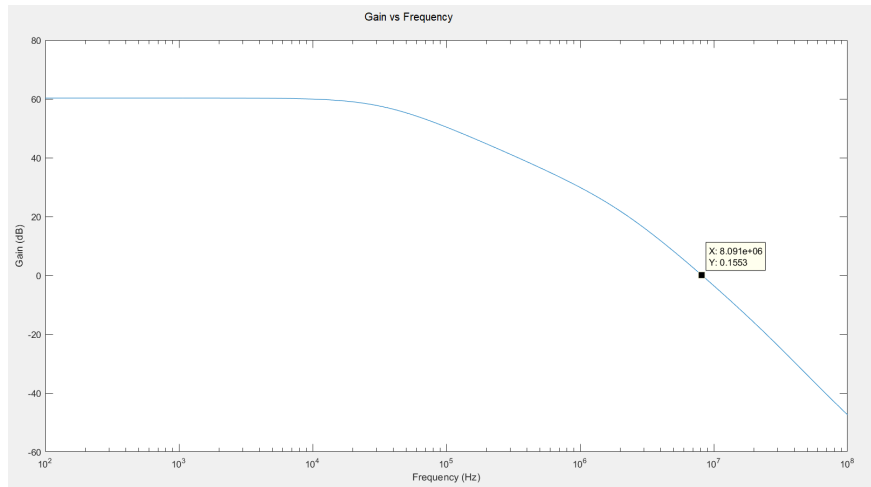


Figure 4: Gain with $900\ \Omega$ load resistance

As seen, the gain is valued at just over 60 dB, which meets the 3 dB drop in gain requirement at $900\ \Omega$ load. The zero crossing for the gain was found to be approximately 8 MHz. In order to be a stable amplifier, the phase shift should not change more than 180 degrees before the zero crossing of the gain. The resultant phase plot from simulations is see in Figure 5 below.

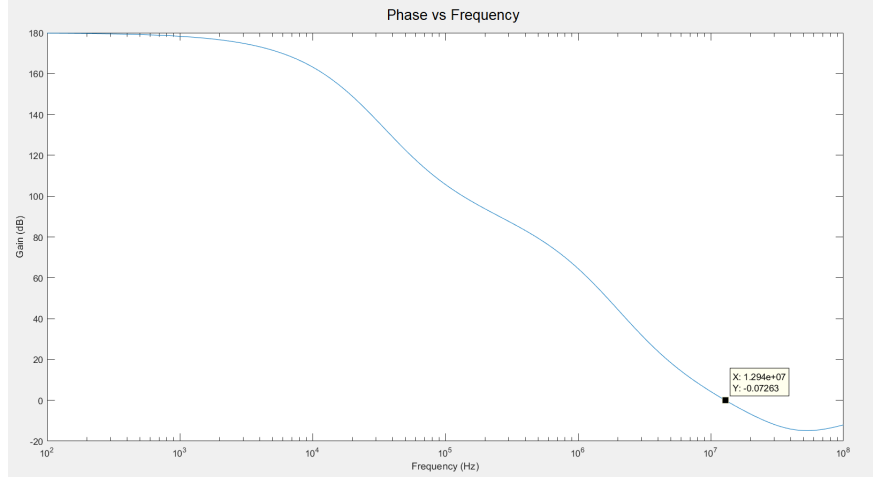


Figure 5: Phase plot with $900\ \Omega$ load resistance

The value for an 180 degree phase shift was found to be approximately 12.9 MHz from the simulations. This is well beyond the required 8.9 MHz found from the plot of the gain in Figure 4. All of the nodal voltages and currents were found during the simulation using dynamic DC analysis in Microcap 11. The current values are shown in Table 2 AC analysis was used in order to simulate the gain and phase.

Table 2: Current values from simulated circuit

Simulated current values	
I_{Ref}	$410.8\ \mu\text{A}$
I_{D_1}	$204.4\ \mu\text{A}$
I_{D_2}	$204.4\ \mu\text{A}$
I_{CS}	$\approx 227\ \mu\text{A}$
I_C	$\approx 2\ \mu\text{A}$

The voltage values are seen in Table 3 below.

Table 3: Current values from simulated circuit

Simulated voltage values	
V_{Ref2}	$-340\ \text{mV}$
V_{Ref1}	$-2.987\ \text{V}$
V_{D_1}	$2.796\ \text{V}$
V_{D_2}	$2.796\ \text{V}$
V_{Base}	$9.7\ \mu\text{V}$
V_{out}	$\approx 0\ \text{V}$

The circuit simulated as expected with the chosen DC bias conditions utilizing a bias current of $400\ \mu\text{A}$.

3 Experimental Implementation

This section details the experimental implementation of an actively loaded differential amplifier with a common source output, cascoded current mirror and a class B amplifier stage at the output. These also include components for frequency compensation and a load. The power supplies and analysis were implemented using the Digilent Analog Discovery kit. The experimental circuit can be seen Figure 6.

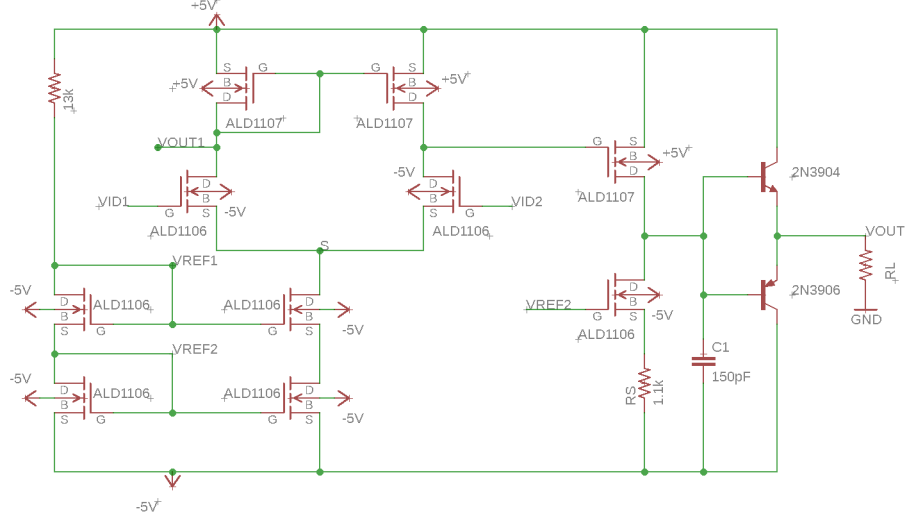


Figure 6: Experimental range of operation

The DC bias conditions were measured using a DT830B DVM. Nodal voltages were measured in reference to ground and current was measured by wiring the DVM in series while in ammeter mode. The bias conditions were measured while both input nodes to the circuit were grounded. The final measured values can be seen in Table 4.

Table 4: Experimental DC values

DC Bias Conditions	
V_{Ref1}	-3.01 V
V_{Ref2}	-403 mV
D1	2.82 V
D2	2.84 V
S	2 V
OutCS	0.09 mV
I_{Ref}	387 μ A
I_{D1}	193.7 μ A
I_{D2}	194 μ A
I_{CS} (CS stage)	217 μ A
I_C Collector	2.23 μ A

Notably, the voltage at the "OutCS" node should be zero. In the default state, the offset at that node was measured to be 2.5V. A potentiometer was used as the source degeneration resistance for the common

source amplifier. This pot was varied until the offset was nulled out and the final resistance value required was found to be $1.1\text{k}\Omega$. The range of operation for the circuit can be seen in Figure 7.

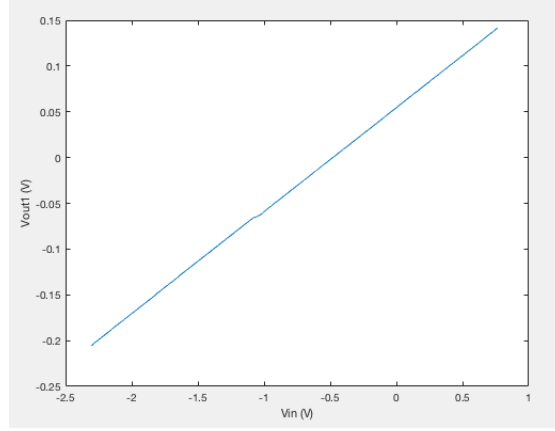
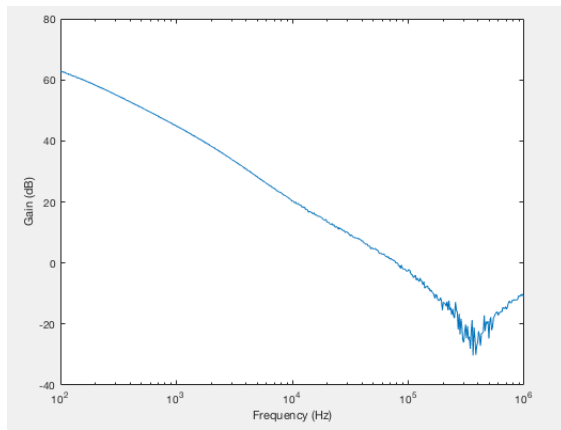
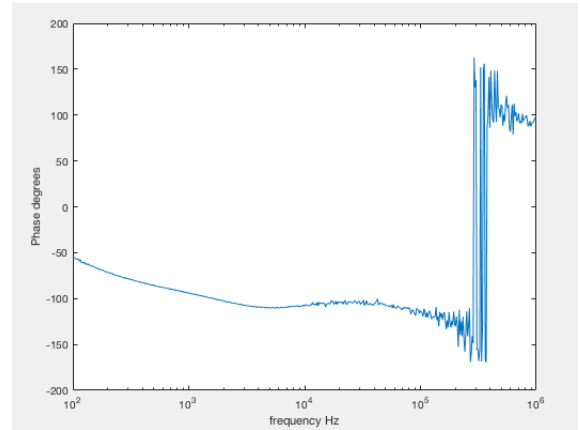


Figure 7: Experimental range of operation

The range of operation is extremely narrow. This, however, is expected due to the limits imposed by the use of a cascode current mirror. The cascode affords more gain at the expense of voltage range. This was explored in more depth in Task 3. In order to prevent the op amp from saturating, a 1000:1 voltage divider was added at the signal input. The channel 1 probe was connected after the voltage divider to compensate for the 60dB drop from the voltage divider. Channel 2 was connected at the final output of the operational amplifier. In order to ensure the op amp was unity gain stable, a 150pF capacitor had to be added to the output node of the common source amplifier stage. Prior to this modification there was no 0 dB gain crossing which meant that op amp was in fact unstable and would oscillate without input. The compensated gain can be seen in Figure 8.



(a) Gain plot of loaded amplifier and frequency compensation



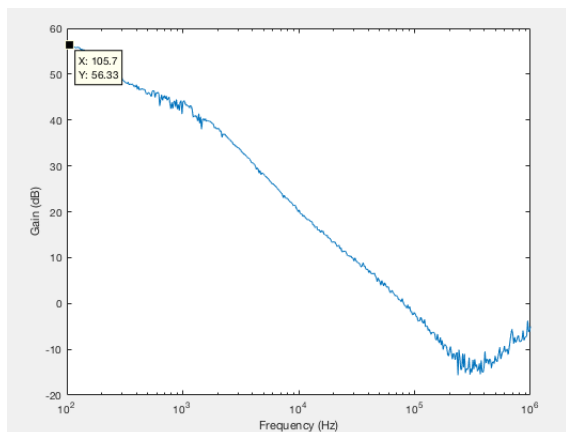
(b) Phase plot of loaded amplifier with frequency compensation

Figure 8: Common mode gain, A_{cm} at 1V

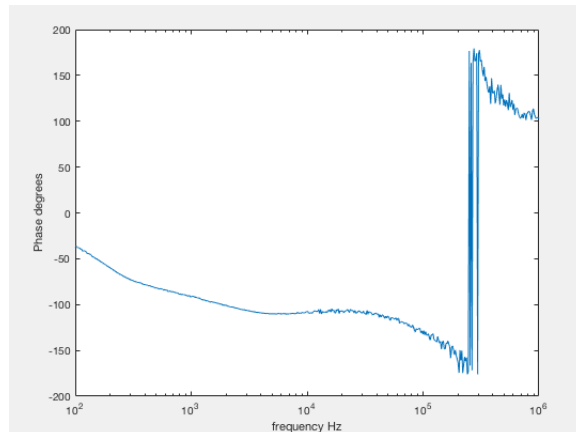
This addition moved the unity gain frequency bandwidth to 170 kHz, which is greater than the required

150kHz. The system is also now stable which allows for the loaded gain to be measured.

Per the requirements of the lab, the op amp should be able to drive a load that is as low as a $500\ \Omega$ load. The loaded gain with a $500\ \Omega$ load can be seen in Figure 9.



(a) Gain of loaded amplifier



(b) Phase plot of loaded amplifier

Figure 9: Loaded gain and phase of open loop configuration

It can be seen that the gain dropped 3.67dB from the unloaded gain of 60dB. This is slightly out of spec and can be compensated by using an only slightly larger load of $600\ \Omega$. The op amp did, however, remain stable with the added load. The spectrum from DC to 12 kHz can be seen in Figure 10.

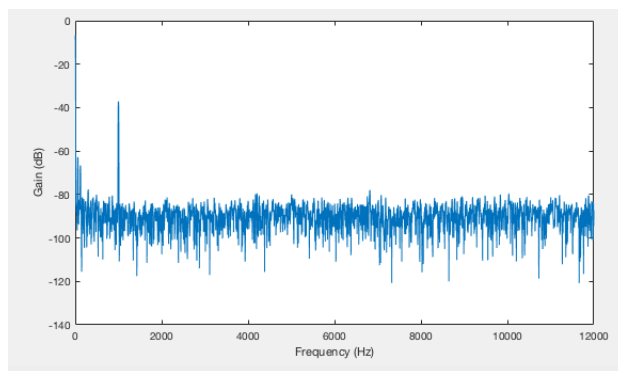


Figure 10: Harmonic spectrum of open loop amplifier

The op amp was then required to be constructed in two different configurations. One in the inverting configuration and the other in the non-inverting. The experimental schematic for the inverting can be seen in Figure 11.

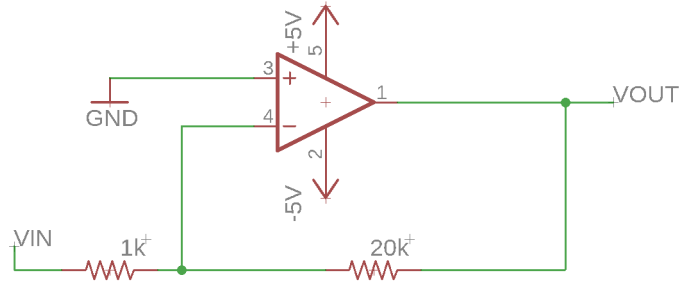
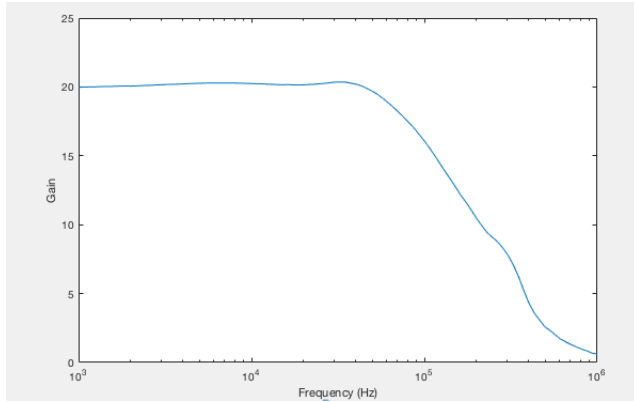
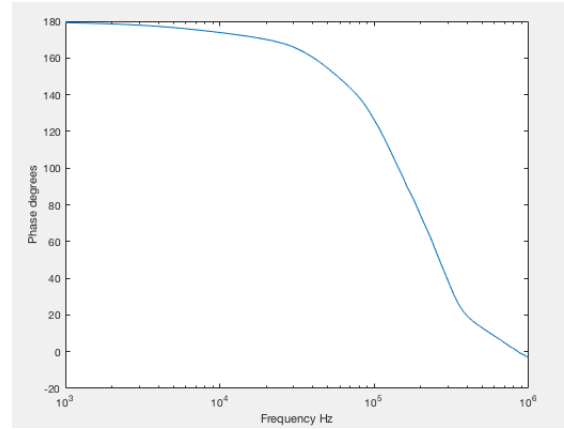


Figure 11: Schematic of inverting amplifier

The op amp shown is the op amp designed in prior in Task 4. The ideal gain was is -20 V/V . The measured gain can be seen in Figure 12.



(a) Gain of inverting amplifier



(b) Phase plot of inverting amplifier

Figure 12: Inverting gain and phase

The gain can be seen to be 20 V/V . It should be noted that the negative sign of this measurement comes from the fact that the phase plot starts at 180° phase. Notably, this configuration seems to have driven the op amp back into instability with the disappearance of the 0dB crossing. The 3dB point for this topology is 90kHz. The spectrum plot for the inverting configuration can be seen in Figure 13.

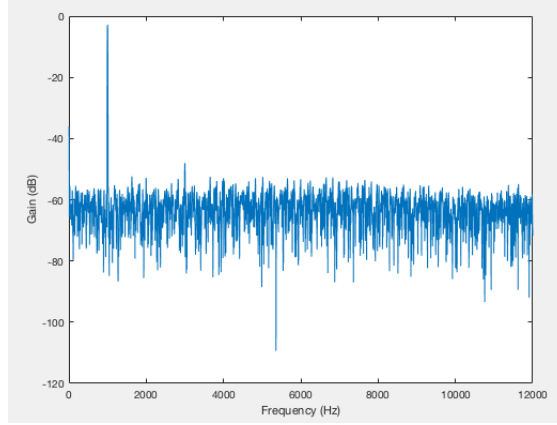


Figure 13: Harmonic spectrum of inverting amplifier

This was generated by inputting a 100mV_{pp} signal at 1kHz . The second harmonic was undiscernable with only the 1kHz having any meaningful amplitude. The total harmonic distortion was calculated in Matlab and was found to be 1.41% . Finally op amp was configured for non inverting output. This topology can be seen in Figure 14

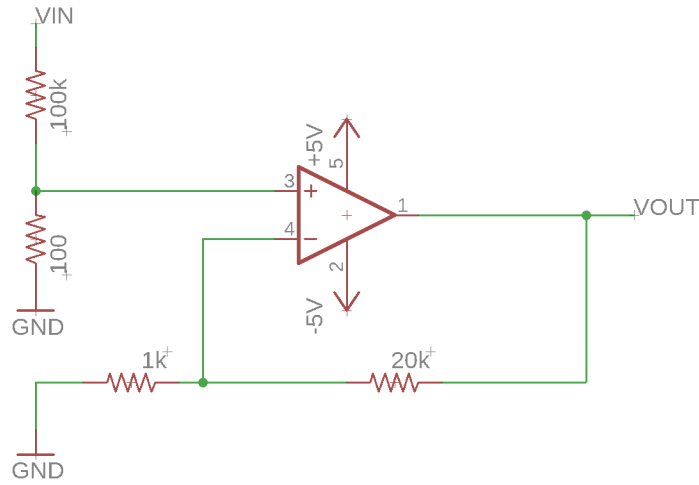
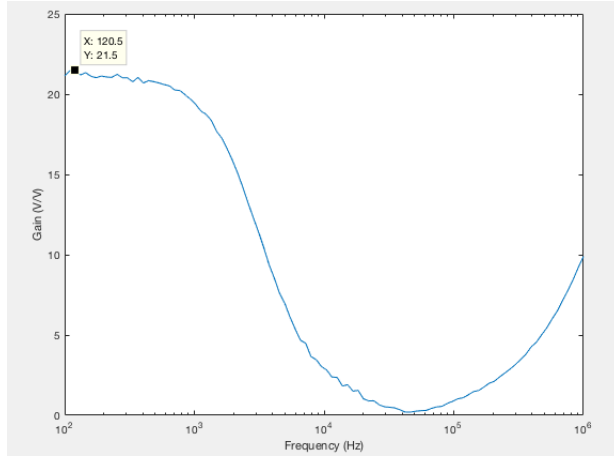
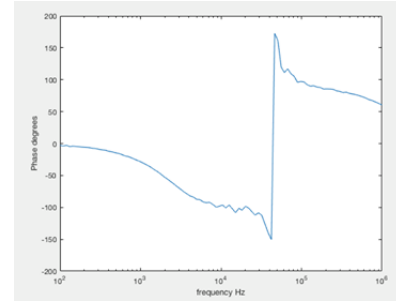


Figure 14: Gain of non-inverting amplifier

This configuration should, under ideal operation, provide 21V/V of gain. The measured gain can be seen in Figure 15.



(a) Gain of non-inverting amplifier



(b) Phase plot of non-inverting amplifier

Figure 15: Non-inverting configuration gain and phase

The measured gain yields 21.5 V/V. This is slightly larger than the predicted 21 V/V but with the correct phase of 0. This amplifier featured a 3dB point of 2 kHz. With only a minor differences in the measured gain from the expected gain, the circuit operated as intended.

4 Discussion

After several minor changes, the op amp operated correctly. The largest change that had to be made was the inclusion of a 150 pF capacitor at the output of the common source amplifier stage. The inclusion of this capacitor change the pole location such that the 0dB crossing point now occurred prior to the 180° phase shift location. Prior to this change the amplifier was unstable and did not have a zero crossing that was in the range of the Digilent's Network analyzer, despite the fact that the 180° phase occurred at about 200 kHz. Some of the other possible locations for this capacitor include across the drains of the active load amplifier and at the input of the common source amplifier. The location that worked the best for the purposes of this lab was the output of the common source amplifier. It should be noted that the op amp remains useful even if it is not unity gain stable, this is due to two reasons; the fact that under feedback op amp can be made stable, and that the op amp can be used as a oscillator which will be seen in Task 6.

This lab also served as introduction to feedback applications of operational amplifiers. The op amp was configured into both inverting and non-inverting topologies. In these two configurations the op amp is expected to behave like any commercial op amp that has been used in ECE 214 and ECE 342. The specifications are outlined in Table 5.

Table 5: Specification values from simulated vs experimental circuit

Parameters	Simulated	Experimental
A_d	75 dB	60 dB
Unity Gain	50MHz	170kHz
3dB drop load	900 Ω	500 Ω V
Inverting gain	-20V/V	-19.9V/V
Non-inverting gain	21 V/V	21.5 V/V
Total Harmonic Distortion	N/A	1.41%

Feedback can be used to improve the performance of the circuit depending on which configuration is chosen by the designer. The stability of the circuit can be improved with the correct setup. One of the largest advantages offered by feedback is the improvement it provides to both in the input and output resistance of the amplifier. An ideal voltage amplifier has infinite input impedance and zero output impedance. For the discrete circuit implemented this was not the case. With the use of feedback the input impedance can be increased by a factor of $1 + A\beta$ while decreasing the output impedance by the same factor.

One of the largest challenges faced by this lab was the op amp remained extremely sensitive to environmental changes. Everytime the circuit was deployed for testing the offset voltage at the output of the common source amplifier had to be changed through the adjustment of the source degeneration resistance. This is due to the thermal coefficients of the MOSFETs are fairly dependent on ambient temperature. A couple of degrees can change the operation range of the amplifier, resulting in the necessity of a new source resistance. The value of the capacitor to ensure stability was constant at 150 pF and did not require any alteration between testing sessions.

5 Conclusion

The design, simulation, and construction of experiments to measure the performance of feedback to the op amp. The gain was measured at 60 dB while unloaded. The smallest value for the load resistor which caused a 3 dB drop in gain was found to be 500 Ω , with a gain measured at 56.33 dB. The compensated unity gain frequency while stable was measured at 170 kHz. The inverting configuration featured -19.9V/V gain with a THD of 1.41%. The non-inverting topology yielded a gain of 21.5V/V. An important lesson learned during this lab was that achieving a gain too high over specification is not helpful when trying to measure values and achieving stability, which is as important as the final gain value.

References

- [1] N. W. Emanatoglu. (2018) Task 5 [Online]
- [2] N. W. Emanatoglu. (2018) Task 5 briefing [Online]