Task 5: Voltage Amplifier

Optical Uplink

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Abstract

The design, simulation and construction of an amplifier circuit are described. In task 5 of the optical uplink project, a voltage amplifier will increase the signal from the active bandpass filter from a low voltage range from 100mV to 5V. Two ways are explored to accomplish this task. The first is using a common source NMOS circuit. The second is using a NPN BJT common emitter circuit. The specifications required, for the purposes of use in the optical uplink project, are a lower cutoff frequency of $\leq$ 1kHz, upper cutoff frequency of 200 kHz, and a peak gain of 21 dB $\pm$ 1 dB. Also, the 2nd Harmonic distortion for a 20 mVp-p sinusoidal signal at 1 kHz must be $<$ 2%. For the purposes of the optical uplink project, the NMOS was chosen instead of the BJT. The lower cutoff frequency for the BJT was greater than 1kHz, while the NMOS had a lower cutoff frequency of approximately 600 Hz. The NMOS circuit output a 22 dB gain and the BJT output 25 dB gain.

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1 Introduction

This report describes design, implementation and test of two voltage amplifiers. One consisting of negative metal oxide semconducting field effect transistors (NMOS). The other comprised of bipolar junction transistors. Figure 1 demonstrates where in the optical uplink project the voltage amplifier is placed.

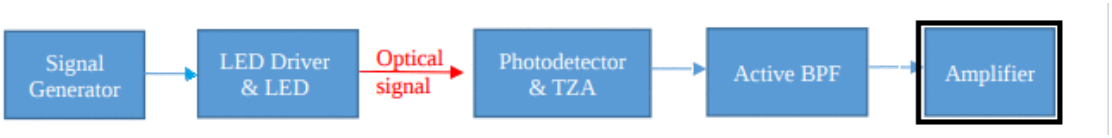

Figure 1: Block diagram for optical uplink [1]

The voltage amplifier is required by the optical uplink project. The output signal from the multi-feedback bandpass filter (MFBP) is in the hundreds of millivolt range. In order to make a more easily detectable signal, a voltage amplifier is required. This can achieved through the use of either a common source or common emitter amplifier. The specifications for this lab are summarized in Table 1.

Table 1: Voltage amplifier specifications

Specifications	Required
Peak gain, with load	21 dB ± 1dB%
Bias current for N_1	1mA
Lower cut-off frequency	≥100 mA
Upper cut-off frequency	at least 200 kHz
R_{in}, small signal	at least 1 MΩ
R_{out}, small signal	at least 3 kΩ
2^{nd} Harmonic distortion @ 1kHz	<2%
Supply voltages	±12 V

The voltage amplifier circuit receives the voltage signal from the MFBP and increases the amplitude of the voltage wavefrom. The desired final output being 5 V. This is achieved with either the use of a NMOS common source amplifier or an NPN BJT common emitter amplifier.

Section 2 of this report describes the design and simulations of the common source amplifier and the common emitter amplifier. Experimental results are addressed in section 3. A discussion of the results, sources of error, and areas of possible improvement are outlined in section 4. Section 5 concludes this report.

2 Circuit Development

This section covers the design choices associated with the various circuits constructed. Both a NMOS common source amplifier and BJT common emitter amplifier. Only the NMOS circuit required design choices as the BJT component values were provided as part of the lab.

The order in which the circuits are discussed is as follows: first the NMOS amplifier followed by the BJT amplifier.

2.1 NMOS common source

The NMOS common source amplifer for this lab was constructed using 2N7000 NMOS transistors. The circuit essentially consists of two parts, the voltage amplifier stage and the current mirror. The generic circuit for the current driver is shown in Figure 2.

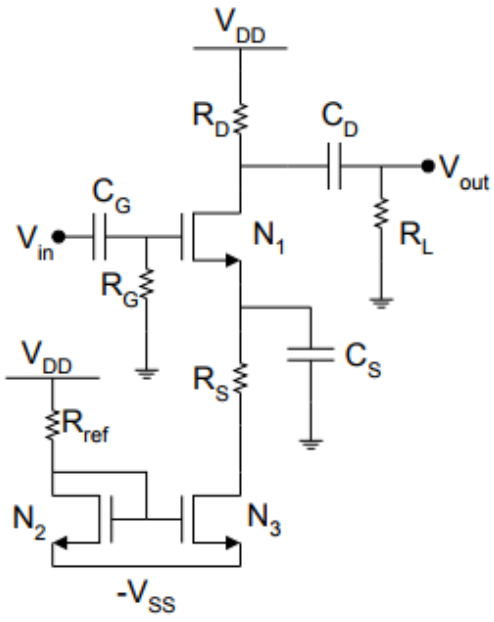

Figure 2: Generic common source amplifier circuit [1]

In order to understand the operation of the circuit, DC analysis of the circuit is required. At DC all the capacitors behave as shorts. It is known that the current through a MOSFET is seen in Equation 1

$$I_D = k(V_{gs} - V_t)^2, \tag{1}$$

Where k is the transconductance parameter, V_{gs} is the gate-source voltage and V_T is the threshold voltage. From the datasheet [2], I_D is 75 mA when V_{gs} is 4.5 V. From Equation 1 k can be found to be 8.5 mA/V. Again using Equation 1, the corresponding V_{gs} for a bias current of 1 mA is found to be 1.85 V. Upon finding the voltage drop over the NMOS, the source resistance can then be found by KCL across the amplifier NMOS. R_s is found to be 8.3 kΩ, R_{ref} can found to be 22.2 kΩ. The capacitor values are chosen such that their impendence is less than their corresponding resistor values. The impendence of the capacitor can be found by Equation 2

$$Z_c = \frac{1}{j\omega C}, \tag{2}$$

where ω is the angular frequency of the input signal in rad/s. By setting Z_c to be less than the corresponding R values, C can be solved to be 4.7 μF.

AC analysis of the circuit is then required in order to find the drain resistance. Figure 3 shows the equivalent small signal model for the NMOS.

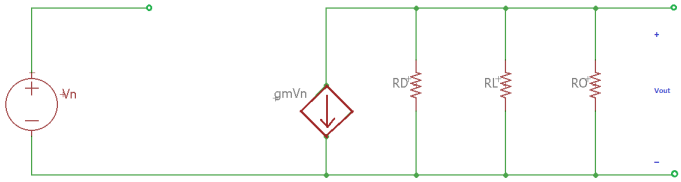

Figure 3: Equivalent small signal circuit

The transconductance of this circuit is defined as Equation 3

$$g_m = \frac{2I_D}{V_{ov}}, \tag{3}$$

where V_{ov} is the overdrive voltage. From this small signal transconductance is found to be 2.8 mA. The small signal r_0, defined as Equation 4

$$r_o = \frac{1}{\lambda I_{DS}}, \tag{4}$$

where λ is the body effect, and found from the datasheet [2] to be zero for the operating conditions. The open circuit gain can then be found by Equation 5

$$\frac{v_o}{v_{in}} = g_m R_o, \tag{5}$$

where R_o is the equivalent resistance of (R_D || R_L). The load resistance is provided by the lab, but for this calculation can be assumed to nearly infinite, therefore R_D is found to be around 2 kΩ. The circuit was then simulated in NGSpice integrated with Matlab. The simulated circuit can be seen in Figure 4.

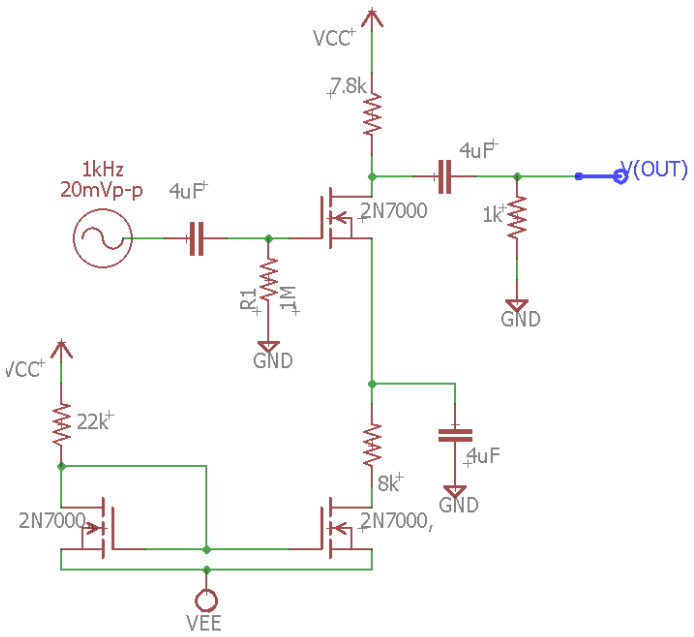

Figure 4: Simulated common source amplifier circuit

A significant change was required in order to meet specs, the R_D value calculated was off by a factor of 4. This is due to assumptions made during analysis for the solution of the transconductance amplifier. The final R_D was found by to be 7.8 kΩ more detail is provided in discussion. In addition, the negative bias voltage was altered to -8 V in order to reduce harmonic distortion. The frequency of the NMOS is shown in Figure 5.

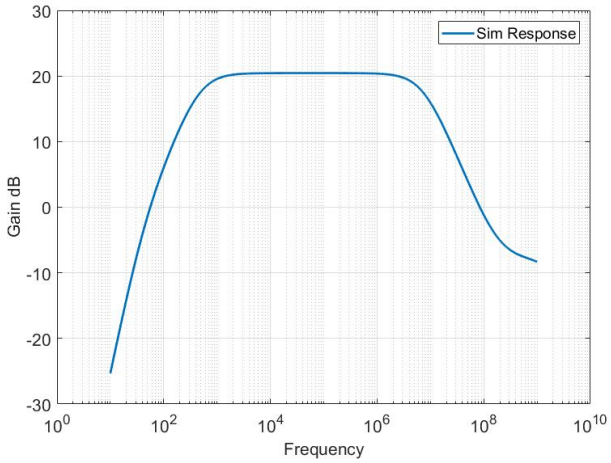

Figure 5: Simulated frequency response of NMOS amplifier

The NMOS met the specified gain at 21 dB with a 3dB lower cut off frequency well below the required 1 kHz. The FFT of NMOS can be seen in Figure 6.

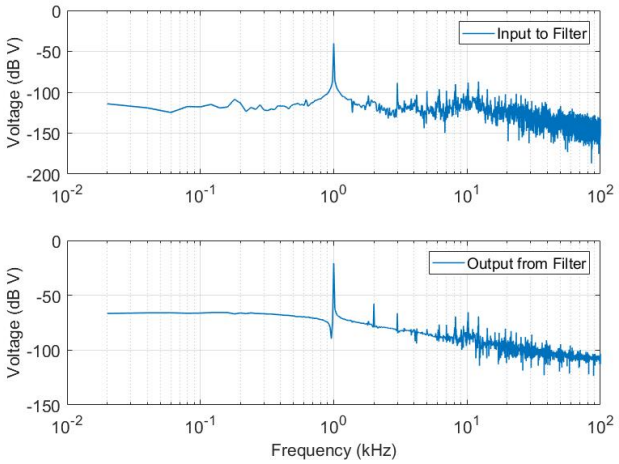

Figure 6: Simulated FFT of second harmonic distortion

This analysis was performed by inputting a 10 mV signal at 1 kHz. The measured distortion on the second harmonic is required to be less than 2%. By inspection the distortion is found to be 1.5%. Table 2 summarizes the NMOS simulation results.

Table 2: NMOS summary

Q_1, Q_2, Q_3	2N7000
R_ref	19.3 kΩ
R_D	7.8 kΩ
R_S	8 kΩ
R_G	1 MΩ
C_g, C_d, C_l	4.7 μF
Lower cutoff	500 Hz
Upper cutoff	10 MHz

After making slight alterations the circuit worked correctly in simulations.

2.2 BJT common emitter

The BJT operates similarly to the NMOS circuit. The difference being it is now an NPN transistor and is therefore a current controlled voltage source, as opposed to the NMOS which is a voltage controlled. The values for the BJT circuit were not solved for, but instead provided as part of the lab, which can be seen in Table 3

Table 3: BJT experimental values

Q_1, Q_2, Q_3	2N3904
R_ref	19.3kΩ
R_C	4.7kΩ
R_B	10kΩ
R_E	3.3kΩ
R_L	1kΩ
C_B, C_C, C_E	500nF
Gain	30db
Lower cutoff	3 kHz
Upper cutoff	100 MHz

The simulated circuit is shown in Figure **??**.

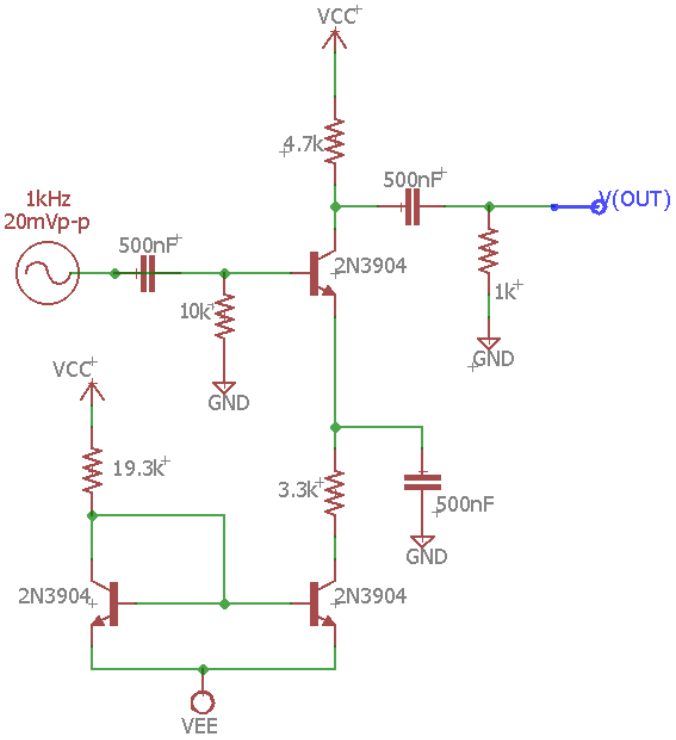

Figure 7: Simulated circuit of BJT

The simulations of the BJT follow and were performed in Matlab integrated with NGspice. The frequency response of the circuit can be seen in Figure 8.

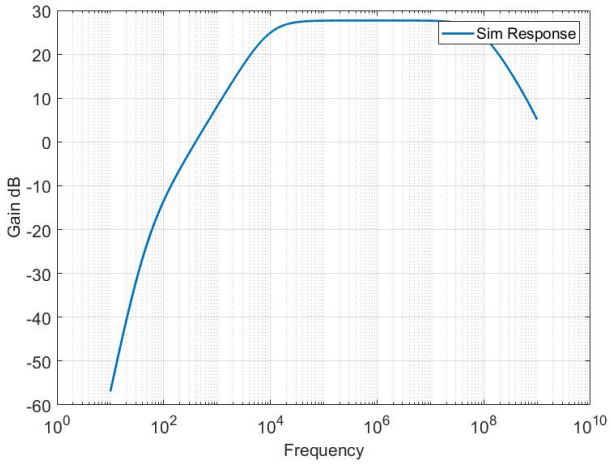

Figure 8: Simulated frequency response of BJT

Notably, the 3dB lower cutoff is greater than 1 kHz. The corresponding passband gain is significantly higher than 20 dB. This is not ideal, because the output could begin to saturate due to excessive gain. The FFT of the BJT can be seen in Figure 9

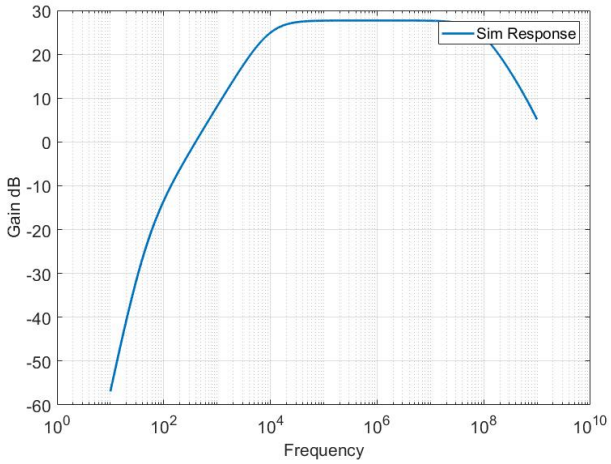

Figure 9: Simulated FFT BJT circuit

The BJT achieved a far smaller second harmonic distortion than the NMOS, with only a .25% distortion for the 2 kHz harmonic.

3 Experimental Implementation

The circuits required only minor changes from simulation to experimental implementation.

3.1 NMOS amplifier

The final circuit is shown in Figure 10.

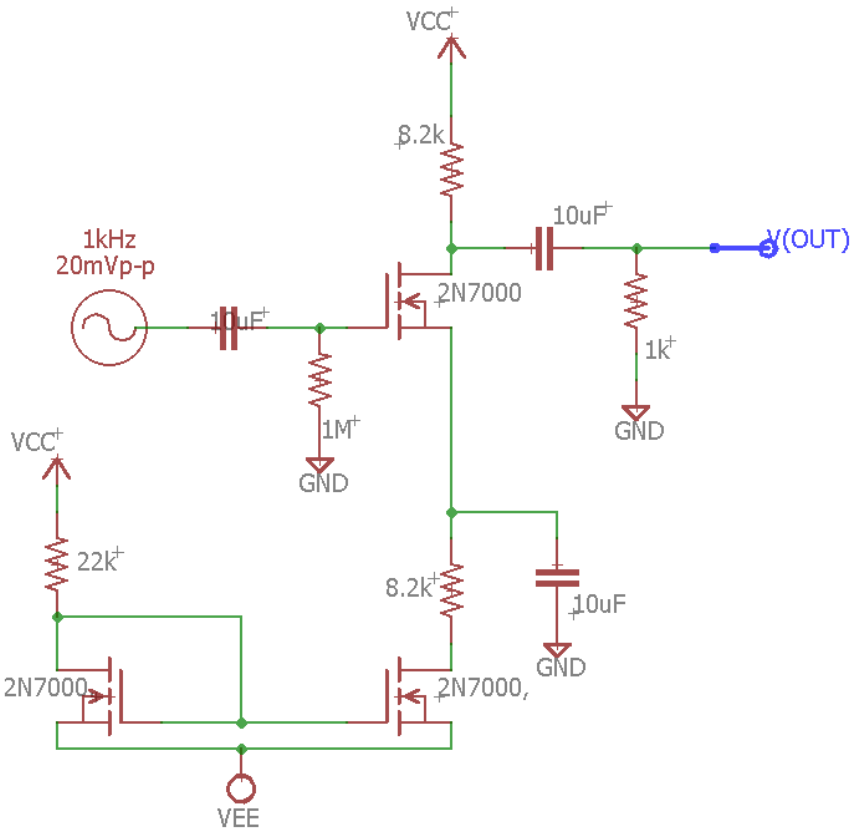

Figure 10: NMOS final circuit schematic

Some of the resistor values had to be changed in order to meet specifications. The capacitors had to be increased as well due to the poor performance of the equivalent nominal value electrolytics. The implemented capacitors are parallel plate which operate better at higher frequencies. Figure 11 demonstrates the experimental frequency response of the NMOS amplifier.

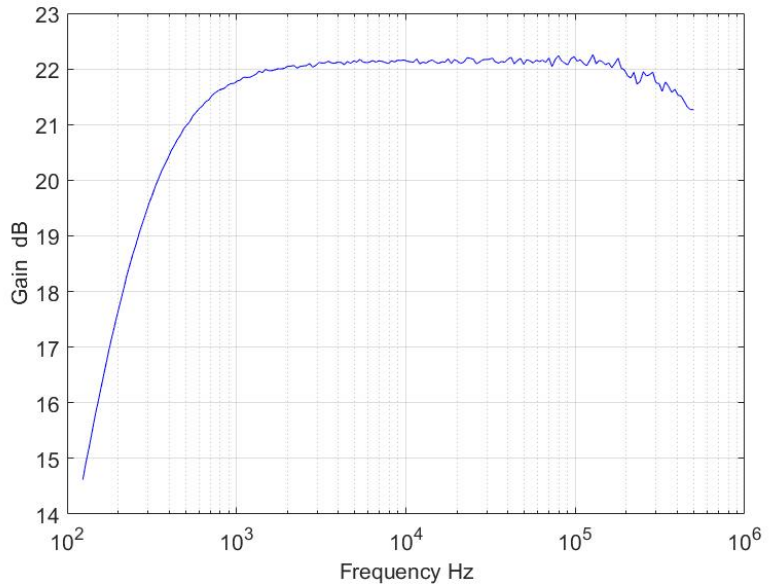

Figure 11: NMOS experimental frequency response

The gain was just on the high end of the specification at 22 dB. The lower cutoff frequency is less than 1 kHz. The upper cutoff also meets spec by being greater than 200 kHz. The FFT of the circuit can by seen in Figure 12.

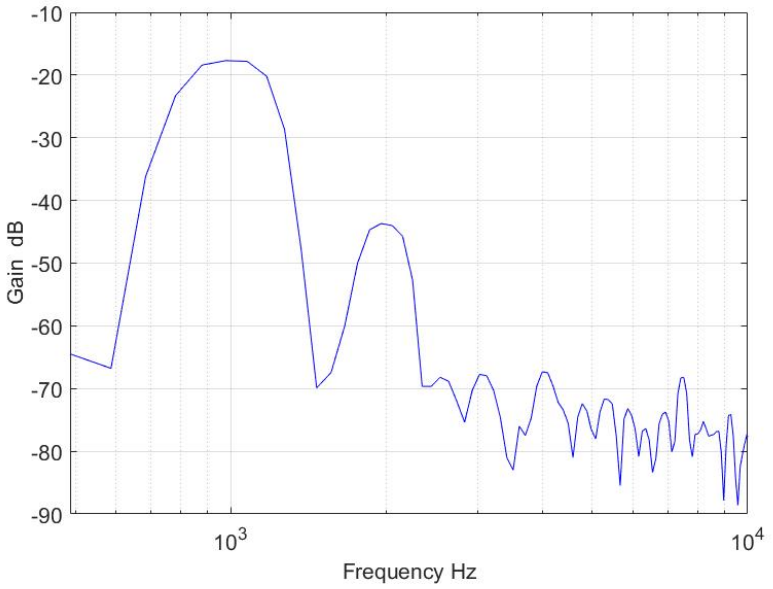

Figure 12: NMOS experimental FFT

The second harmonic distortion was slightly too high at 5%. This can be altered by the negative bias volt-

age, for the purpose of this lab, 5% was deemed acceptable. Table 4 shows the summary of the experimental NMOS circuit.

Table 4: NMOS experimental values

Q_1, Q_2, Q_3	2N7000
R_ref	22 kΩ
R_g	1 MΩ
R_d	8.2 kΩ
R_s	8.2 kΩ
R_L	1kΩ
C_B, C_C, C_E	10 μF
Gain	21 dB
Lower cutoff	600 Hz
Upper cutoff	10 MHz

After minor alterations the circuit operated correctly.

3.2 BJT amplifier

The BJT required only a slight change of capacitor values, due to availability. Figure 13 shows the final circuit for the BJT amplifier circuit.

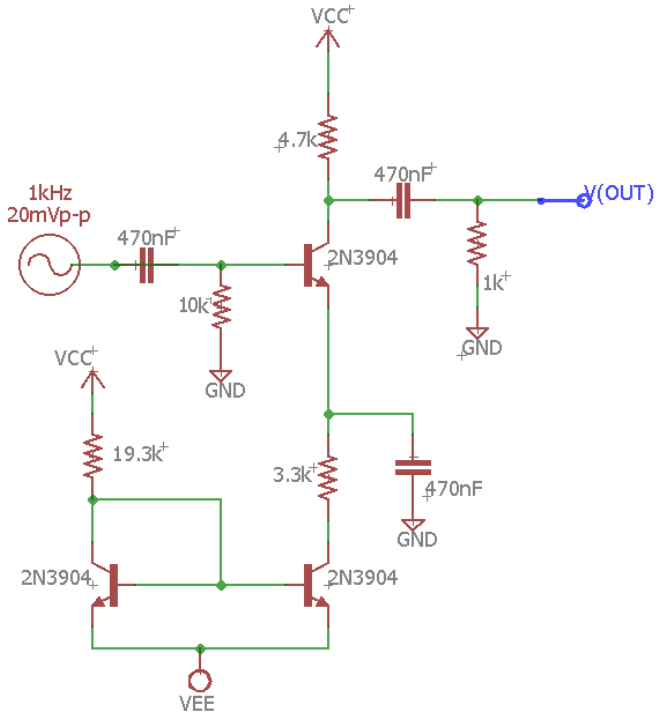

Figure 13: BJT final schematic

The BJT was built using the provided components. The experimental frequency response of the circuit is shown in Figure 14.

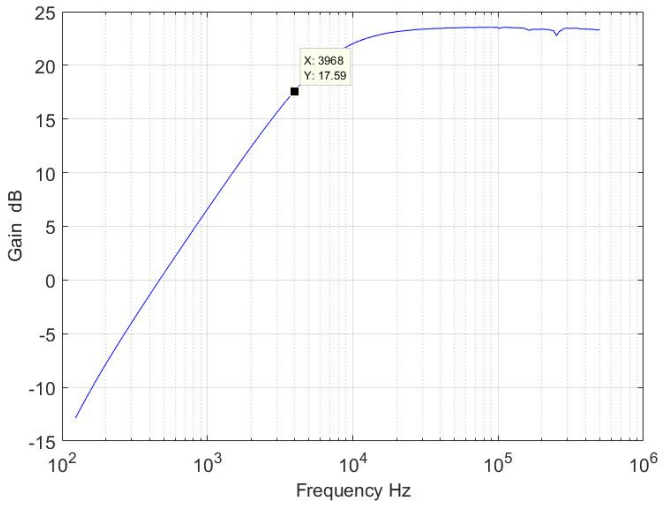

Figure 14: BJT experimental frequency response

The gain was a little less than the simulated, at 24 dB, but the lower cutoff was quite higher at 6 kHz, far higher than the specified 1 kHz. The upper cutoff can not be measured exactly due to the limitations of the Digilent Discovery board's network analyzer. The measured values are only accurate up to 500 kHz. The measured FFT of the BJT can be seen in Figure 15.

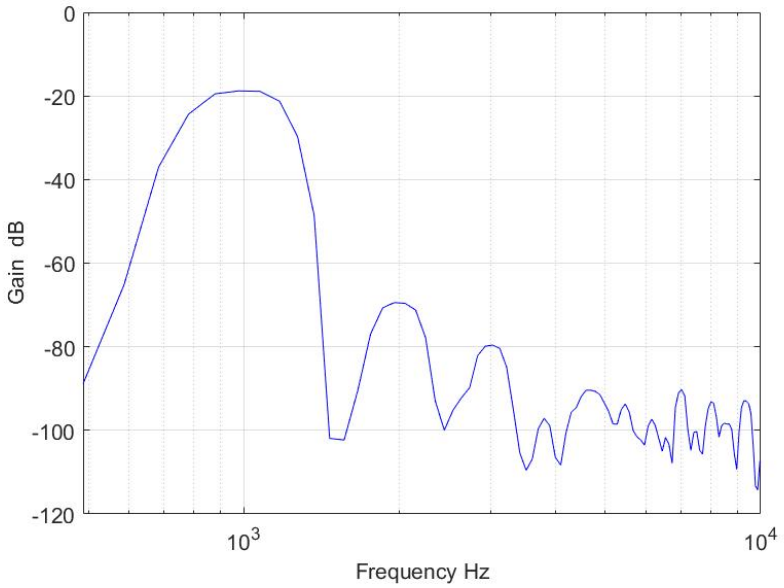

Figure 15: BJT experimental FFT

The second harmonic distortion was significantly less than the NMOS while still being in spec, at roughly 1%. Table 5 shows the summary of the BJT performance.

Table 5: BJT experimental values

Q_1, Q_2, Q_3	2N3904
R_ref	19.3kΩ
R_C	4.7kΩ
R_B	10kΩ
R_E	3.3kΩ
R_L	1kΩ
C_B, C_C, C_E	470nF
Gain	25 dB
Lower cutoff	6 kHz
Upper cutoff	>500 kHz

Overall, the BJT operated as expected, discussion and comparison of the two circuits can be found in Discussion.

4 Discussion

After several minor changes, both circuits operated correctly. This lab served as introduction to the main differences between MOSFET and BJT devices. The two components are both transistors but have defining differences, mainly the polarity of the devices. The specifications are outlined in Table 6.

Table 6: BJT and NMOS comparison

BJT	Values	NMOS	Values
Q_1, Q_2, Q_3	2N3904	N_1, N_2, N_3	2N7000
R_ref	19.3kΩ	R_Ref	22kΩ
R_C	4.7kΩ	R_D	8.2kΩ
R_B	10kΩ	R_G	1MΩ
R_E	3.3kΩ	R_S	8.2kΩ
R_L	1kΩ	R_L	1kΩ
C_B, C_C, C_E	470nF	C_G, C_S, C_D	10μF
Gain	25 dB	Gain	22 dB

Notably, different voltages than those specified in the lab manual were used as the Analog Discovery handles small voltage signals very poorly, producing a lot of noise. Other than this both circuits had little issue performing as expected.

The BJT, while having a larger gain and much less 2nd harmonic distortion, did not have the required cutoff frequency to meet the specification for the optical link project, thus the NMOS CS amplifier was chosen for it's ability to meet specification.

One of the biggest challenges of this lab was the mathematical assumptions and operations used to solve for the transistor values in simulation. When dealing with such devices the assumptions used can some-

times give wildly incorrect values and lead to repetition of calculations until correct. Fortunately simulations help greatly with reducing the time it takes to get to the correct solution.

The final circuits fell well within specifications and operated correctly after minor component alterations.

5 Conclusion

The design, simulation, and implementation of a voltage amplifier have been explained. The specifications required, for the purposes of use in the optical uplink project, are a lower cutoff frequency of $\leq$ 1kHz, upper cutoff frequency of 200 kHz, and a peak gain of 21 dB $\pm$ 1 dB. Also, the 2nd Harmonic distortion for a 20 mVp-p sinusoidal signal at 1 kHz must be $< 2\%$. The sinusoidal source was 20 mV_{P-P} at 1kHz, and the supply voltages were $\pm$ 12V. This resulted in a lower cutoff frequency of approximately 600 Hz and the upper cutoff frequency was in the MHz range, which exceeds the required $\geq$ 200 kHz. The 2nd harmonic distortion was measured to be approximately 5%. An important lesson was learned about the comparison between a voltage amplifier using NMOS components and a voltage amplifier using BJT components.

References

[1] D.E. Kotecki Lab.(2017) Lab #5 Voltage Amplifier [Online]. Available: http://davidkotecki.com/ECE342/labs/ECE342_2017_Lab5.pdf

[2] ON Semiconductor. (2017) 2N7000 [Online]. Available: http://www.onsemi.com/PowerSolutions/supportDoc.do?type=models&rpn=2N7000