Task 4: Operational Amplifier

Discrete Amplifier

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Abstract

The design, simulation, and construction of experiments to measure the performance of a differential amplifier is explored.Two differential amplifiers will be tested. The first amplifier is a resistively loaded amplifier, while the second differential amplifier has an active load. The common mode rejection ratio, input common mode voltage range and differential gain verses singled-ended gain will be measured. The double-ended resistively loaded with cascode current mirror amplifier has a differential gain of 19 dB with a common mode gain of approximately -55 dB and a CMRR max of 90 dB at 1V. The double-ended active loaded amplifier has a max differential gain of 30 dB has a max common mode gain of approximately -29 and a max CMRR of 59 dB.

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1 Introduction

This report describes the design, construction, and analysis of an discrete component operational amplifier. The topology chosen includes a simple current mirror that sinks current to a resistively loaded amplifier which in turn is cascaded with an actively loaded differential pair which outputs single-endedly to a common source amplifier stage. This common source stage is then passed to an output Bipolar Junction Transistor (BJT) amplifier stage. The general schematic for a generic op amp is shown in Figure 1.

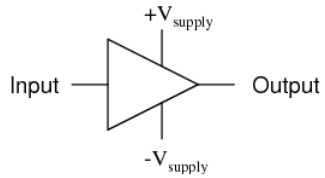

Figure 1: General operational amplifier symbol [1]
[1]

Operation amplifiers serve an integral building block for modern electronics. Op amps provide large gain with various configuration schema. This allows the circuit designer to use the op amp in different topologies and achieve different results, all without modifying the op amp circuit itself. In addition, an op amp provides significant gain while maintaining stability. The objective of this lab is to create an op amp out of discrete components that achieves the specifications as seen in Table 1.

Table 1: Specifications

Specifications	
Power	$\pm$5V
Bias Current	500 μA
Overall Voltage Gain	200V/V (46 dB)
CMRR	$\geq$ 60dB
Output Voltage Swing	$\geq \pm$ 2V

The input stage of an operational amplifier consists of a differential amplifier. For the purposes of this experiment, the NMOS MOSFET that will be used is the ALD1106, and the ALD1107 for the PMOS MOSFET. Differential amplifiers are desirable for their increased immunity to noise and that DC coupling of stages is possible without disturbing bias conditions. Each one of these designs will have some advantage as well as some disadvantage over the other circuits. The primary function of the input differential pair will be to provide a high common mode rejection ratio (CMRR). The differential gain, Ad, need not be high, as long as the common mode gain, Acm, is very small. Some op-amp designs use multiple differential input-differential output stages until they convert to a single ended input.

These differential amplifiers are biased by a current mirror, cascoded or simple, (assumed to be ideal for simulations) and constructed using PMOS and NMOS integrated circuits. The circuit on the left is a resistively loaded differential amplifier. The circuit depicted on the right is an actively loaded differential amplifier.

Section 2 of this report describes the design, and when relevant, the simulations of the experiments. Experimental results and implementation are addressed in Section 3. A discussion of the results, sources of

error, and areas of possible improvement are outlined in Section 4. Section 5 concludes this report.

2 Circuit Development

Three different op amp topologies were provided as part of the lab. The chosen circuit can be seen in can be seen in Figure 2.

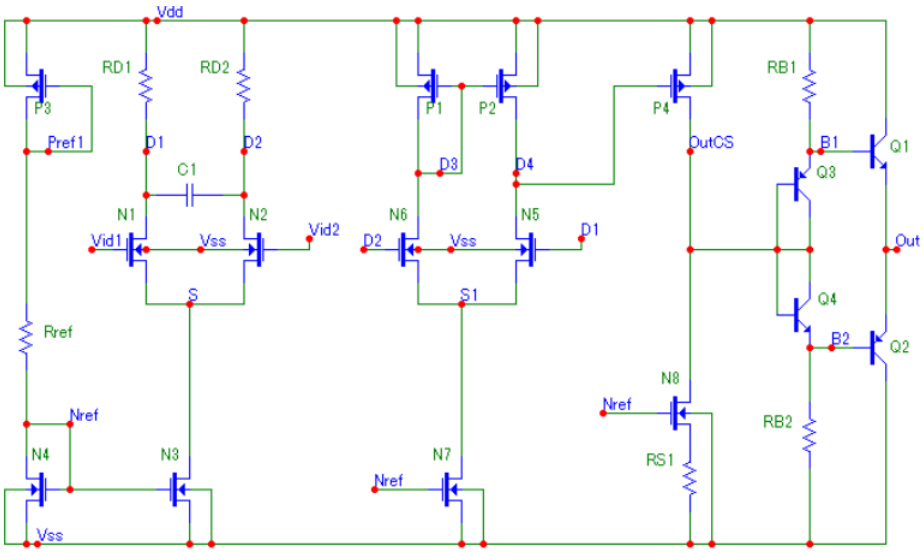

Figure 2: Generic schematic for chosen topology [2]

This design was chosen due to the fact that every stage, with the exclusion of the output stage, was designed as part of a previous task. The stages can be broken down as such: a simple current mirror, a resistively loaded differential pair, an active loaded differential pair, an active load common source amplifier and finally a BJT amplifier output stage. The final simulated circuit can be seen in Figure 3

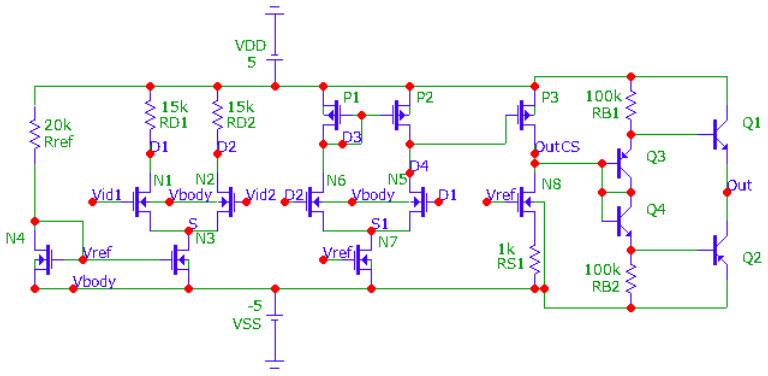

Figure 3: Simulated op amp circuit

The circuits will be simulated in MicroCap 11. The values for the components will initially be the values calculated in circuit development. The generic bias conditions for the ALD1106 and 1107 are summarized in Table 4.

I_{DS}	ALD1106				ALD1107			
	V_{OV}	V_{GS}	g_m	r_o	$\|V_{OV}\|$	V_{GS}	g_m	r_o
100 µA	0.63	1.43	3.16E-04	333 kΩ	1.00	-1.80	2.00E-04	333 kΩ
200 µA	0.89	1.69	4.47E-04	167 kΩ	1.41	-2.21	2.83E-04	167 kΩ
400 µA	1.26	2.06	6.32E-04	83.3 kΩ	2.00	-2.80	4.00E-04	83.3 kΩ
500 µA	1.41	2.21	7.07E-04	66.7 kΩ	2.24	-3.04	4.47E-04	66.7 kΩ
1 mA	2.00	2.80	1.00E-03	33.3 kΩ	3.16	-3.96	6.32E-04	33.3 kΩ
2 mA	2.83	3.63	1.41E-03	16.7 kΩ	4.47	-5.27	8.94E-04	16.7 kΩ

Figure 4: Typical ALD bias conditions [3]

Here the typical bias conditions for the constraining MOSFETs can be seen. For the purposes of this lab, the bias current of 400 μA was chosen.

2.1 Resistively Loaded Differential Amplifier

The resistively loaded amplifier stage requires a current mirror in order to generate the chosen bias current of 400 μA. This was achieved by applying Ohm's Law. The V_{gs} of the simple current mirror needs to be -3V. In order to have the correct current R_{ref} was set to 20kΩ. The simulated resistive load differential pair can be seen in Figure 5.

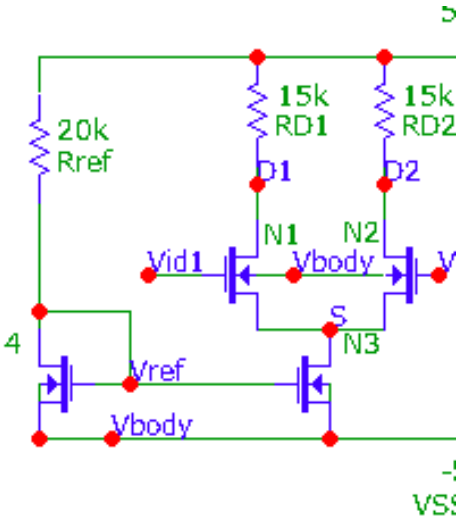

Figure 5: Simulated resistive load differential amplifier

In addition, the current through the load resistors needs to be half of the bias current. As a result, the resistance values can be found by applying KVL which can be seen in Equation **??**

$$V_{o_1} = V_{DD} - \frac{1}{2} I_{bias} R_d, \tag{1}$$

where V_{DD} is the supply voltage. This leads to R_{drain} of 15kΩ. The differential gain of the circuit can be found by Equation 2

$$A_d = g_m R_d, \tag{2}$$

where g_m is the transconductance of the amplifying NMOS and R_d is the drain resistance and was calculated to be 16 dB. The output is double ended due to it feeding another amplifier stage. The simulated gain can be seen in Figure 6.

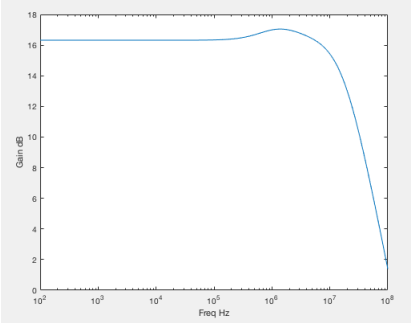

Figure 6: Simulated resistive load differential gain

This was measured by performing an AC analysis in Microcap from 100Hz to 1MHz. This was performed by grounding one of the inputs whilest measuring the voltage differentially from the output nodes. The simulated value was marginally higher at 16.2 dB. The simulated phase can be seen in Figure 7.

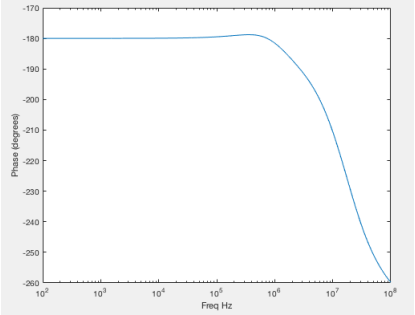

Figure 7: Simulated resistive load differential phase

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The phase can be seen to be 180 degrees stable until 1 MHz. This is desirable for an input stage, which is why the differential pair was chosen as the first stage. This stage was then cascaded with an active load differential pair.

2.2 Active Load Differential Pair

The next stage of op amp is the active load differential pair. This circuit is identical to that designed in Task 3. This circuit can be seen in Figure 8. This modification allows for the single ended output to achieve gain that is comparable to that of the active load with a double ended output.

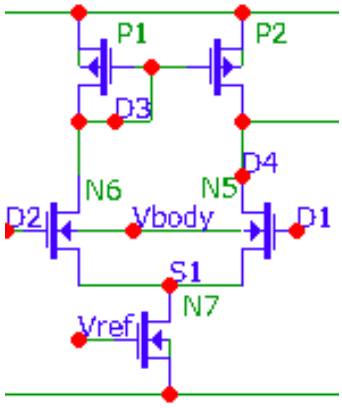


Figure 8: Simulated active load differential amplifier

The differential gain for an actively loaded differential pair can be seen with Equation **??**

$$A_d = g_{m_N}(r_{o_P}||r_{o_N}), \tag{3}$$

where r_o is the small signal output resistance of a MOSFET which is found by the Equation **??**

$$r_o = \frac{1}{\lambda I_{DS}}, \tag{4}$$

where λ is the channel length modulation parameter. The output resistance for NMOS is found to be 172kΩ and PMOS is found to be 162kΩ. he differential gain was calculated to be 35 dB. The simulated differential gain for the active load can be seen in Figure 9.

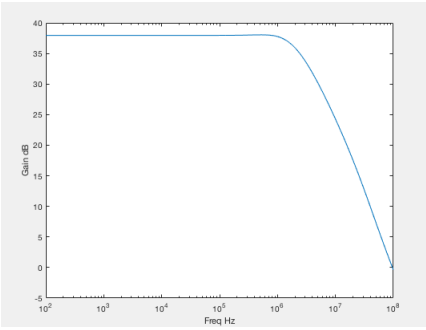


Figure 9: Simulated active load differential gain

This simulation was performed in the same manner as the resistive load. The differential gain is found to be much high than resistive load at 38 dB and consistent with the calculated value of 35 dB. The phase of the active load can be seen in Figure 10.

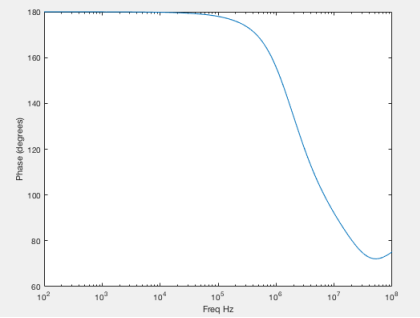


Figure 10: Simulated active load differential phase

This stage can be seen to only be 180 degree stable until 100 kHz. This is the minimum required by the lab specifications. This stage is then passed to an active loaded common source stage.

2.3 Common Source Amplifier

The common source amplifier features an active load which serves as a biasing network. The common source allows for the output loading effects of the active load to be ignored due to the near infinite input impedence seen at the gate of the common source. The simulated circuit can be seen in Figure 11.

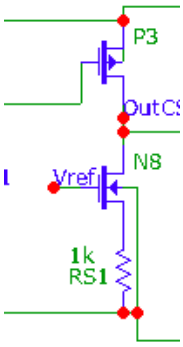


Figure 11: Simulated common source amplifier

The voltage gain of a common source amplifier can be expressed in Equation 5

$$A_{vo} = -\frac{g_m R_d}{1 + g_m R_s}, \tag{5}$$

where R_s is the resistance seen at the source of the amplfying transistor which in this case is the r_o of the

active load. The gain can be calculated to be 23 dB. The active load features source degeneration, this resistor value should be large enough to ensure that with grounded inputs the common source output node is 0V. The resistor that achieved this is 1 kΩ. The simulated gain can be seen in Figure 12.

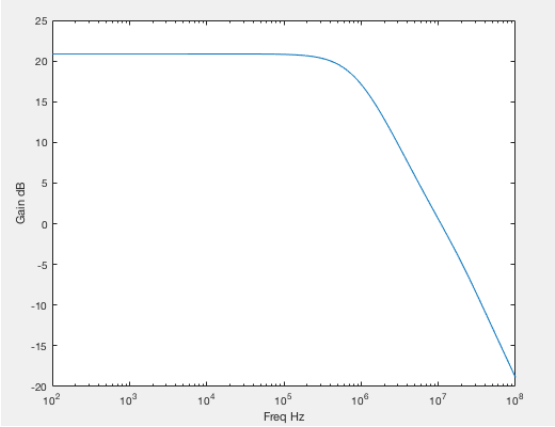


Figure 12: Simulated common source amplifier gain

The gain is slightly less than the calculated 23 dB at 20.5 dB. The phase the common source stage can be seen in Figure 13.

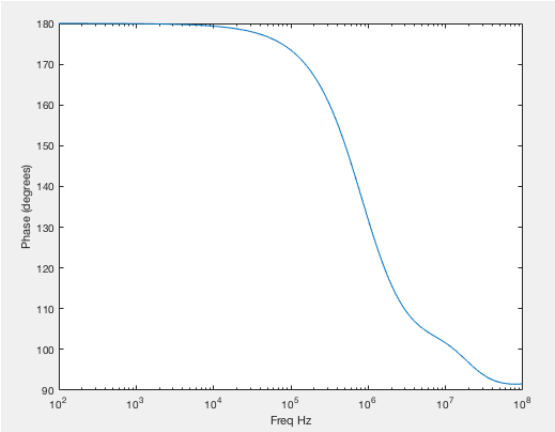


Figure 13: Simulated common source amplifier phase

The common source, similar to that of the active load, is 180 degree stable until 100 kHz. The common source is then fed to an output stage. The output stage will be covered in more detail in a later task. For the purposes of this lab the output stage can be treated as an emitter follower.

2.4 Output Stage

Due to the design of this stage is mostly beyond the scope of this task, the largest deisgn consideration was choosing resistors values great enough to ensure that the base emitter voltages of remain less than 0.7V. These values were changed in Microcap until the correct bias conditions were found. The resistor values were found to be 100 kΩ. The simulated gain can be seen in Figure 14.

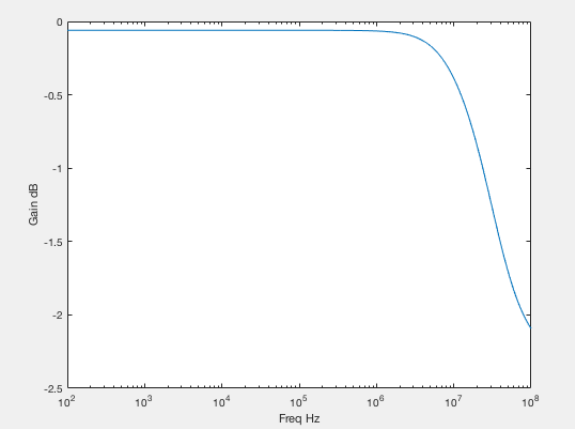


Figure 14: Simulated output stage gain

The gain can be seen to be a little less than one, this is expected by the emitter follower nature of the stage. The Ideal emitter follower has a voltage gain of 1 V/V. The simulated phase can be seen in Figure 15.

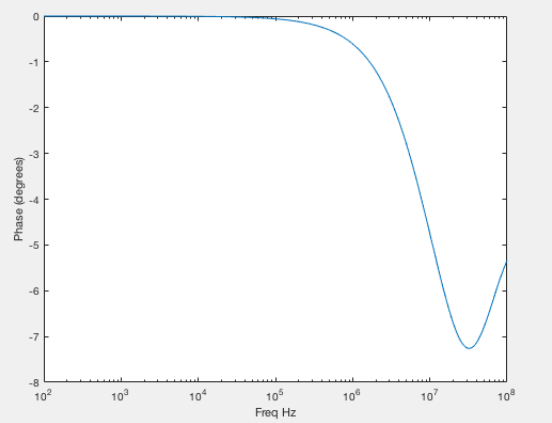


Figure 15: Simulated output stage phase

The output stage remains 180 degree stable until 1 MHz, which is a decade higher than the previous two stages. The overall gain of the circuit can be seen in Figure 16.

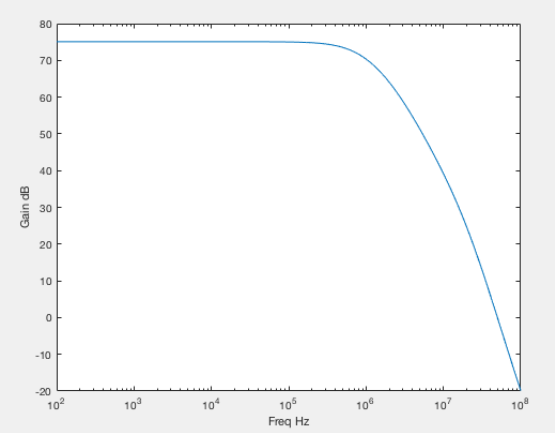


Figure 16: Simulated overall gain

The gain can be seen to be much greater than the required 46 dB at 75 dB. Care is necessary when building this circuit as very little input could result in a railed output. The final phase can be seen in Figure 17.

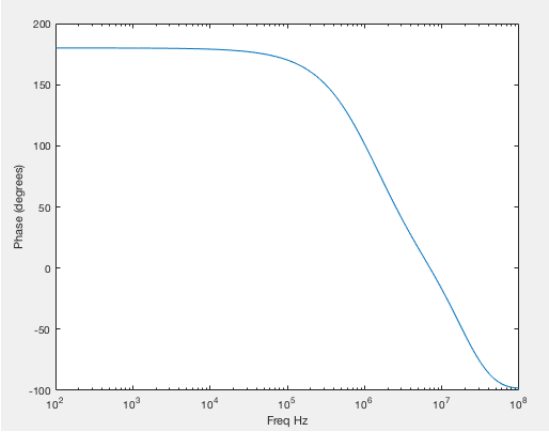


Figure 17: Simulated overall phase

The final output can be seen to be 180 degree stable until 100 kHz, which is required by the specifications. The DC bias conditions measured in Microcap can be seen in Table 2.

Table 2: DC bias values

DC Bias Conditions	
Vref	-3.003V
D1	1.284V
D2	1.284V
D3	2.78V
D4	2.78V
S	.972V
S1	-1.34V
OutCS	-82mV
Out	-11.4mV

The DC bias conditions match that of this found in previous tasks. Notably the output of both the CS and final stage is not 0V, which is what is expected. This is due to body effect and channel length modulation effects, this voltage is known as the offset voltage.

3 Experimental Implementation

This section details the experimental implementation of the two differential amplifiers, the resistively loaded and active loaded. The power supplies and analysis were implemented using the Digilent Analog Discovery kit.

3.1 Resistively loaded differential amplifier

The resistively loaded amplifier was constructed in two different ways. The first was constructed using a cascode current mirror and the other was constructed using a simple current mirror.

3.1.1 Cascode current mirror

The experimental circuit for the resistively loaded differential amplifier is shown in Figure 18 below.

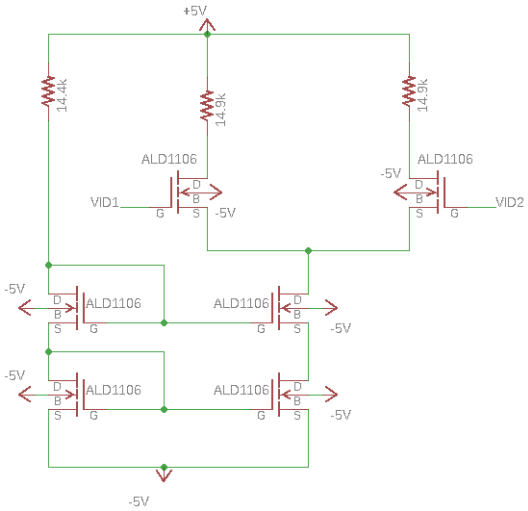


Figure 18: Experimental active load differential amplifier

The drain resistances were measured to be 14.9kHz for each branch

Compared to the simulated circuit for the resistively loaded differential amplifier, that values needed to be changed in order to meet specifications. The values of the node voltages and altered component values are seen in Table 3 below.

Table 3: Experimental resistively loaded differential amplifier values

Simulated resistively loaded differential amplifer	
Components/Nodes	Values
V_{ref_1}	-3.13V
V_{ref_2}	-0.62V
I_{bias}	397μA
I_{ref_1}	197μA
I_{ref_2}	196μA

The VTC for this topology can be seen in Figure 19.

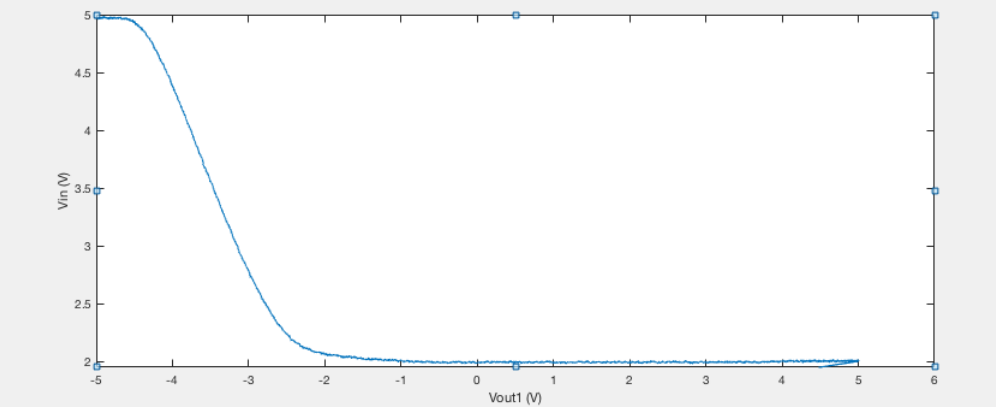
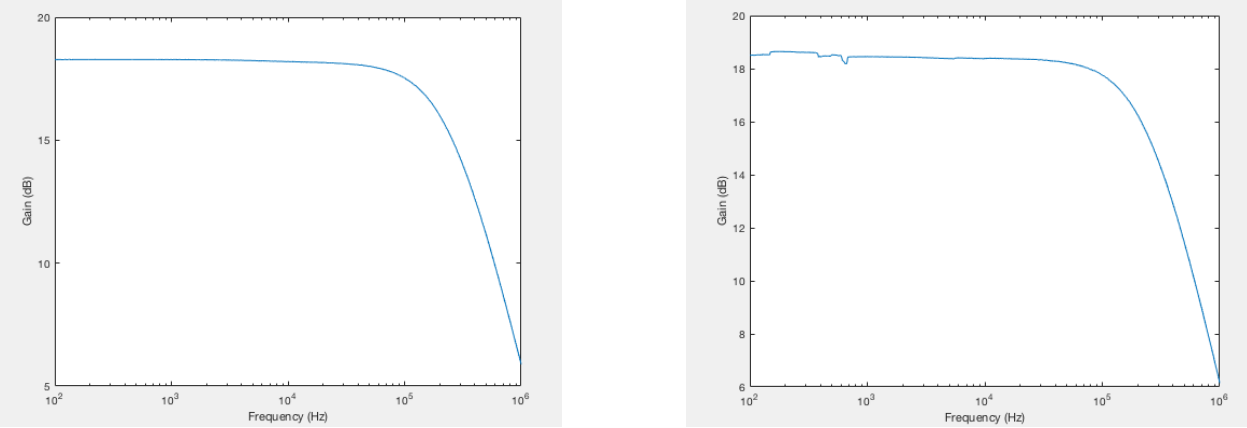


Figure 19: Experimental VTC of cascode resistive load amplifier

The range of operation can be seen by the central linear region, this region is the region of saturation for this set up. The differential gain for both the single ended and double ended outputs can be seen in in Figure 20.

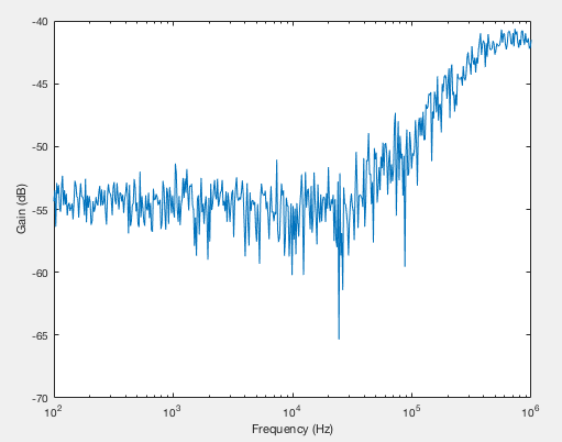


(a) Ad, double ended

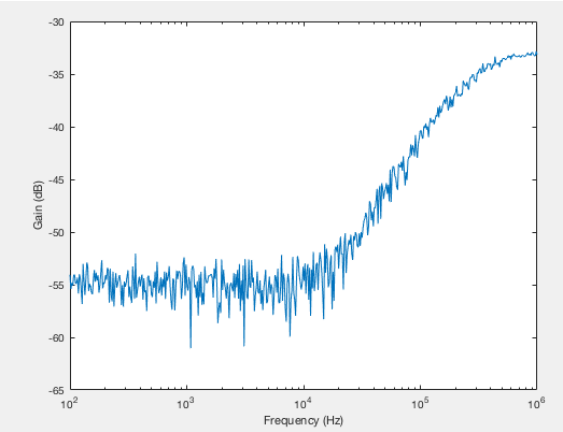
(b) Ad, single ended

Figure 20: Differential gain, Ad, Cascode resistive load

It can be seen that the single ended operated slightly better than the double ended. The common mode gain measured at 100mV can be seen in Figure 21.



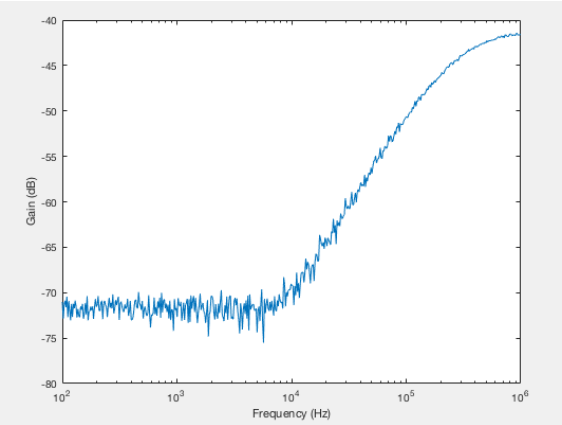
(a) Acm, double ended



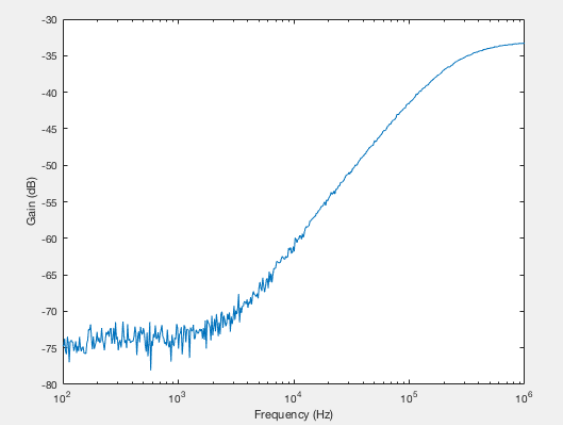
(b) Acm, single ended

Figure 21: Common mode gain, Acm, cascode resistive load

The measurement was repeated for 1V as well, which can be seen in Figure 22



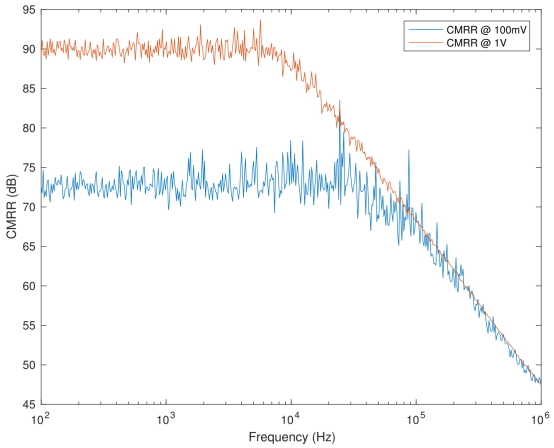
(a) Acm, double ended



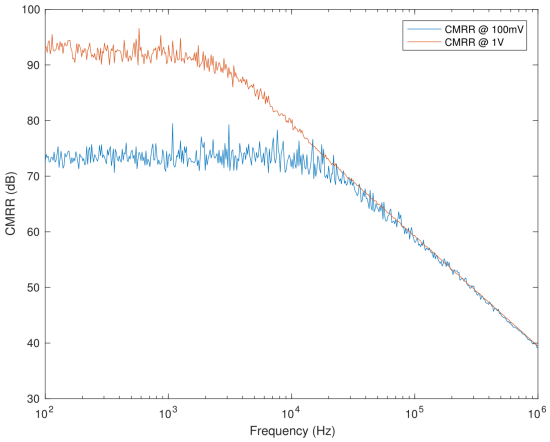
(b) Acm, single ended

Figure 22: Common mode gain, Acm, cascode resistive load

The 1V clearly had less noise, which is ideal. The trade off, however, is this can saturate the differential gain. From these measurements the CMRR was found by combining the datasets for Ad and Acm in Matlab and can be seen in Figure 23.



(a) CMRR double ended



(b) CMRR single ended

Figure 23: CMRR cascode resistive load

The amplifier produced a much higher CMRR, approximately 15dB, for the 1V input.

3.1.2 Simple current mirror

The simple current mirror was created by simply removing the conducting transistor N3 from the cascode. The DC bias conditions can be seen in Table 4

Table 4: Experimental resistively loaded differential amplifier, simple current mirror

Simulated resistively loaded differential amplifer	
Components/Nodes	Values
V_{ref_1}	-3.09V
I_{bias}	398μA
I_{ref_1}	202μA
I_{ref_2}	203μA

The change to simple did little to impact the DC bias conditions of the circuit. The VTC of the simple current mirror mode can be seen in Figure 24.

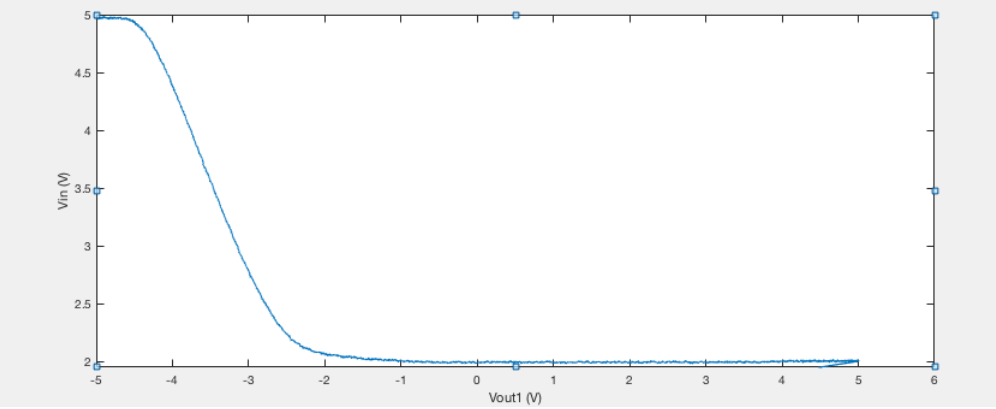
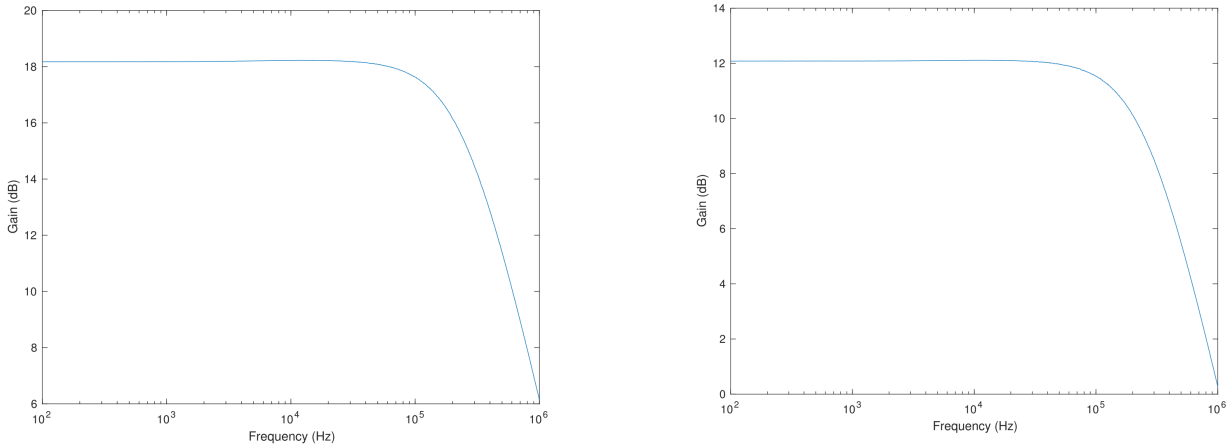


Figure 24: Experimental VTC of simple current mirror resistive load amplifier

The compliance range is wider than that of the cascode, discussion of this can be found in the Discussion section. The differential gain for the simple current mirror case can be seen in Figure 25.

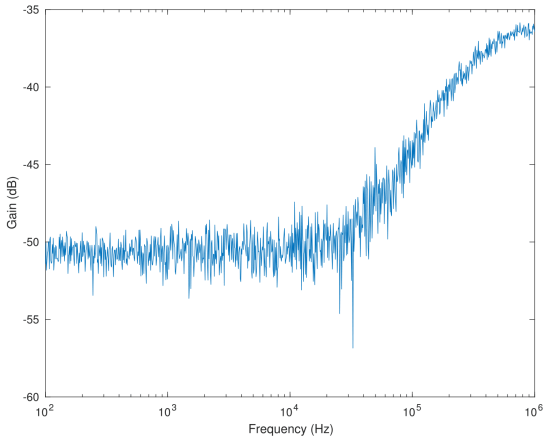


(a) Ad, double ended

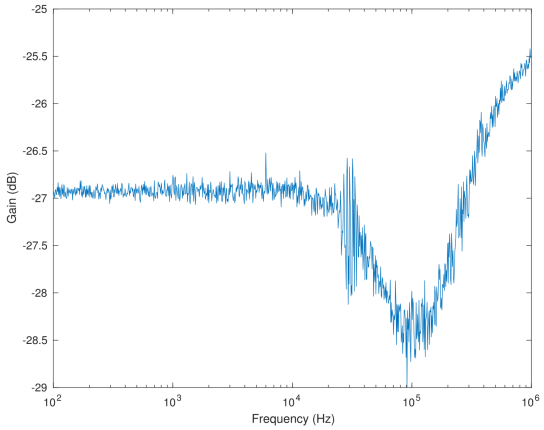
(b) Ad, single ended

Figure 25: Differential gain, Ad, simple resistive load

It can be seen that the single ended operated slightly better than the double ended. The common mode gain measured at 100mV can be seen in Figure 26.



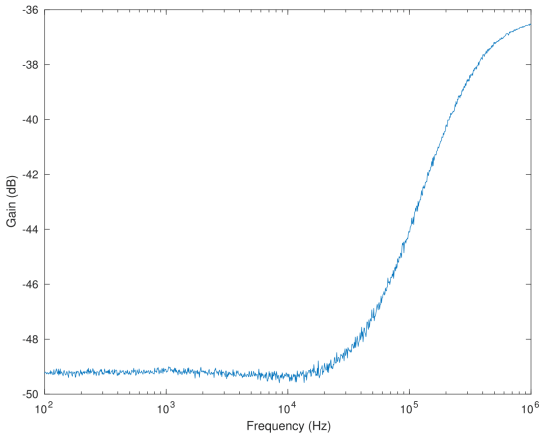
(a) Acm, double ended



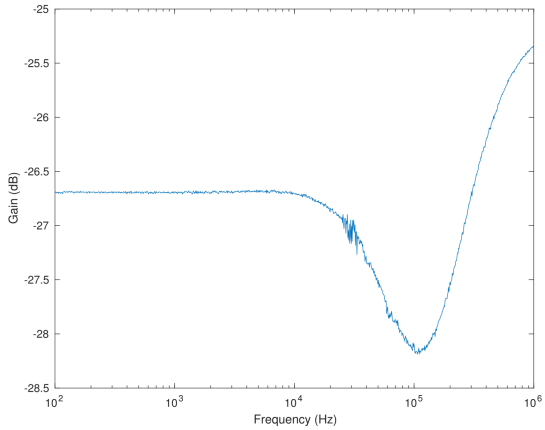
(b) Acm, single ended

Figure 26: Common mode gain, Acm at 100mV, simple resistive load

The measurement was repeated for 1V as well, which can be seen in Figure 27



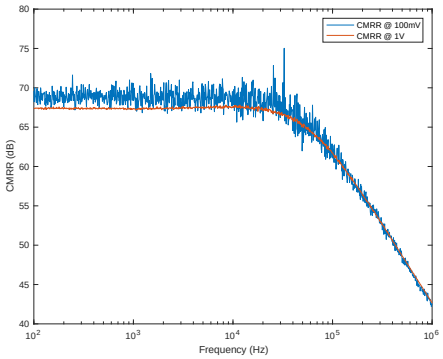
(a) Acm, double ended



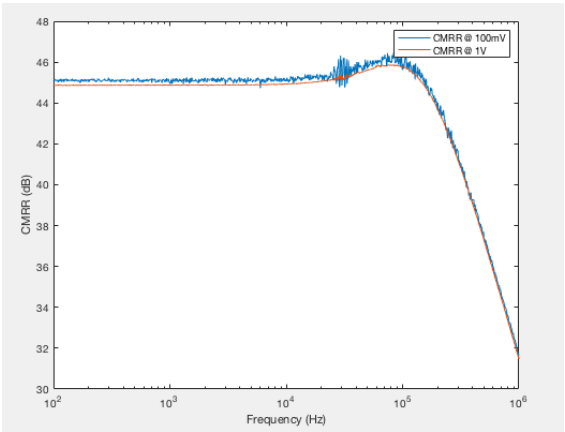
(b) Acm, single ended

Figure 27: Common mode gain, Acm at 1V, simple resistive load

The 1V clearly had less noise, which is ideal. The trade off, however, is this can saturate the differential gain. From these measurements the CMRR was found and can be seen in Figure 28.



(a) CMRR double ended



(b) CMRR single ended

Figure 28: Common mode gain, CMRR, simple current resistive load

As with the cascode, the amplifier performed better with noise rejection at the higher voltage.

3.2 Active Load Differential Amplifier

The active load was constructed using PMOS load. The Schematic can be seen in Figure 29.

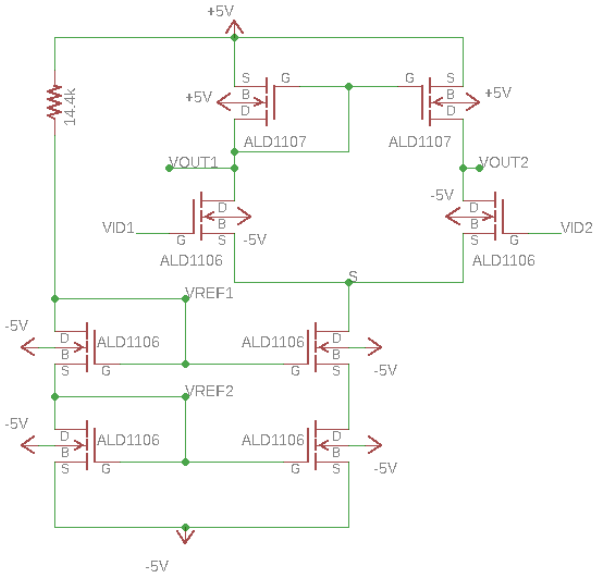


Figure 29: Experimental active load differential amplifier

The VTC for the active load can be seen in Figure 30.

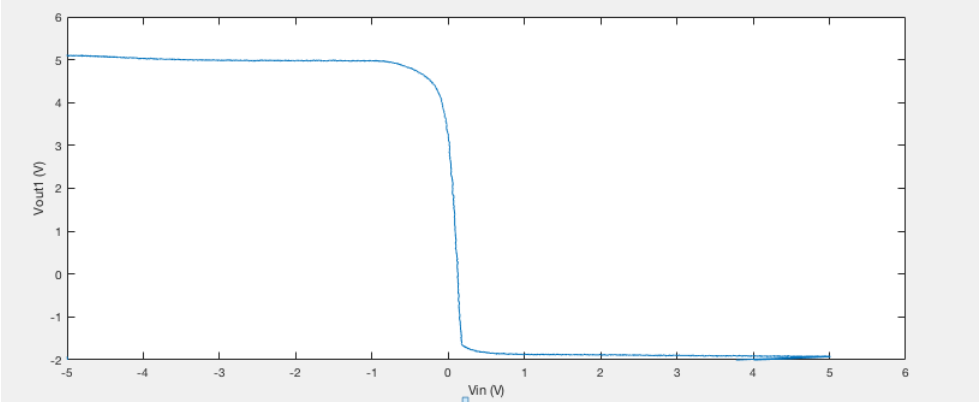


Figure 30: Experimental VTC of active load

The circuit had a much smaller operation range than the resistive load. The differential gain can be seen in Figure 31.

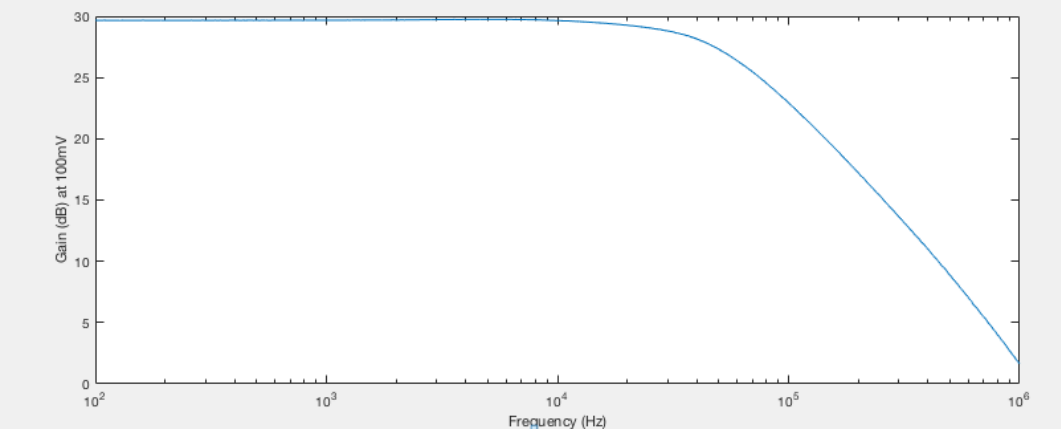
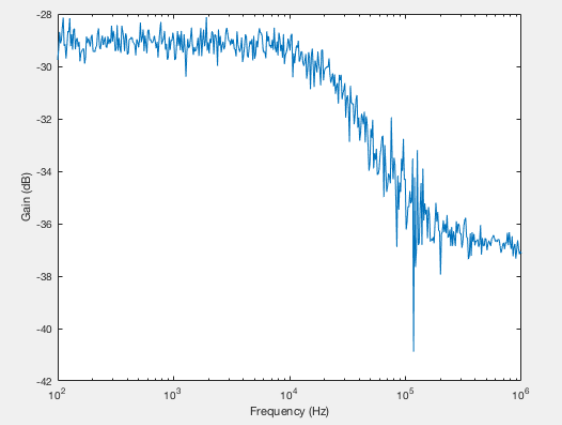
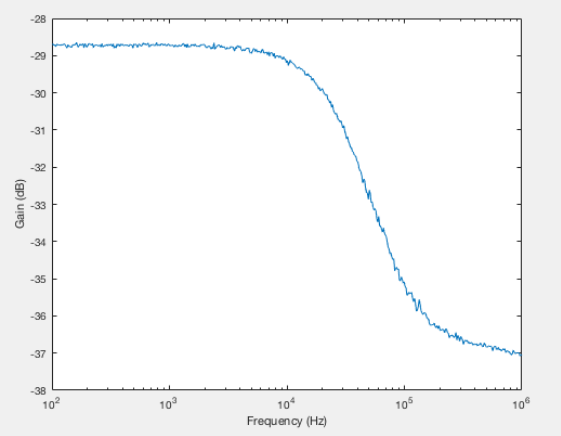


Figure 31: Ad, double ended

The double ended reached higher gain than the single ended. The Acm measured at 100mV and 1V can be seen in Figure 32.



(a) Acm, 100mV



(b) Acm, 1V

Figure 32: Common mode gain, Acm, active load

The commode mode gain was better at the higher voltage. The CMRR can be seen in Figure 33.

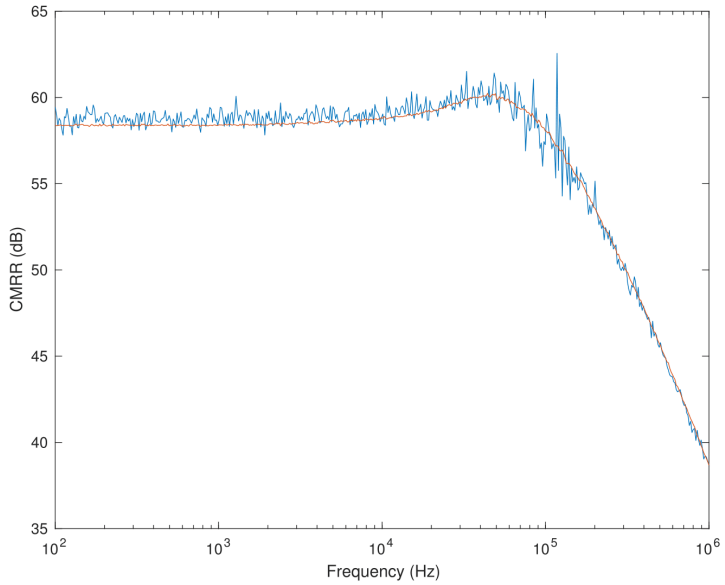


Figure 33: CMRR active load differential amplifier

The CMRR was slightly lower than the resistive, but produced a better gain of 30 dB.

4 Discussion

This lab served as an introduction to differential amplifiers. Specifically, it highlighted the advantages and disadvantages of a resistively loaded and active loaded differential amplifier. All tasks for the lab were completed. However, multiple issues arose during the experimentation process.

When the circuit was functioning correctly, only a few minor deviations were noticeable from the calculated to the experimental results. These differences are most likely due to the equations used during calculations, which did not take every factor of the MOSFETS and circuits into considerations. The values that resulted from these calculations were ideal ones, that were close to what the values actually were. The final values can be seen in Table 5 below.

Table 5: Final values for resistively loaded differential amplifier

Resitively Loaded Differential Amplifier Results		
Components/Nodes	Simulated	Experimental
V_{ref_1}	-3.09 V	-3.13 V
V_{ref_2}	-.056 V	-.062 V
I_{bias}	401μA	397 μA
I_{ref_1}	199μA	197 μA
I_{ref_2}	202 μA	196 μA
R_{ref}	8.125kΩ	14.4kkΩ
R_{D_1}	15kΩ	14.9kΩ
R_{D_2}	15kΩ	14.9kΩ
Ad	23.5 dB	18 dB
Acm	-20.7.5 dB	-55
CMRR 1V	40 dB	90dB

The amplifier did work as expected, but the gain was lacking as seen in the experimental section. One of the most significant observations from this experiment has been the impact of the two different current mirrors on the amplifier. The simple current mirror had the widest compliance range, providing more wiggle room in terms of operation. Current mirrors suffering from wide mismatch would benefit from a change to the simple topology as it would provide a wider range of operation. The cascode suffered from a more narrow range of operation, this however, is not without benefit. The cascode was able to produce a max differentially gain of 18.5dB while the simple current mirror only produced a max gain of 18dB. In addition the cascode featured better CMRR compared to the simple, 90dB compared to 67dB. Overall the cascode provided much better gain performance at the cost of a restricted compliance range.

An active loaded amplifier performed better in terms of gain which is seen in Table 6.

Table 6: Final values for active loaded differential amplifier

Active Loaded Differential Amplifier Results		
Components/Nodes	Simulated	Experimental
V_{ref_1}	-3.07 V	-3.05 V
V_{ref_2}	-.051 V	-.048 V
I_{bias}	401 μA	398 μA
I_{ref_1}	200 μA	202 μA
I_{ref_2}	199 μA	203 μA
R_{ref}	8.125kΩ	14.4kΩ
Ad	29.3 dB	30 dB
Acm	-19.5 dB	-29dB
CMRR 1V	49 dB	59dB

An advantage of the active load amplifier is less passive elements in the circuit are used. Also, the gain is much higher for the single stage analyzed in the lab. Finally, the CMRR is much larger in the single-ended active load, than the single-ended resistive load. The tradeoff, again, being a extremely restricted compliance range compared to the resistive load. This is due to transistor mismatch.

5 Conclusion

The design, simulation, and construction of experiments to measure the performance of a differential amplifier is explored.Two differential amplifiers were tested. The first amplifier is a resistively loaded amplifier, while the second differential amplifier has an active load. The common mode rejection ratio, input common mode voltage range and differential gain verses singled-ended gain were measured. It was found that the active loaded differential amplifier was more efficient with less passive components, and also produced a higher gain than the resistively loaded differential amplifier. The double-ended resistively loaded with cascode current mirror amplifier has a differential gain of 19 dB with a common mode gain of approximately -55 dB and a CMRR max of 90 dB at 1V. The double-ended active loaded amplifier has a max differential gain of 30 dB has a max common mode gain of approximately -29 and a max CMRR of 59 dB. An important lesson learned was about the tradeoff between an optimal operation range and the final gain achievable by a circuit. In addition the benefits of both a simple and cascode current mirror were explored.

References

[1] All About Circuits. (2018) Single-ended differential amplifiers [Online]: https://www.allaboutcircuits.com/textbook/semiconductors/chpt-8/single-ended-differential-amplifiers/

[2] N. W. Emanatoglu. (2018) Task 4 [Online]

[3] N. W. Emanatoglu. (2018) Task 4 briefing [Online]