1. Description

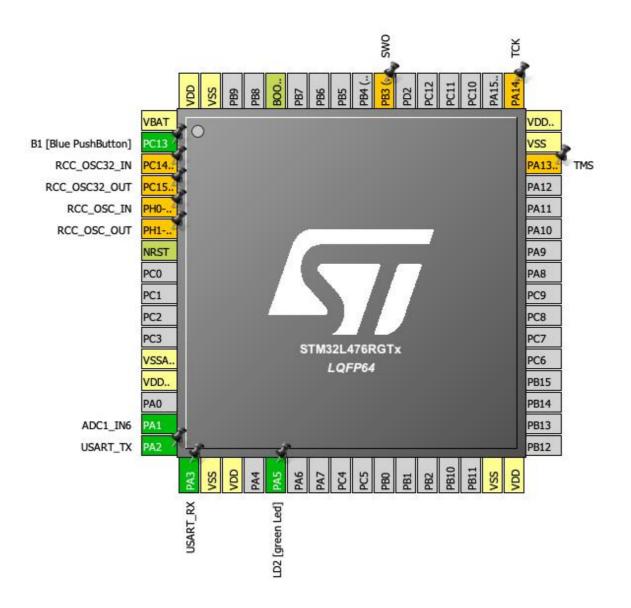
1.1. Project

Project Name	DMA
Board Name	NUCLEO-L476RG
Generated with:	STM32CubeMX 4.26.0
Date	12/12/2018

1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476RGTx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



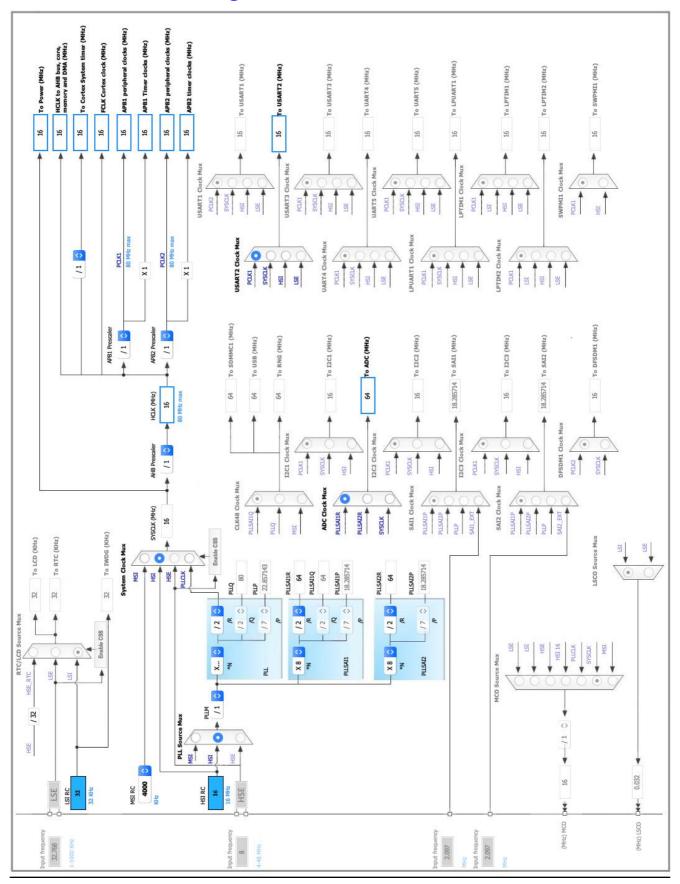
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN (PC14) *	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT (PC15) *	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN (PH0) *	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT (PH1) *	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
15	PA1	I/O	ADC1_IN6	
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
21	PA5 **	I/O	GPIO_Output	LD2 [green Led]
31	VSS	Power		
32	VDD	Power		
46	PA13 (JTMS-SWDIO) *	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDDUSB	Power		
49	PA14 (JTCK-SWCLK) *	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 (JTDO-TRACESWO) *	I/O	SYS_JTDO-SWO	SWO
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

^{**} The pin is affected with an I/O function

^{*} The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



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5. IPs and Middleware Configuration

5.1. ADC1

IN6: IN6 Single-ended

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler Asynchronous clock mode divided by 2 *

Resolution ADC 12-bit resolution

Data Alignment Left alignment *

Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled
DMA Continuous Requests Enabled *

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data overwritten *

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular ConversionsEnableEnable Regular OversamplingDisableNumber Of Conversion1

External Trigger Conversion Source

Timer 4 Trigger Out event *

External Trigger Conversion Edge

Trigger detection on the rising edge

Rank 1

Channel Channel 6
Sampling Time 2.5 Cycles
Offset Number No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

5.2. SYS

Timebase Source: SysTick

5.3. TIM4

Channel1: Output Compare No Output

5.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 10000 *

Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Update Event *

Clear Input:

Clear Input Source Disable

Output Compare No Output Channel 1:

Mode Frozen (used for Timing base)

Pulse (16 bits value) 0
CH Polarity High

5.4. USART2

Mode: Asynchronous

5.4.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable RX Pin Active Level Inversion Disable Data Inversion Disable Disable TX and RX Pins Swapping Overrun Enable DMA on RX Error Enable MSB First Disable

^{*} User modified value

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA1	ADC1_IN6	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USART_RX
Single Mapped Signals	PC14- OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T (PC15)	RCC_OSC32_O UT	n/a	n/a	n/a	
	PH0- OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
	PA13 (JTMS- SWDIO)	SYS_JTMS- SWDIO	n/a	n/a	n/a	TMS
	PA14 (JTCK- SWCLK)	SYS_JTCK- SWCLK	n/a	n/a	n/a	TCK
	PB3 (JTDO- TRACESWO)	SYS_JTDO- SWO	n/a	n/a	n/a	SWO
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Falling edge trigger detection	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [green Led]

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	High *

ADC1: DMA1_Channel1 DMA request Settings:

Mode: Circular *

Peripheral Increment: Disable

Memory Increment: Enable *

Peripheral Data Width: Word *

Memory Data Width: Word *

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
ADC1 and ADC2 interrupts	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38		unused	
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM4 global interrupt	unused		
USART2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
FPU global interrupt		unused	

^{*} User modified value

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476RGTx
Datasheet	025976_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.0



9. Software Project

9.1. Project Settings

Name	Value
Project Name	DMA
Project Folder	/Users/RoastBeefy/Documents/SeniorProject/HAL_Framework/DMA
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_L4 V1.12.0

9.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	