Display Adaptor

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***Abstract*— This document provides an overview on how to design of a display adaptor that can sustain a 100x100 active image with only vertical blanking section.**

***Keywords*— Display Unit, Vertical Blanking, Active Image, Display controller.**

I. INTRODUCTION

This document manifests the various steps involved in the design and implementation of the display adaptor which can display a 100x100 image in RGB format. First, the individual modules for the implementation of the display adaptor have been developed and tested individually. After that we integrated all to form a top module. The basic operation consists of fetching a 24-bit pixel from the system memory and placing it in the active image area one at a time. Each module involved in the development of the display adaptor has been explained in detail below.

II. MODULES

The individual modules involved in the construction of the display adaptor is listed below. These modules were integrated later to form the display adaptor. For this particular design the inputs VBOut, AIPOut, AILOut are initiated to 2, 100 and 100 respectively.

a.) File Read
b.) Dual Buffers
c.) Pixel Counter and Line Counter
d.) Address Counters
e.) Frame MUX
f.) Display Unit

a.) File Read :
The File read module reads the data from the input file and places it into a memory.

b.) Dual Buffers :
The Buffers buf0 and buf1 are the display buffers. They are continuously fed with the image data from the 32 bit wide system bus WData. First buf0 will be filled and once it is full buf1 starts filling with the help of WE0 and WE1 signals.

c.) Pixel Counter and Line Counter :
The Pixel counter and line counter help in identifying the current pixel and line in each cycle.

d.) Address Counters :
The Address Counters give addr0 and addr1 which indicates the address in the buffers from which the data is read to frame buffer.

e.) Frame MUX :
The Frame MUX has three inputs from blanking region, buf0 and buf1. Depending on the signals SelBlank, SelBuf0 and SelBuf1 output changes between blanking pixels and active image pixels.

f.) Display Unit:
The display unit controls all the operations in the display adaptor and is activated when CSDisplay signal becomes high. Once it is activated the first component of vertical blanking pixel will arrive at the frame. In the following two cycles, the other 2 components of the first blanking pixel will arrive at the frame. While the last component arrives the IncPx goes high to increase the PXOut. Here the condition (PxOut == AIPOut -1) is checked to see it is the last pixel in the line. If it is true then, the condition (LineOut == VBOut -1) is checked to see if it is the last line. If the end of blanking region is reached the RE0 signal becomes high in the same cycle enabling SelBuf0 to become high in the next cycle. Now, in the next cycle the first component of the active pixel is read from buffer 0. Signals SelR0, SelG0 and SelB0 become high once every 3 cycles to select the R, G and B components of the pixel. Also, Similar to blanking region all the conditions are checked till the data from buff0 is completely processed. After the last data is read from buff0, signal SyncVB becomes high indicating start of the new blanking region of next frame. After all the data is retrieved, the data is written to a file.

Conclusion:

The verification of the Display Adaptor is performed by giving input, the image data of a 100x100 bmp image. The binary data of the bmp image is retrieved with the help of a python file. Then the header was removed and only the pixel array data was given as input to the display adaptor. After simulation, the binary text from output file is again converted into hexadecimal with the help of another python file. After appending the removed header to this data, the complete set is pasted on a Hex Editor software to create a new BMP image. The output image matches with the input and thus the display adaptor verification is performed

successfully. This process is repeated cyclically between Buf0 and Buf1 twice and thus data of 4 images is again as input and are verified. In this way by combining all the individual modules, we created a top module which shows the successful implementation of a Display Adaptor

REFERENCES

[1] Ahmet Bindal, *Fundamentals Of Computer Architecture and Design, 5th Ed.*