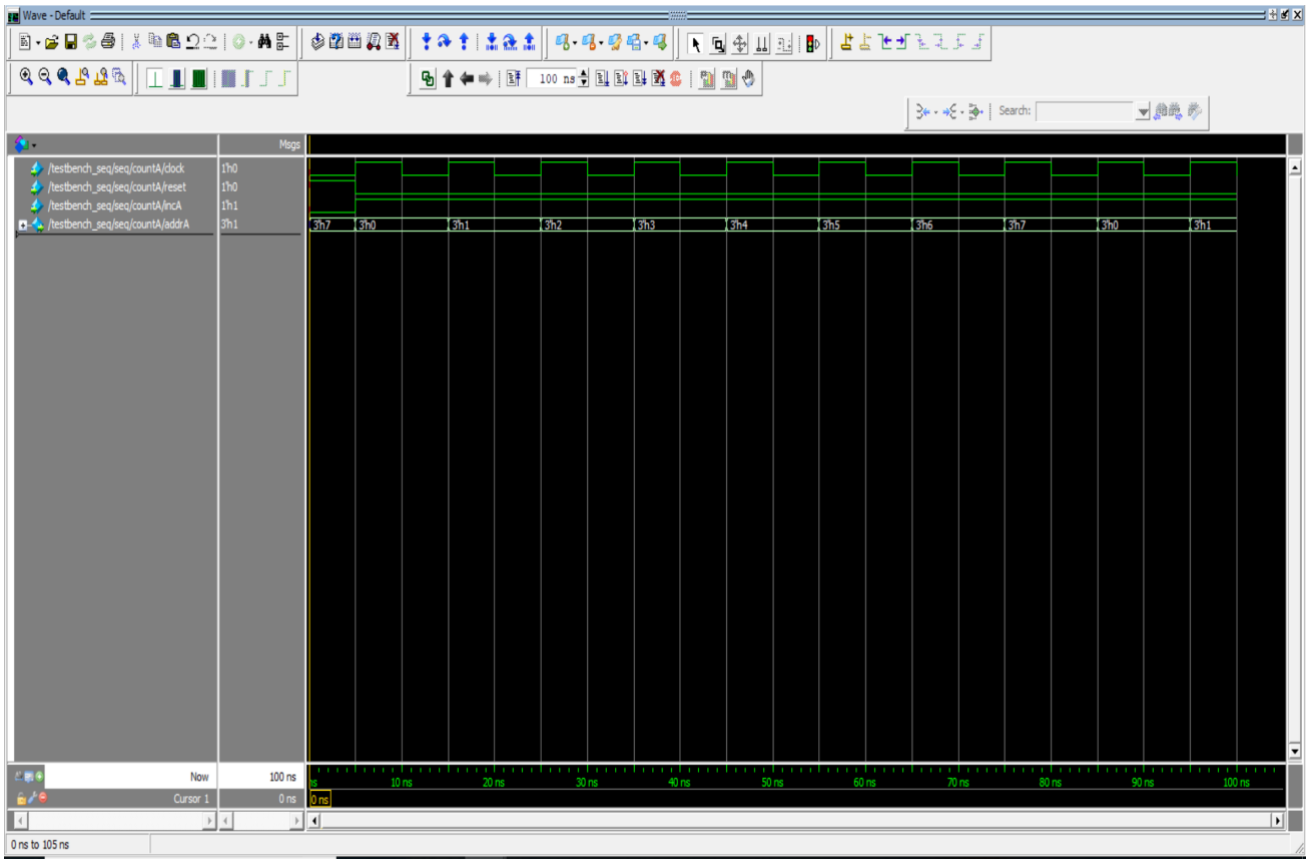
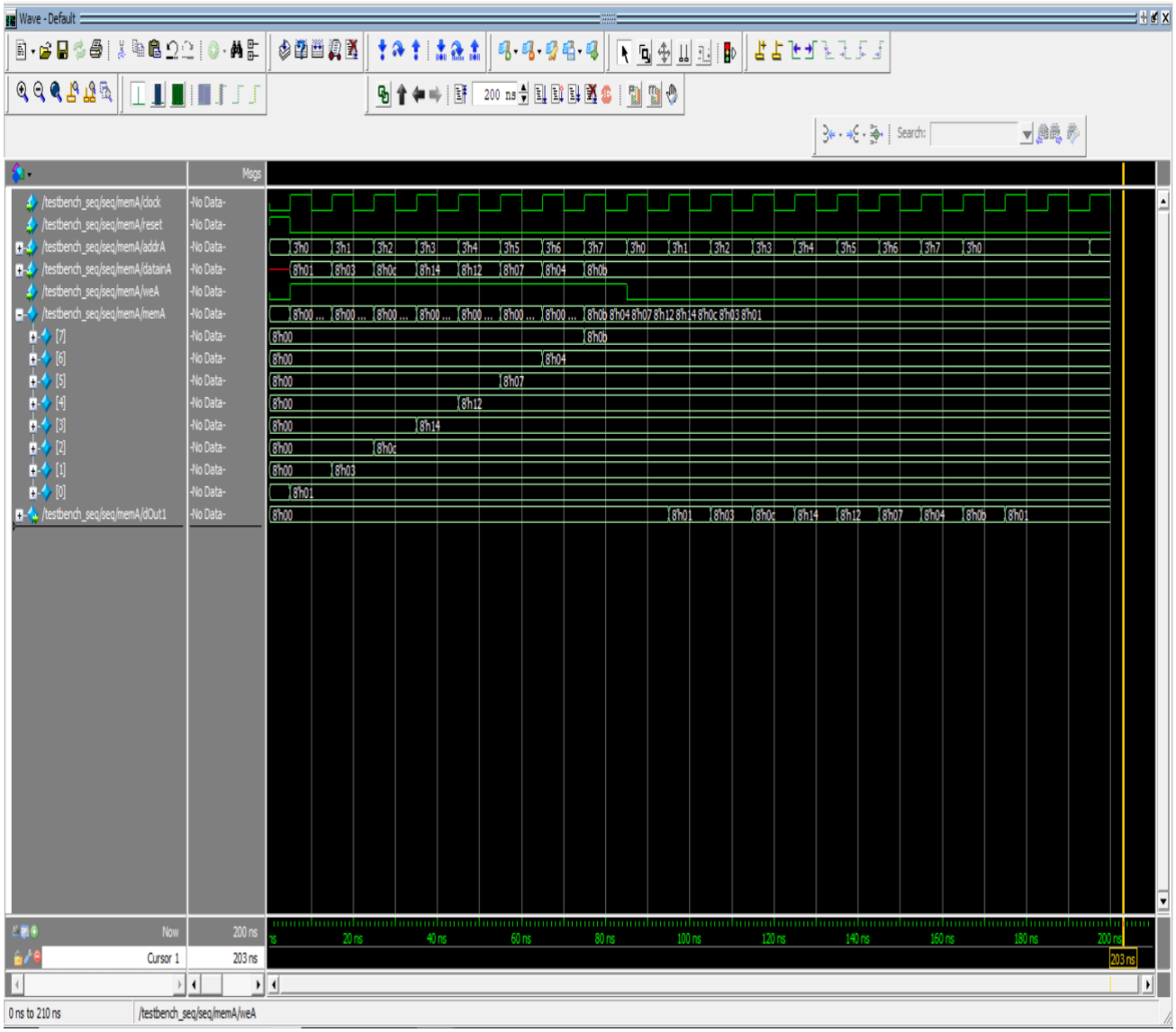
Timing Diagrams:

Counter: The 3 bit counter in the timing diagram generates values from 3'b0 to 3'b111 depending on reset and incA. When incA is high counter value increments and when incA is low counter value remains the same.



Memory: In memory values are written when weA is high and values are read when weA is low. In the timing diagram weA is high for the first eight cycles and then becomes low after 8th cycle allowing to read from memory.



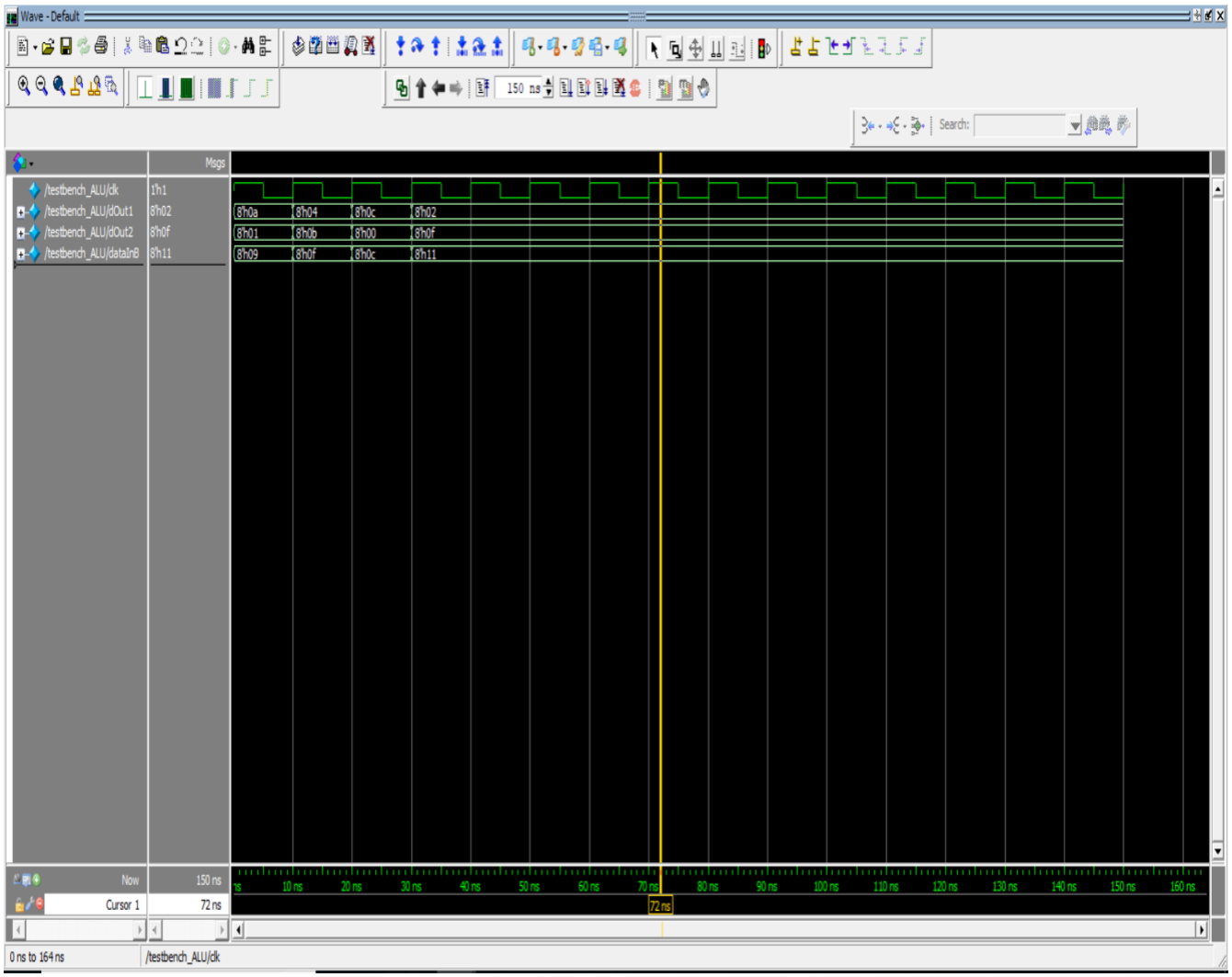
ALU: ALU perform either addition or subtraction depending on the vales of dOut1 and dOut2.

In the 1st cycle since dOut1>dOut2 subtraction should be performed.

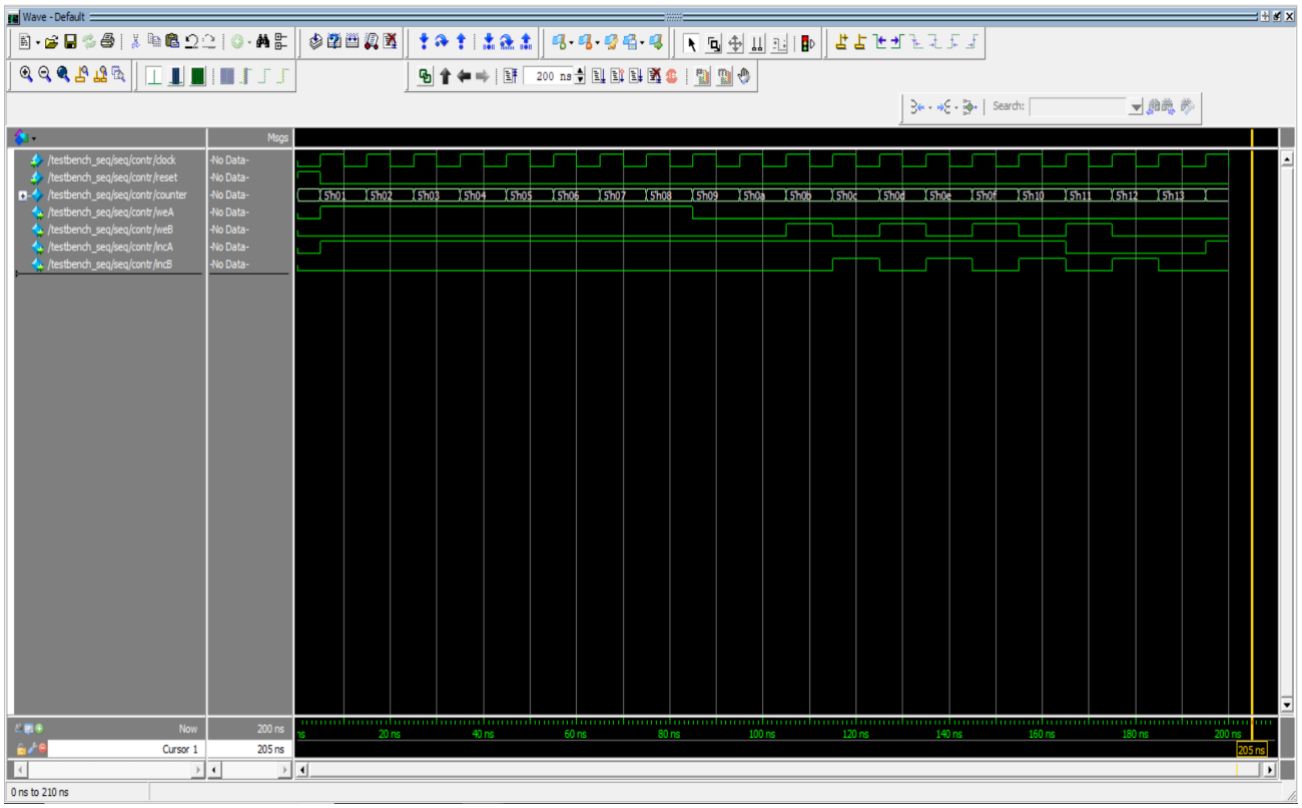
dOut1=8'h0a dOut2=8'h01 expected result: 8'h09

In the 2nd cycle since dOut1<dOut2 addition should be performed.

dOut1=8'h04 dOut2=8'h0b expected result: 8'h0f



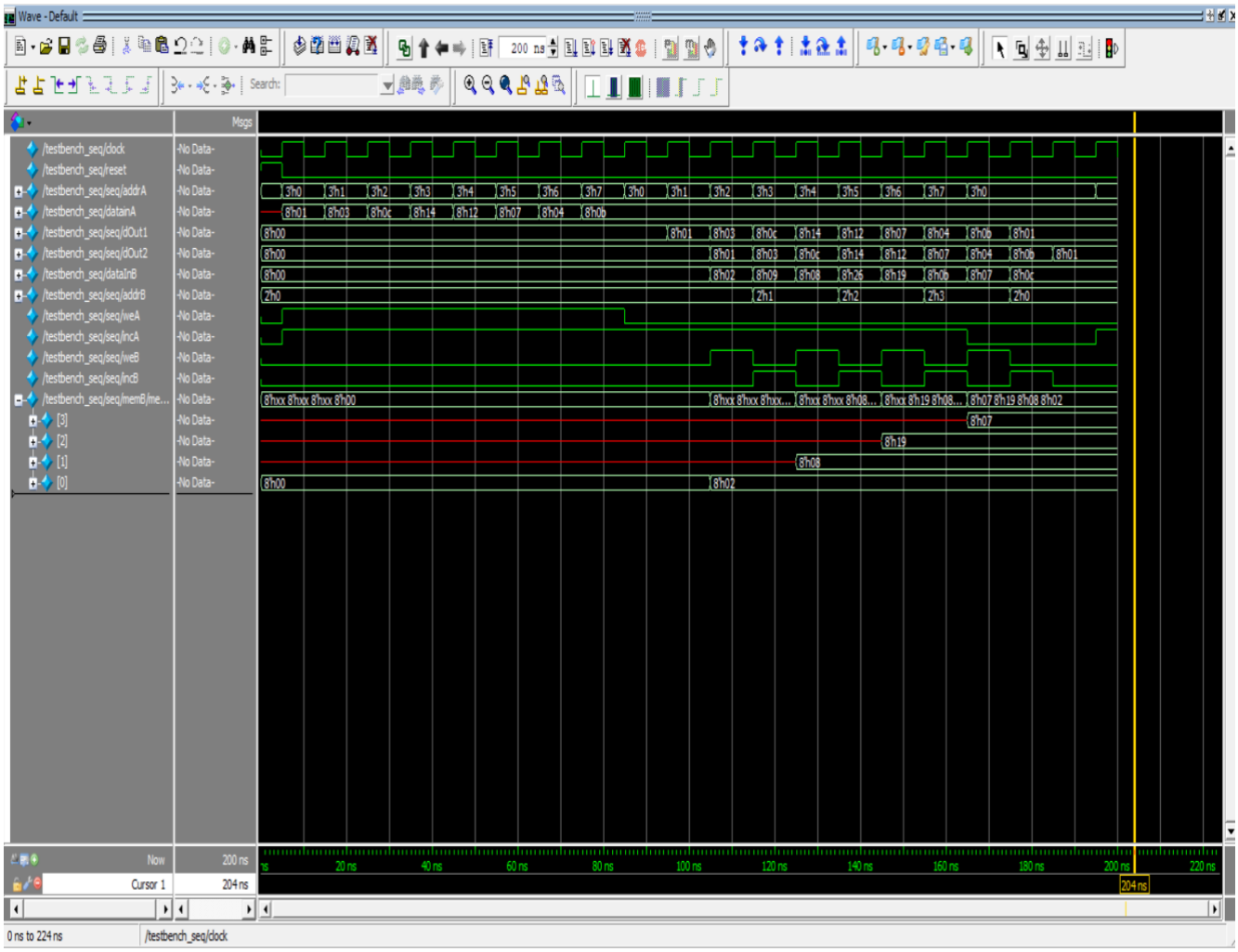
Controller: Controller generates weA, weB, incA, incB signals depending on the 5-bit counter.



Sequential Circuit: In the timing diagram using addrA and dataIn we have written values into memoryA in the first 8 clock cycles. Then we started reading values from memoryA into dOut1 and dOut2. Now depending on the values of dOut1 and dOut2 either addition or subtraction is performed and the result is stored into dataInB as shown below:

Clock Cycle	dOut1	dOut2	Expected Result
11	8'h03	8'h01	8'h02
12	8'h0c	8'h03	8'h09
13	8'h14	8'h0c	8'h08
14	8'h12	8'h14	8'h26
15	8'h07	8'h12	8'h19
16	8'h04	8'h07	8'h0b
17	8'h0b	8'h04	8'h07

Since weB is high only for cycles 11,13,15,17 only those values of dataInB are written into memory.



When reset becomes high all the values in the circuit will automatically be reset. In the timing diagram below reset becomes high in 14th clock cycle so all the values will become 0.