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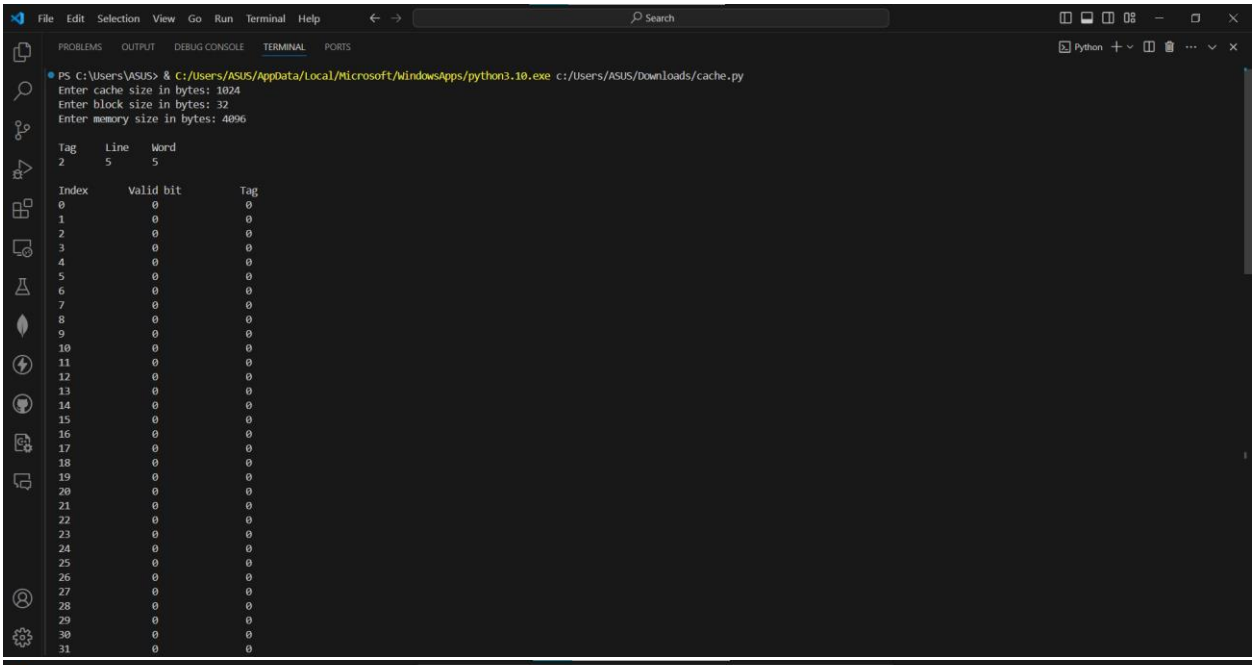
SECTION: ‘L’
CASE STUDY AND PARACACHE

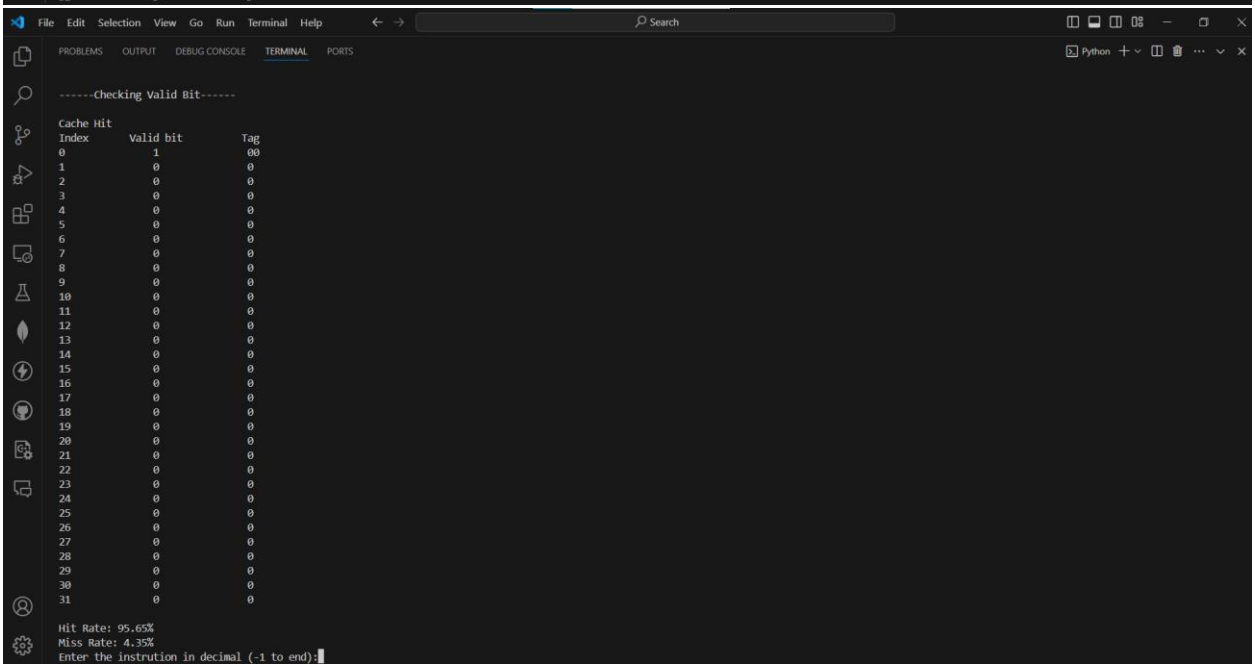
PARACACHE:
INPUT:

```
# Direct mapped cache simulator
import math

def init_table(n):
    matrix = []
    for i in range(n):
        row = [i]  # Assigning the index value as the first element of each row
        for _ in range(1):
            row.append(0)
            row.append("0")
        matrix.append(row)
    return matrix

def print_cache(matrix):
    print("Index\t    Valid bit\t       Tag")
    for row in matrix:
        for element in row:
            print(element, end="\t\t")
        print()

def main():
    cache_size = int(input("Enter cache size in bytes: "))
    block_size = int(input("Enter block size in bytes: "))
    memory_size = int(input("Enter memory size in bytes: "))

    line = cache_size // block_size

    mem_bits = int(math.log2(memory_size))
    line_bits = int(math.log2(line)) #index
    block_bits = int(math.log2(block_size)) #offset
    tag_bits = mem_bits - line_bits - block_bits

    print(f"\nTag\tLine\tWord")
    print(f"{tag_bits}\t{line_bits}\t{block_bits}\n")
    cache_table = []

    cache_table = init_table(block_size)

    print_cache(cache_table)
    hit = 0
    miss = 0
    while True:
        instr = int(input("Enter the instrution in decimal (-1 to end):"))
```

```
        if instr == -1:
            break

        mem_addr = bin(instr)[2:].zfill(mem_bits)
        tag_bin = mem_addr[0:tag_bits]
        index_bin = mem_addr[tag_bits:tag_bits+line_bits] # In string
        index_dec = int(index_bin, 2) # In decimal
        offset_bin = mem_addr[tag_bits+line_bits:] # In string

        print("\nMemory Address:\n")
        print("Tag\t   Index\tOffset")
        print(f"{tag_bin}\t   {index_bin}\t\t {offset_bin}")

        print("\n------Checking Valid Bit------\n")

        if cache_table[index_dec][1] == 0:
            print("Valid bit is 0")
            print("Cache Miss\n")
            miss = miss+1
            cache_table[index_dec][1] = 1  # Make valid bit 1
            cache_table[index_dec][2] = tag_bin # Update the value

        elif cache_table[index_dec][1] == 1:
            if cache_table[index_dec][2] == tag_bin:
                print("Cache Hit")
                hit = hit+1
            else:
                print("Cache Miss")
                miss = miss+1
                cache_table[index_dec][2] = tag_bin

        print_cache(cache_table)
        hit_rate = round((hit/(hit+miss))*100,2)
        miss_rate = round((miss/(hit+miss))*100,2)
        print(f"\nHit Rate: {hit_rate}%\nMiss Rate: {miss_rate}%")

    print("\n------Final Cache Table------\n")
    print_cache(cache_table)

if __name__ == "__main__":
    main()
```

OUTPUT:

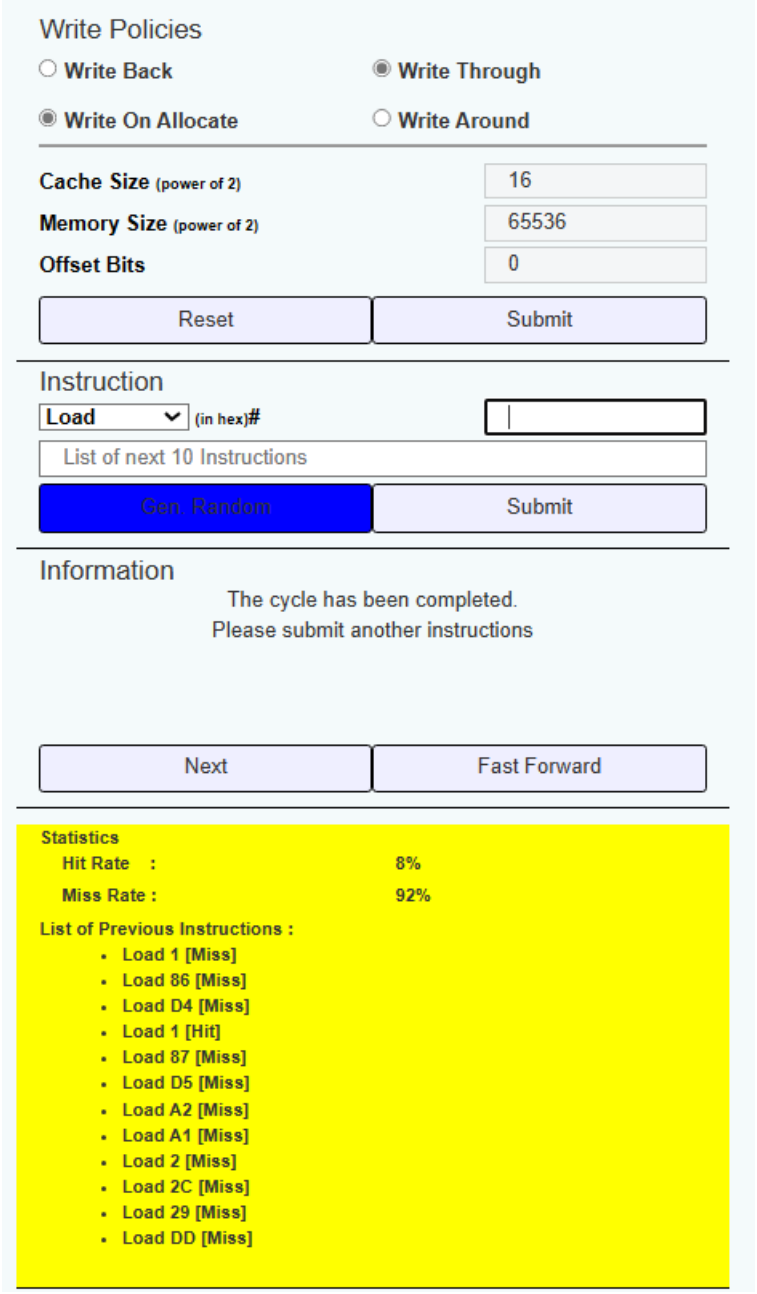

File Edit Selection View Go Run Terminal Help
Search
PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL PORTS
Python
PS C:\Users\ASUS> & C:/Users/ASUS/AppData/Local/Microsoft/WindowsApps/python3.10.exe c:/Users/ASUS/Downloads/cache.py
Enter cache size in bytes: 1024
Enter block size in bytes: 32
Enter memory size in bytes: 4096
Tag Line Word
2 5 5
Index Valid bit Tag
0 0 0
1 0 0
2 0 0
3 0 0
4 0 0
5 0 0
6 0 0
7 0 0
8 0 0
9 0 0
10 0 0
11 0 0
12 0 0
13 0 0
14 0 0
15 0 0
16 0 0
17 0 0
18 0 0
19 0 0
20 0 0
21 0 0
22 0 0
23 0 0
24 0 0
25 0 0
26 0 0
27 0 0
28 0 0
29 0 0
30 0 0
31 0 0


File Edit Selection View Go Run Terminal Help
Search
PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL PORTS
Python
------Checking Valid Bit------
Cache Hit
Index Valid bit Tag
0 1 00
1 0 0
2 0 0
3 0 0
4 0 0
5 0 0
6 0 0
7 0 0
8 0 0
9 0 0
10 0 0
11 0 0
12 0 0
13 0 0
14 0 0
15 0 0
16 0 0
17 0 0
18 0 0
19 0 0
20 0 0
21 0 0
22 0 0
23 0 0
24 0 0
25 0 0
26 0 0
27 0 0
28 0 0
29 0 0
30 0 0
31 0 0
Hit Rate: 95.65%
Miss Rate: 4.35%
Enter the instrution in decimal (-1 to end):

CASE STUDY:

a. 1, 134, 212, 1, 135, 213, 162, 161, 2, 44, 41, 221

Direct Mapped Cache with 16 one-word blocks



DIRECT MAPPED CACHE

Instruction Breakdown

000000001101	1101	0
12 bit	4 bit	0 bit

Memory Block

B. DD W. 0
B. DE W. 0
B. DF W. 0
B. E0 W. 0
B. E1 W. 0
B. E2 W. 0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	1	000000001010	BLOCK A1 WORD 0 - 0	0
2	1	000000000000	BLOCK 2 WORD 0 - 0	0
3	0	-	0	0
4	1	000000001101	BLOCK D4 WORD 0 - 0	0
5	1	000000001101	BLOCK D5 WORD 0 - 0	0
6	1	000000001000	BLOCK 86 WORD 0 - 0	0
7	1	000000001000	BLOCK 87 WORD 0 - 0	0
8	0	-	0	0
9	1	000000000010	BLOCK 29 WORD 0 - 0	0
10	0	-	0	0
11	0	-	0	0
12	1	000000000010	BLOCK 2C WORD 0 - 0	0
13	1	000000001101	BLOCK DD WORD 0 - 0	0
14	0	-	0	0
15	0	-	0	0

Fully Associative with 8 two-word blocks

Replacement Policies

FIFO LRU Random

Write Policies

Write Back Write Through

Write On Allocate Write Around

Cache Size (power of 2) 16

Memory Size (power of 2) 65536

Offset Bits 1

Reset Submit

Instruction

Load (In hex)#

List of next 10 Instructions

Gen. Random Submit

Information

The cycle has been completed.
Please submit another instructions

Next Fast Forward

Statistics

Hit Rate : 25%

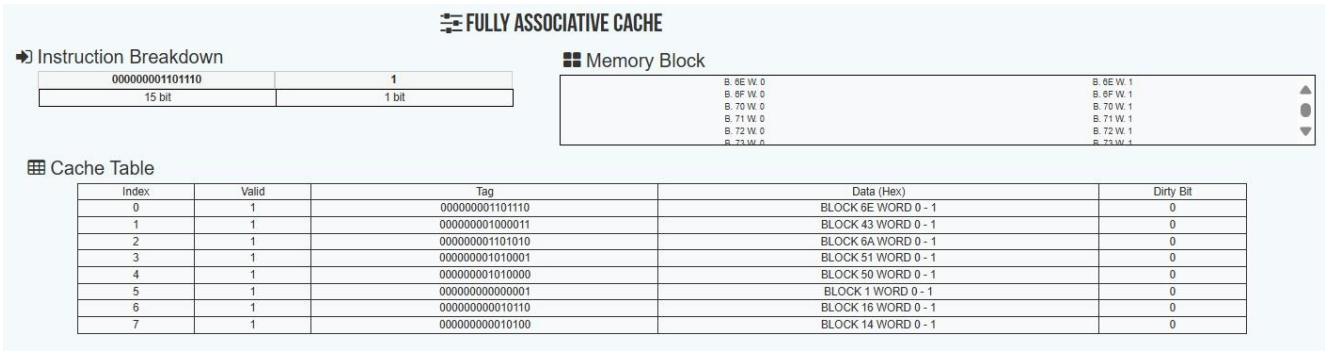
Miss Rate : 75%

List of Previous Instructions :

- Load 1 [Miss]
- Load 86 [Miss]
- Load D4 [Miss]
- Load 1 [Hit]
- Load 87 [Hit]
- Load D5 [Hit]
- Load A2 [Miss]
- Load A1 [Miss]
- Load 2 [Miss]
- Load 2C [Miss]
- Load 29 [Miss]
- Load DD [Miss]

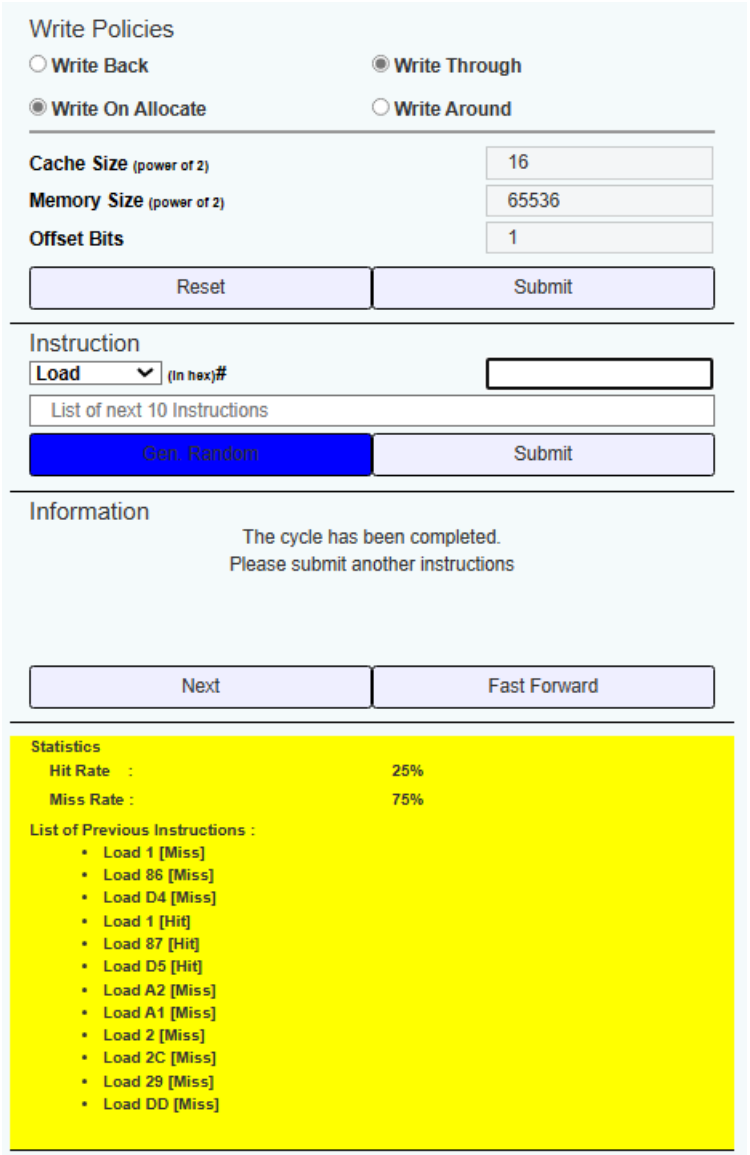
Next Index: 1

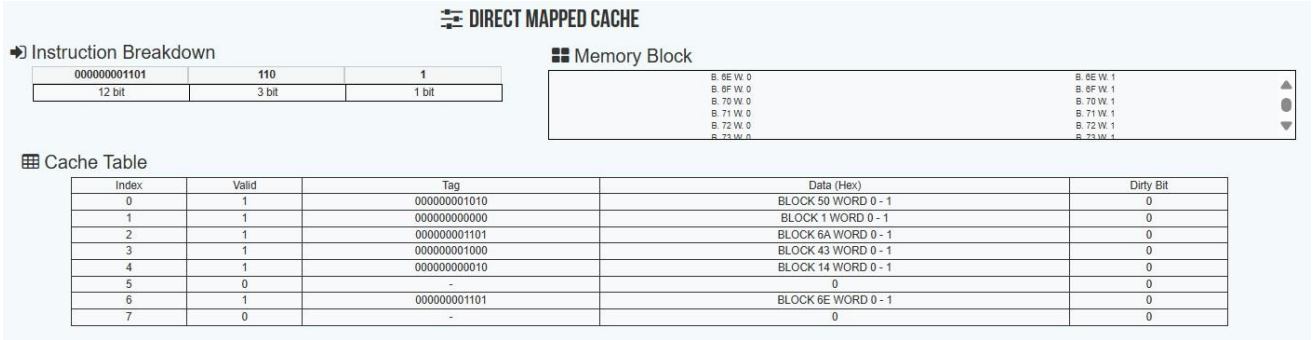
Last Index: 0



Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000000001101110	BLOCK 6E WORD 0 - 1	0
1	1	000000001000011	BLOCK 43 WORD 0 - 1	0
2	1	000000001101010	BLOCK 6A WORD 0 - 1	0
3	1	000000001010001	BLOCK 51 WORD 0 - 1	0
4	1	000000001010000	BLOCK 50 WORD 0 - 1	0
5	1	000000000000001	BLOCK 1 WORD 0 - 1	0
6	1	000000000010110	BLOCK 16 WORD 0 - 1	0
7	1	000000000010100	BLOCK 14 WORD 0 - 1	0

1 way Set Associative with 8 two-word blocks

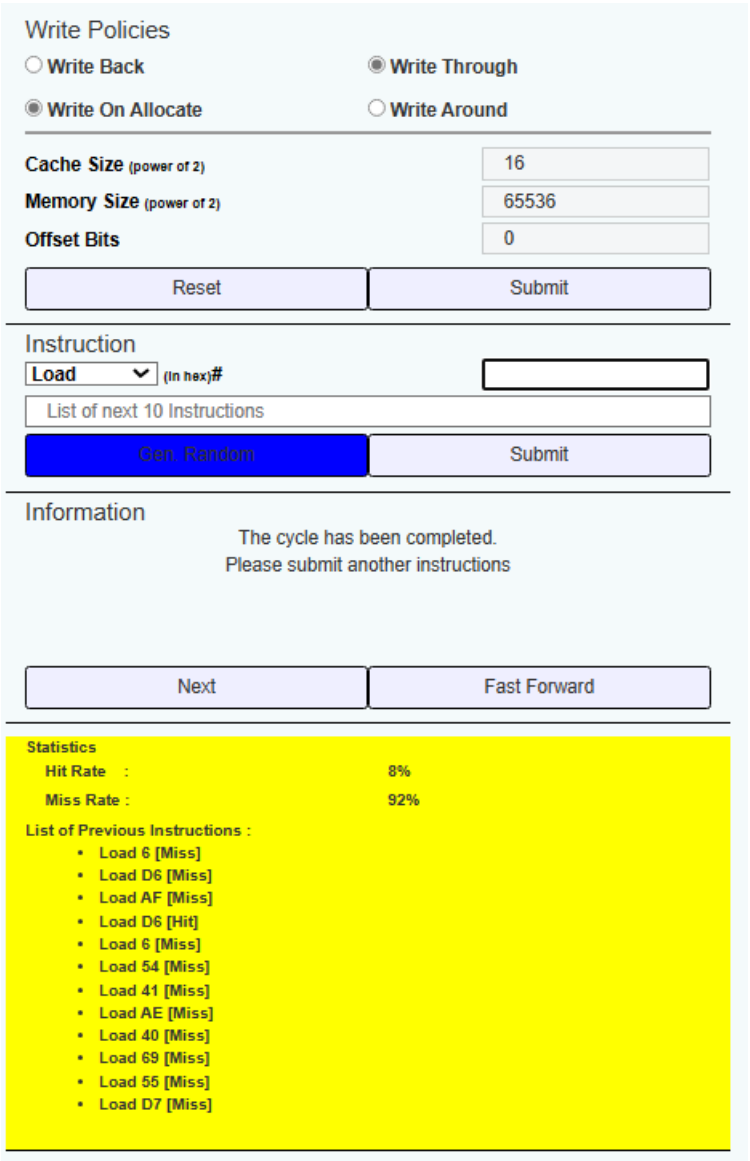


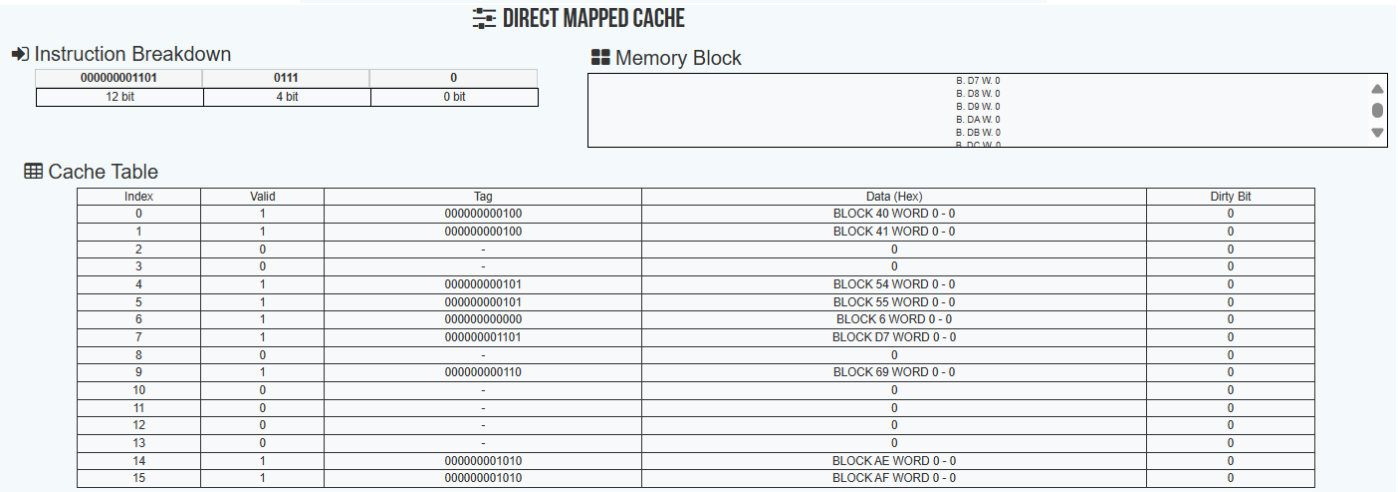


Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000000001010	BLOCK 50 WORD 0 - 1	0
1	1	000000000000	BLOCK 1 WORD 0 - 1	0
2	1	000000001101	BLOCK 6A WORD 0 - 1	0
3	1	000000001000	BLOCK 43 WORD 0 - 1	0
4	1	000000000010	BLOCK 14 WORD 0 - 1	0
5	0	-	0	0
6	1	000000001101	BLOCK 6E WORD 0 - 1	0
7	0	-	0	0

b. 6, 214, 175, 214, 6, 84, 65, 174, 64, 105, 85, 215

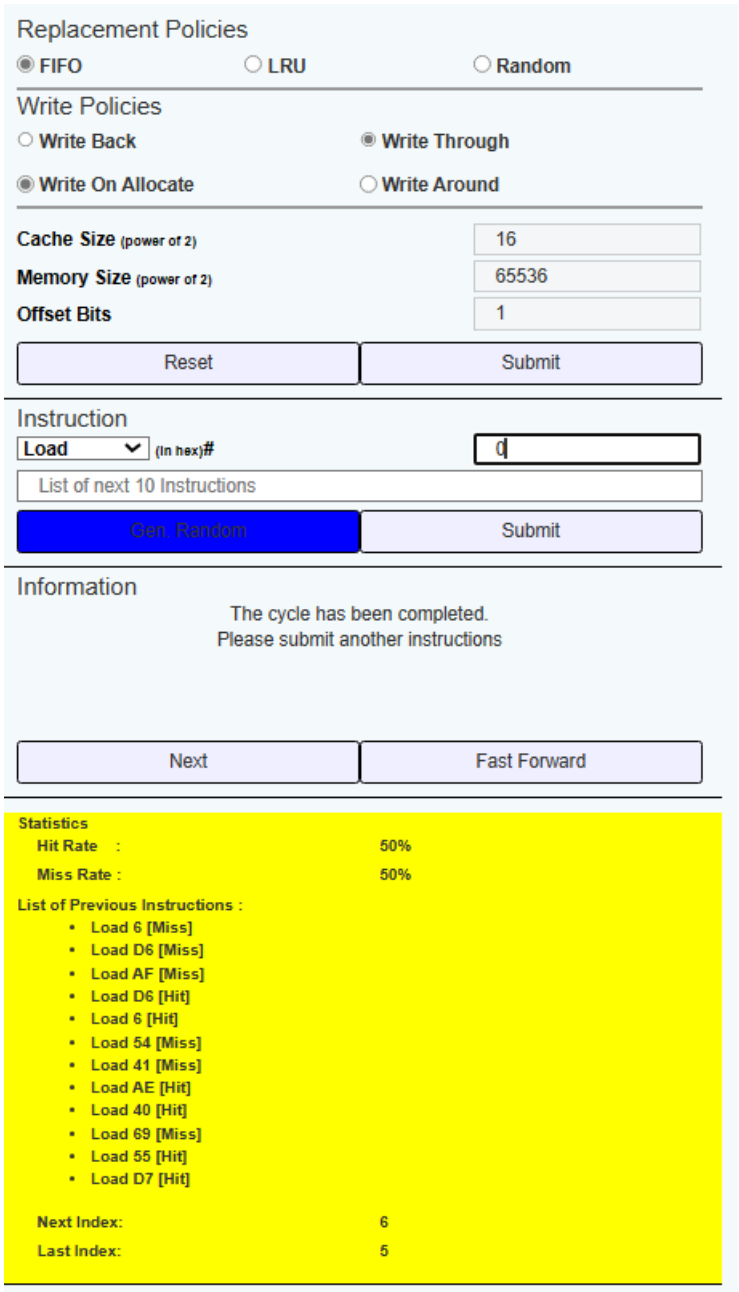
Direct Mapped Cache with 16 one-word blocks

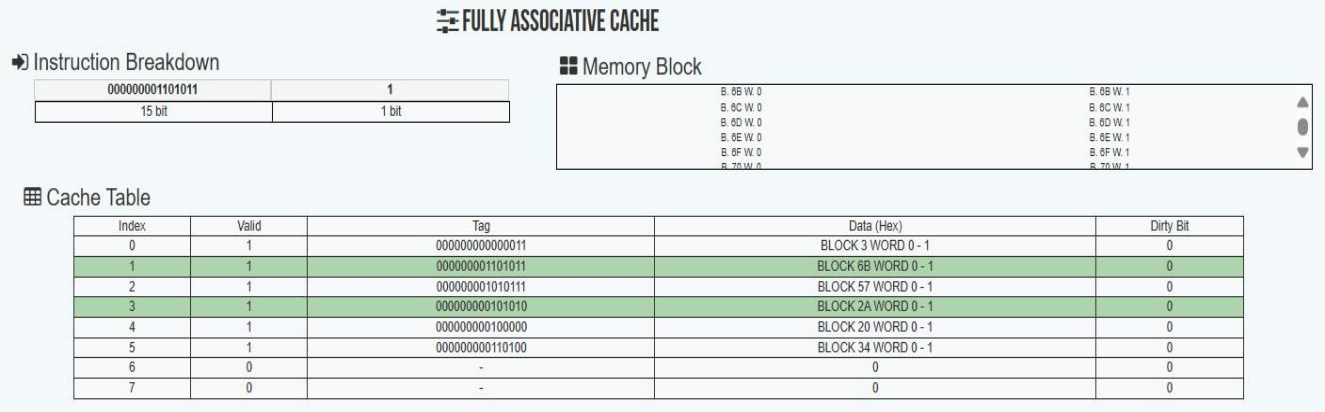




Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000000000100	BLOCK 40 WORD 0 - 0	0
1	1	000000000100	BLOCK 41 WORD 0 - 0	0
2	0	-	0	0
3	0	-	0	0
4	1	000000000101	BLOCK 54 WORD 0 - 0	0
5	1	000000000101	BLOCK 55 WORD 0 - 0	0
6	1	000000000000	BLOCK 6 WORD 0 - 0	0
7	1	000000001101	BLOCK D7 WORD 0 - 0	0
8	0	-	0	0
9	1	000000000110	BLOCK 69 WORD 0 - 0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	1	000000001010	BLOCK AE WORD 0 - 0	0
15	1	000000001010	BLOCK AF WORD 0 - 0	0

Fully Associative with 8 two-word blocks





Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000000000000011	BLOCK 3 WORD 0 - 1	0
1	1	000000001101011	BLOCK 6B WORD 0 - 1	0
2	1	000000001010111	BLOCK 57 WORD 0 - 1	0
3	1	000000000101010	BLOCK 2A WORD 0 - 1	0
4	1	000000000100000	BLOCK 20 WORD 0 - 1	0
5	1	000000000110100	BLOCK 34 WORD 0 - 1	0
6	0	-	0	0
7	0	-	0	0

1 way Set Associative with 8 two-word blocks

Write Policies

- ○ Write Back
- ◉ Write Through
- ◉ Write On Allocate
- ○ Write Around

Cache Size (power of 2)	16
Memory Size (power of 2)	65536
Offset Bits	1

Reset | Submit

Instruction

Load (In hex)#

List of next 10 Instructions

Gen. Random | Submit

Information

The cycle has been completed.
Please submit another instructions

Next | Fast Forward

Statistics

Hit Rate : 33%

Miss Rate : 67%

List of Previous Instructions :

- Load 6 [Miss]
- Load D6 [Miss]
- Load AF [Miss]
- Load D6 [Hit]
- Load 6 [Miss]
- Load 54 [Miss]
- Load 41 [Miss]
- Load AE [Hit]
- Load 40 [Hit]
- Load 69 [Miss]
- Load 55 [Hit]
- Load D7 [Miss]

DIRECT MAPPED CACHE

Instruction Breakdown

000000001101	011	1
12 bit	3 bit	1 bit

Memory Block

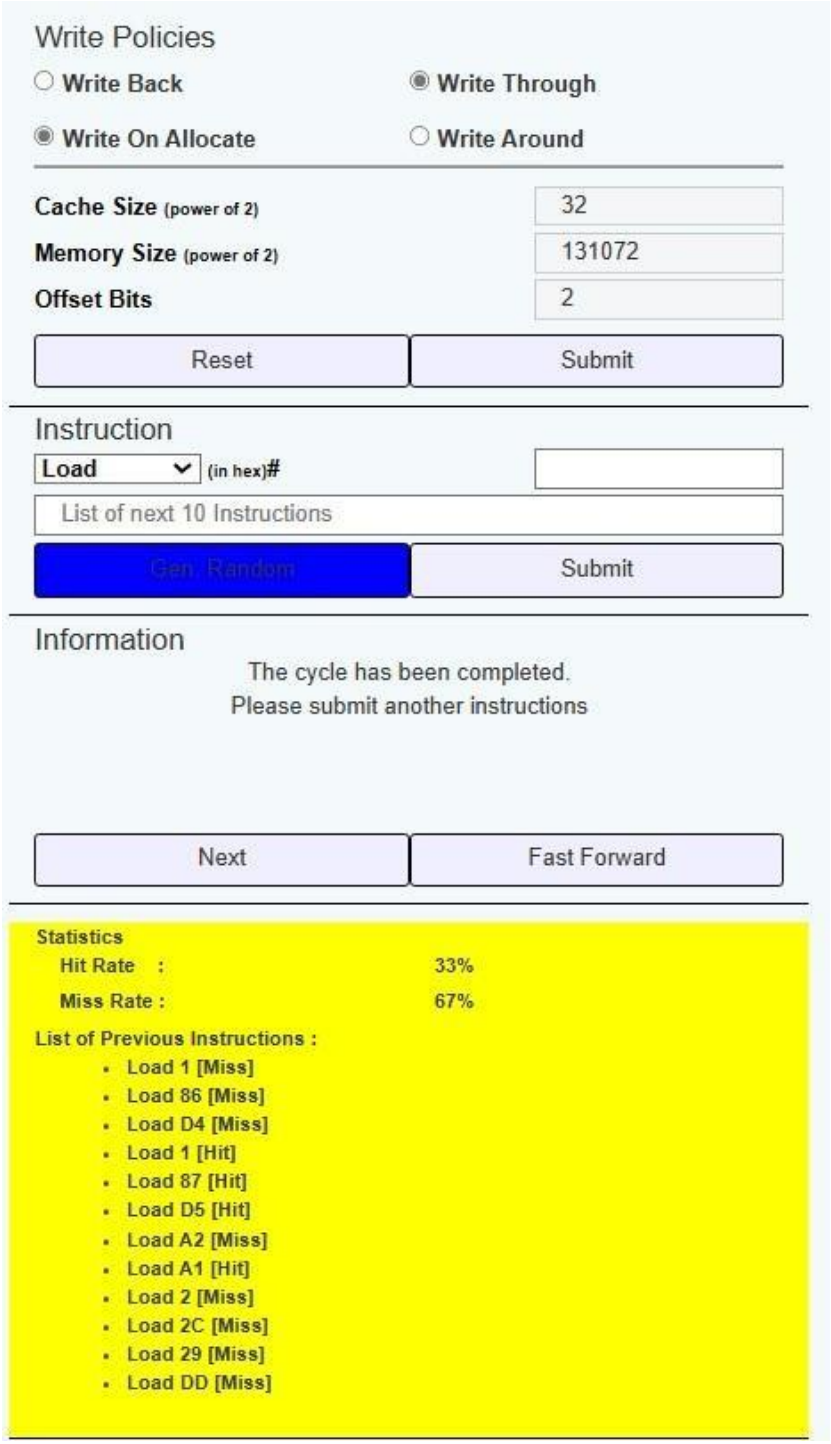
B. 6B W. 0	B. 6B W. 1
B. 6C W. 0	B. 6C W. 1
B. 6D W. 0	B. 6D W. 1
B. 6E W. 0	B. 6E W. 1
B. 6F W. 0	B. 6F W. 1
B. 70 W. 0	B. 70 W. 1

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000000000100	BLOCK 20 WORD 0 - 1	0
1	0	-	0	0
2	1	000000000101	BLOCK 2A WORD 0 - 1	0
3	1	000000001101	BLOCK 6B WORD 0 - 1	0
4	1	000000000110	BLOCK 34 WORD 0 - 1	0
5	0	-	0	0
6	0	-	0	0
7	1	000000001010	BLOCK 57 WORD 0 - 1	0

f. Para cache Simulator- Cache size: 32 words, Memory Size: 131072 words

a) Write Through



DIRECT MAPPED CACHE

Instruction Breakdown

000000000110	111	01
12 bit	3 bit	2 bit

Memory Block

B. 0 W. 0	B. 0 W. 1	B. 0 W. 2	B. 0 W. 3
B. 1 W. 0	B. 1 W. 1	B. 1 W. 2	B. 1 W. 3
B. 2 W. 0	B. 2 W. 1	B. 2 W. 2	B. 2 W. 3
B. 3 W. 0	B. 3 W. 1	B. 3 W. 2	B. 3 W. 3
B. 4 W. 0	B. 4 W. 1	B. 4 W. 2	B. 4 W. 3
B. 5 W. 0	B. 5 W. 1	B. 5 W. 2	B. 5 W. 3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000000000000	BLOCK 0 WORD 0 - 3	0
1	1	000000000100	BLOCK 21 WORD 0 - 3	0
2	1	000000000001	BLOCK A WORD 0 - 3	0
3	1	000000000001	BLOCK B WORD 0 - 3	0
4	0	-	0	0
5	1	000000000110	BLOCK 35 WORD 0 - 3	0
6	0	-	0	0
7	1	000000000110	BLOCK 37 WORD 0 - 3	0

a) Write back

Write Policies

(●) Write Back ( ) Write Through

(●) Write On Allocate ( ) Write Around

Cache Size (power of 2) 32

Memory Size (power of 2) 131072

Offset Bits 2

Reset | Submit

Instruction

Load (in hex)#

List of next 10 Instructions

Gen. Random | Submit

Information

The cycle has been completed.
Please submit another instructions

Next | Fast Forward

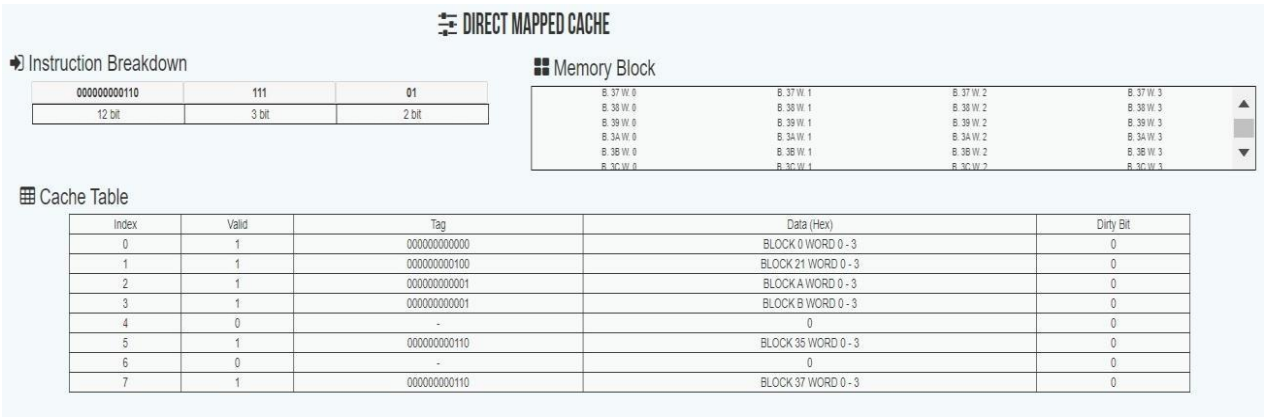
Statistics

Hit Rate : 33%

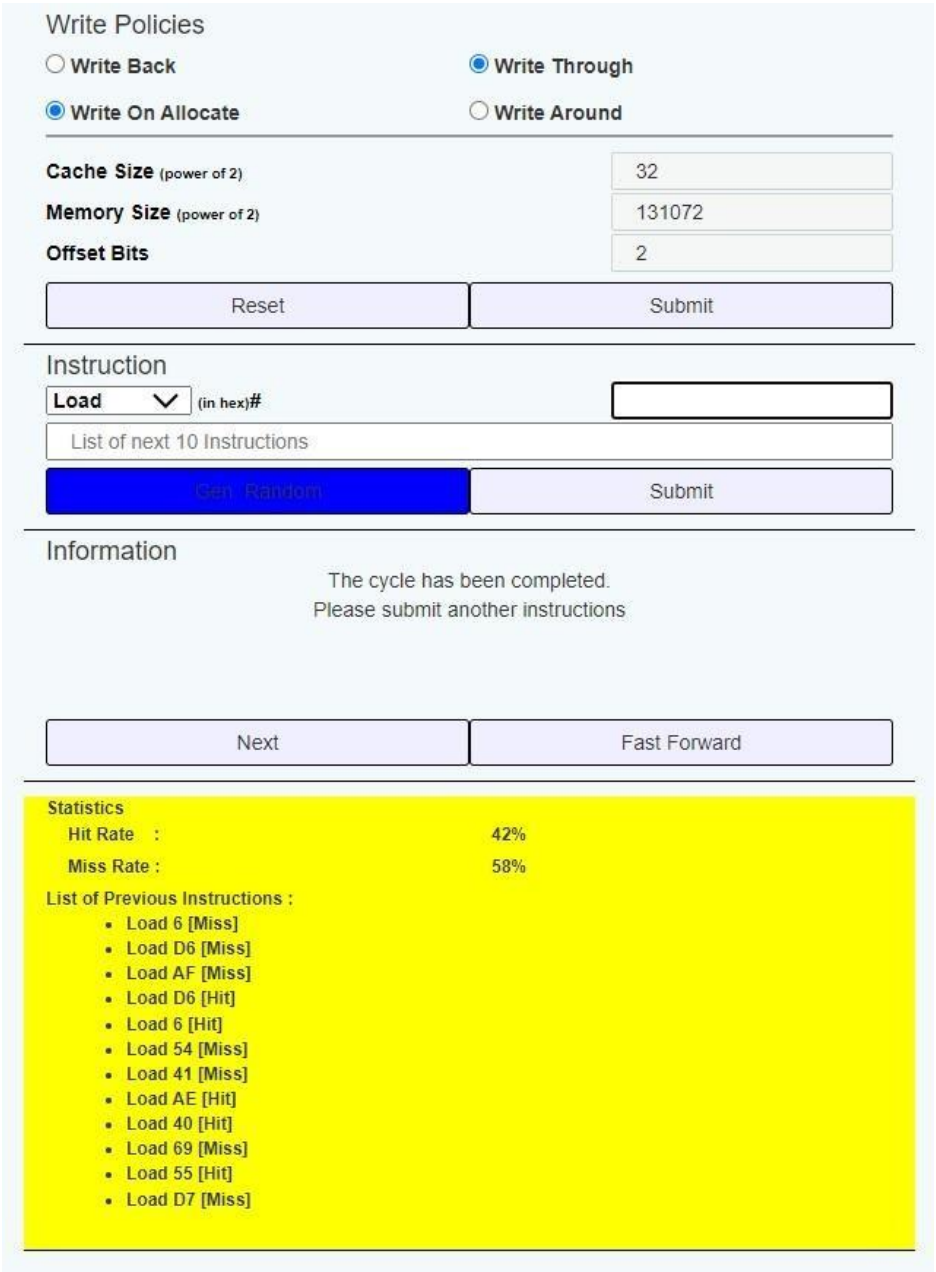
Miss Rate : 67%

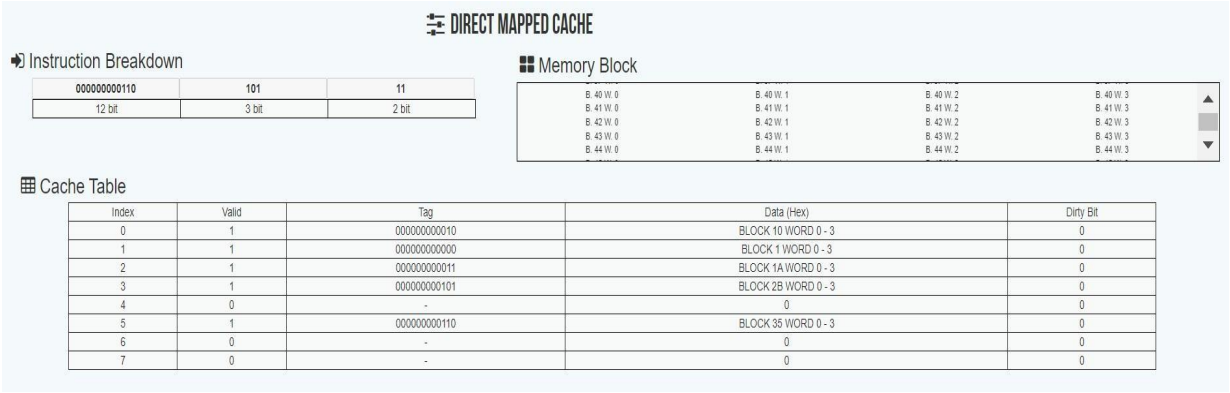
List of Previous Instructions :

- Load 1 [Miss]
- Load 86 [Miss]
- Load D4 [Miss]
- Load 1 [Hit]
- Load 87 [Hit]
- Load D5 [Hit]
- Load A2 [Miss]
- Load A1 [Hit]
- Load 2 [Miss]
- Load 2C [Miss]
- Load 29 [Miss]
- Load DD [Miss]

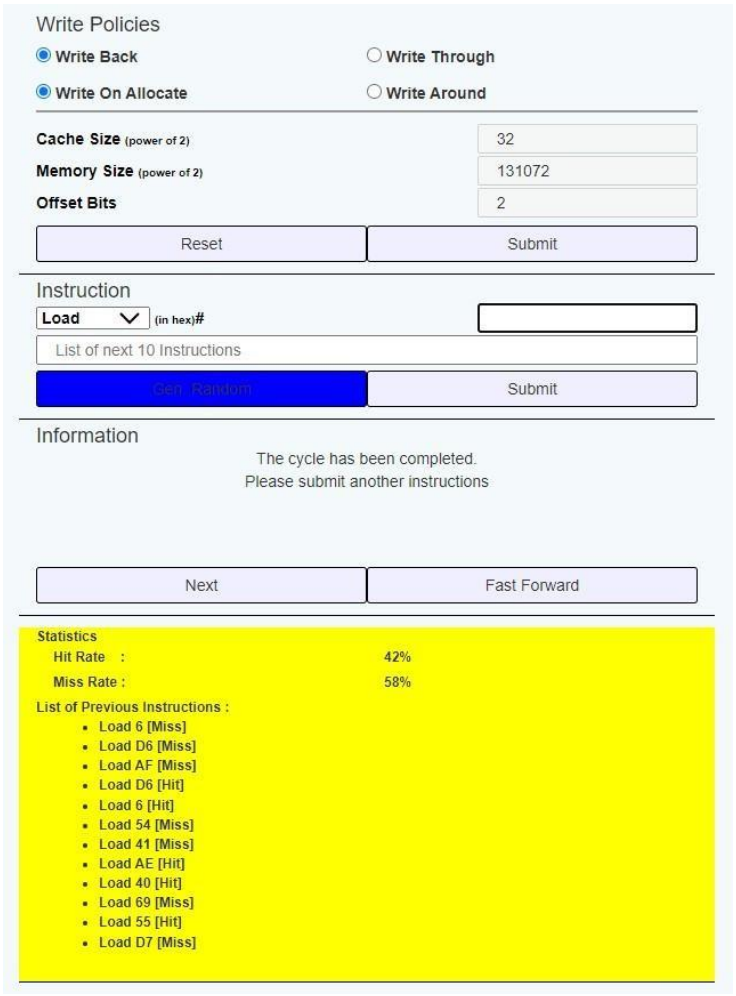


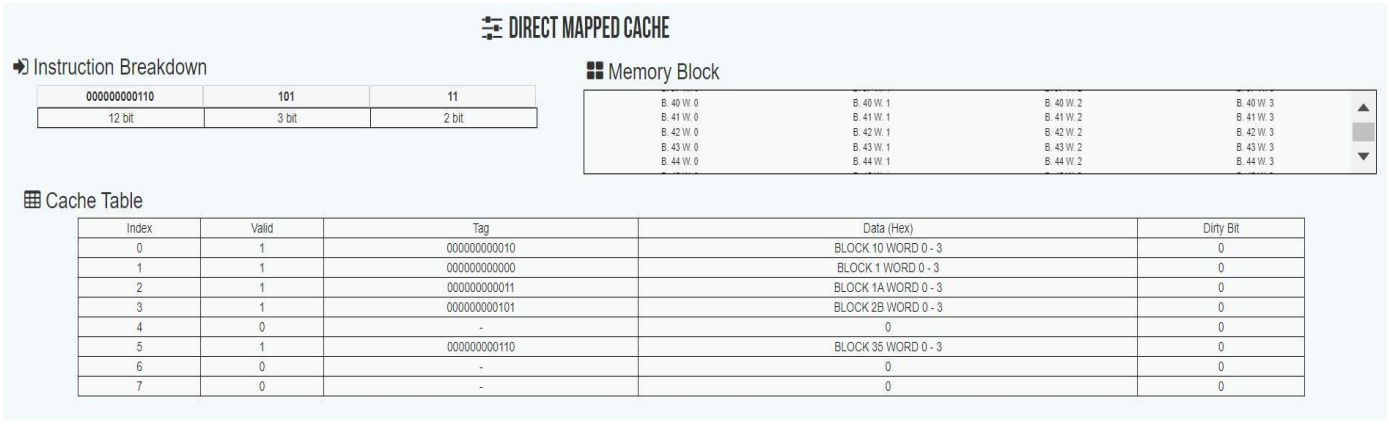
b) Write through




DIRECT MAPPED CACHE
Instruction Breakdown
000000000110
101
11
12 bit
3 bit
2 bit
Memory Block
B. 40 W. 0
B. 40 W. 1
B. 40 W. 2
B. 40 W. 3
B. 41 W. 0
B. 41 W. 1
B. 41 W. 2
B. 41 W. 3
B. 42 W. 0
B. 42 W. 1
B. 42 W. 2
B. 42 W. 3
B. 43 W. 0
B. 43 W. 1
B. 43 W. 2
B. 43 W. 3
B. 44 W. 0
B. 44 W. 1
B. 44 W. 2
B. 44 W. 3
Cache Table
Index
Valid
Tag
Data (Hex)
Dirty Bit
0
1
000000000010
BLOCK 10 WORD 0 - 3
0
1
1
000000000000
BLOCK 1 WORD 0 - 3
0
2
1
000000000011
BLOCK 1A WORD 0 - 3
0
3
1
000000000101
BLOCK 2B WORD 0 - 3
0
4
0
-
0
0
5
1
000000000110
BLOCK 35 WORD 0 - 3
0
6
0
-
0
0
7
0
-
0
0

b Writeback


Write Policies
Write Back
Write Through
Write On Allocate
Write Around
Cache Size (power of 2)
32
Memory Size (power of 2)
131072
Offset Bits
2
Reset
Submit
Instruction
Load
(in hex)#
List of next 10 Instructions
Gen Random
Submit
Information
The cycle has been completed.
Please submit another instructions
Next
Fast Forward
Statistics
Hit Rate :
42%
Miss Rate :
58%
List of Previous Instructions :
Load 6 [Miss]
Load D6 [Miss]
Load AF [Miss]
Load D6 [Hit]
Load 6 [Hit]
Load 54 [Miss]
Load 41 [Miss]
Load AE [Hit]
Load 40 [Hit]
Load 69 [Miss]
Load 55 [Hit]
Load D7 [Miss]


DIRECT MAPPED CACHE
Instruction Breakdown
000000000110
101
11
12 bit
3 bit
2 bit
Memory Block
B. 40 W. 0
B. 40 W. 1
B. 40 W. 2
B. 40 W. 3
B. 41 W. 0
B. 41 W. 1
B. 41 W. 2
B. 41 W. 3
B. 42 W. 0
B. 42 W. 1
B. 42 W. 2
B. 42 W. 3
B. 43 W. 0
B. 43 W. 1
B. 43 W. 2
B. 43 W. 3
B. 44 W. 0
B. 44 W. 1
B. 44 W. 2
B. 44 W. 3
Cache Table
Index
Valid
Tag
Data (Hex)
Dirty Bit
0
1
000000000010
BLOCK 10 WORD 0 - 3
0
1
1
000000000000
BLOCK 1 WORD 0 - 3
0
2
1
000000000011
BLOCK 1A WORD 0 - 3
0
3
1
000000000101
BLOCK 2B WORD 0 - 3
0
4
0
-
0
0
5
1
000000000110
BLOCK 35 WORD 0 - 3
0
6
0
-
0
0
7
0
-
0
0