

Vineet Chadalavada

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EDUCATION

University of North Carolina at Charlotte, Charlotte, NC

Doctor of Philosophy (PhD) in Electrical and Computer Engineering

Aug 2023 – May 2026

Master of Science (MS) in Computer Engineering

Jan 2022 – Dec 2023

Sathyabama Institute of Science and Technology, Chennai, India

Bachelor of Engineering (BE) in Electrical and Electronics Engineering

Jul 2016 – May 2020

PROFESSIONAL EXPERIENCE

Graduate Research Assistant

May 2024 – Aug 2024

- Developed a deep learning model using LSTM networks that improved RUL prediction accuracy for SRAM memory chips by 96%, under varying temperature and voltage conditions, enabling better lifecycle management and reliability assessment for memory hardware.
- Identified and modeled degradation patterns to enable proactive maintenance, leading to a reduction in unexpected hardware failures and improving reliability metrics for memory hardware.

Graduate Research Assistant

May 2023 – Aug 2023

- Developed and validated RTL designs for cryptographic accelerators, debugging FPGA-based implementations for side-channel vulnerabilities using waveform analysis and timing simulations.
- Automated functional verification workflows using machine learning to detect anomalies in power traces, optimizing RTL performance for secure hardware architectures.

Graduate Teaching Assistant

Aug 2022 – Present

- Developed a project on simulating RISC-V pipelined decoder using C.
- Facilitated enhanced learning experiences by designing and evaluating projects.
- Devised a project focused on computing flight time using coordinates, showcasing a hands-on approach to practical learning.
- Led TA classes, evaluated assignments, assisted students in navigating coursework.
- Logic System Design: Assessed assignments, guided students, managed a class of 94 students.

ACADEMIC PROJECTS

Design and Verification of a UART Interface with FIFO Buffering (Xilinx Vivado, Verilog)

- Implemented UART receiver and transmitter using register and flag-based interfaces, simulated readback functionality, and validated data flow through TXRX registers.
- Replaced the interface with a FIFO buffer, developed a state machine to transfer data from buffer to RAM, and performed classification before transmitting via UART.
- Conducted waveform analysis, verified outputs through simulation.

Multi-Processor Architecture (RISC-V, Visual Studio Code, C)

- Implemented a cache coherence system for a 4-processor architecture with 4 Level-1 64KB caches.
- Orchestrated a seamless connection to a shared 1MB memory through a System MemBus.
- Implemented Bus Arbiter, ensured efficient MemBus access control and MESI cache coherence scheme.

Predictive Maintenance Alert System for Engine (Python, Random Forest, Time-Series Analysis)

- Developed a data-driven alert system utilizing NASA's C-MAPSS dataset, predicting Remaining Useful Life (RUL) of engines with high accuracy, enabling proactive maintenance decisions.
- Implemented real-time maintenance classification and alert generation, categorizing engine health into critical risk levels.

TECHNICAL SKILLS

Programming: C, Embedded C, C++, Python, VHDL, Verilog

Software Tools: AutoCADD, MATLAB, Simulink, MAGIC VLSI, Xilinx VIVADO, Cadence, Code Composer Studio, LaTeX

Microcontrollers and FPGAs: ARM Cortex M4, TI MSP 430, Raspberry Pi, Zynq-7000, Xilinx Atrix-7

Cryptography/Security: SCA, AES, Secure Boot Authentication, Physical Unclonable Functions, Dynamic Partial Reconfiguration

EXTRACURRICULAR ACTIVITIES

- Developed and presented a novel cryptographic framework utilizing Ring Oscillator PUF for secure boot authentication and dynamic partial reconfiguration, addressing bitstream modification vulnerabilities, at HOST 2023 conference in San Jose.
- Treasurer, Kappa Phi Chapter, Eta Kappa Nu, IEEE, University of North Carolina at Charlotte.
- Treasurer, Graduate Professional Student Government (GPSG), University of North Carolina at Charlotte.
- Chair, Student Activity and Fee Commission (SAFC), University of North Carolina at Charlotte.