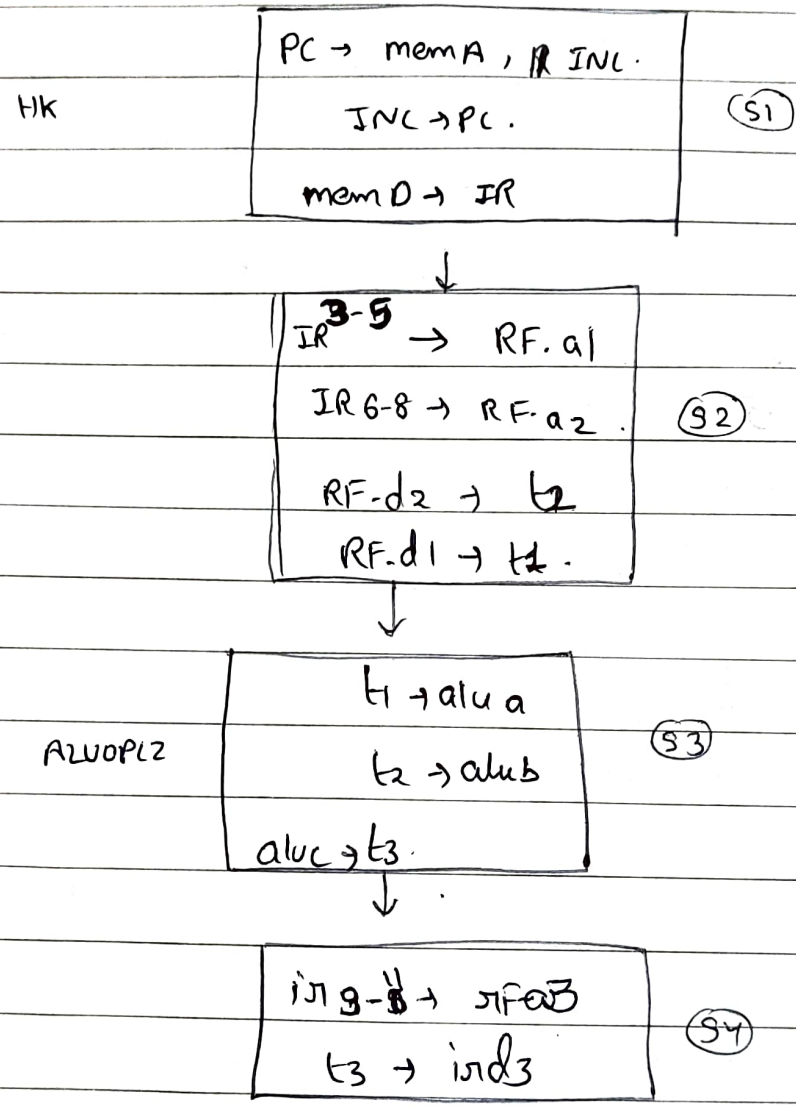
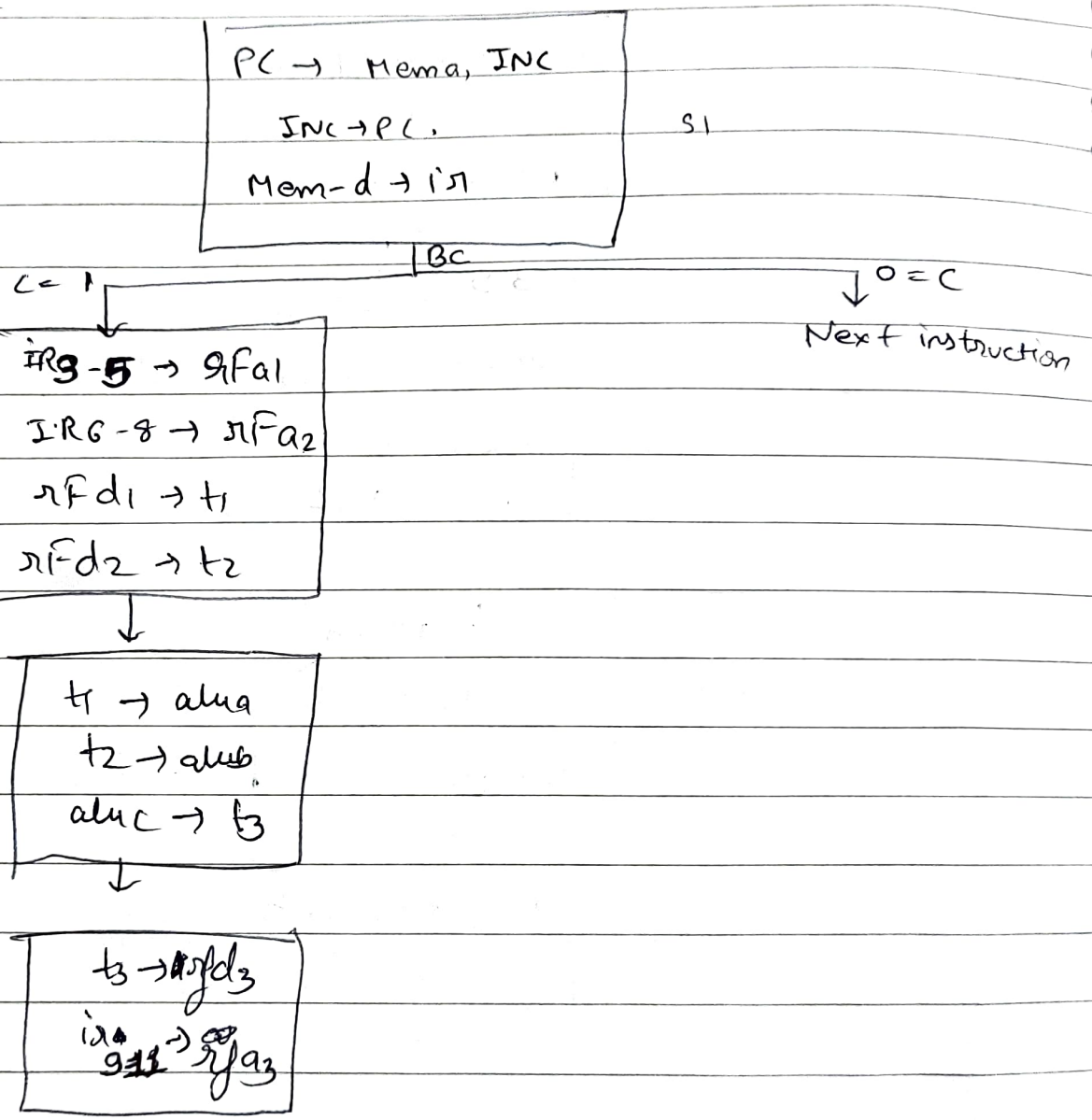
__/__/____

1. ADD RC, RA, RB.


HK
PC → memA, IR INC.
INC → PC.
memD → IR
S1
IR 3-5 → RF.a1
IR 6-8 → RF.a2.
S2
RF.d2 → t2
RF.d1 → t1.
ALUOPCZ
t1 → alu a
t2 → alu b
S3
aluc → t3.
ir 9-11 → rf a3
t3 → ind3
S4

__/__/____

2. ADC.


PC → Mema, INC
INC → PC.
Mem-d → IR
S1
Bc
C = 1
0 = C
Next instruction
IR 3-5 → RFa1
IR 6-8 → RFa2
S2
RFd1 → t1
RFd2 → t2
t1 → alua
S3
t2 → alub
aluc → t3
S4.
t3 → RFd3
RFa3

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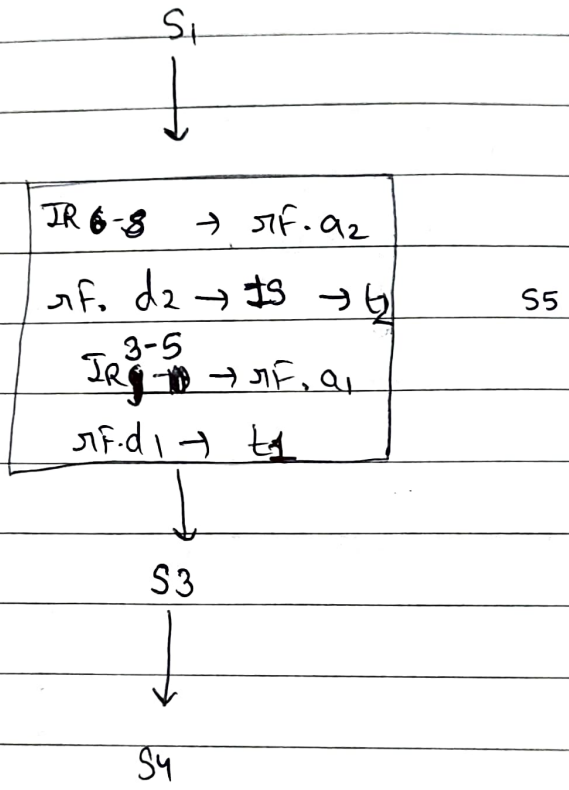
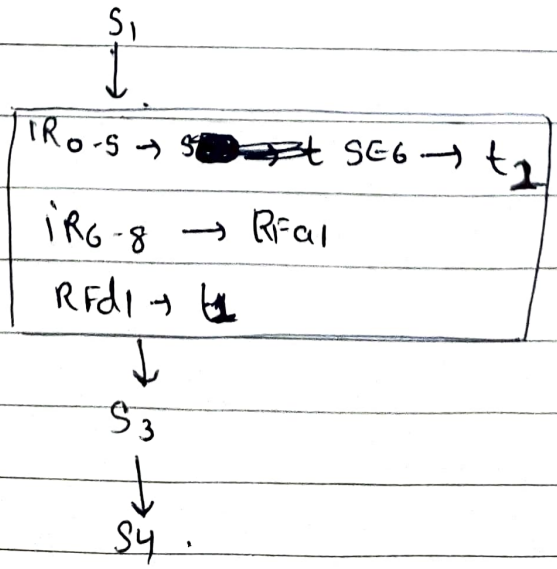
3. ADZ at BC

check Z = 0 or 1. (also S_1 → Z=0 → Next Instruction, Z=1 → $S_2 \rightarrow S_3 \rightarrow S_4$.)

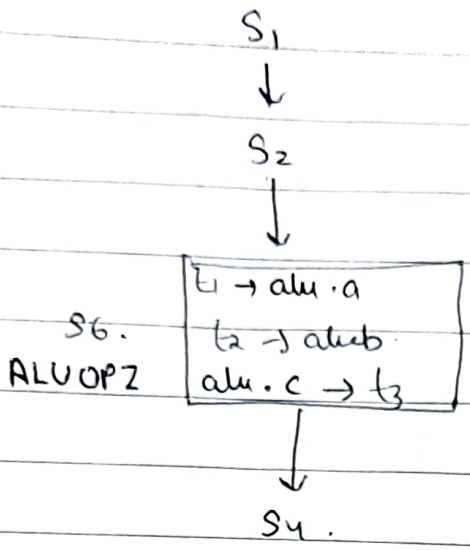
4. ADL



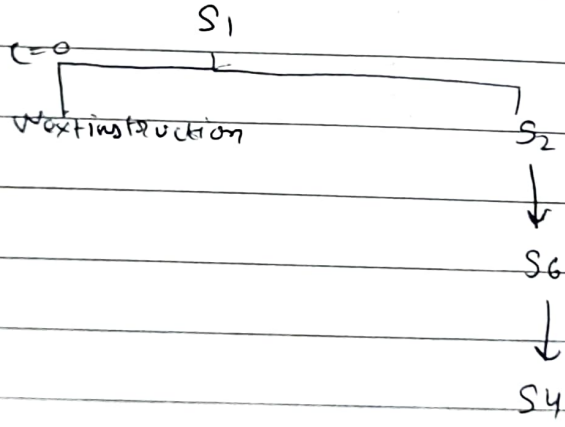
5. ADI



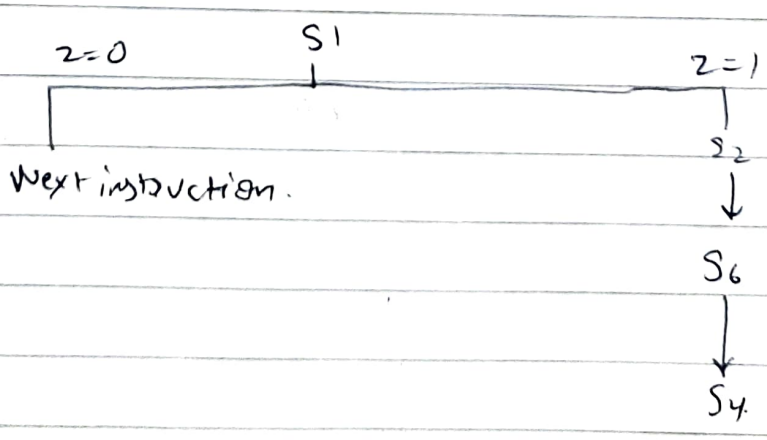
6. NDV RC, RA, RB.



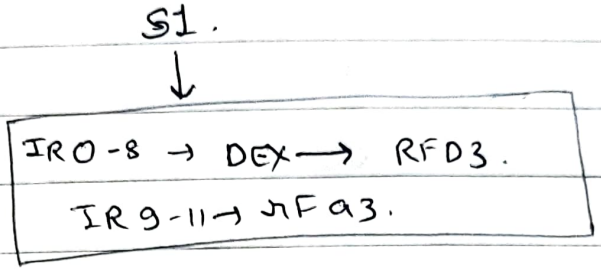
7.



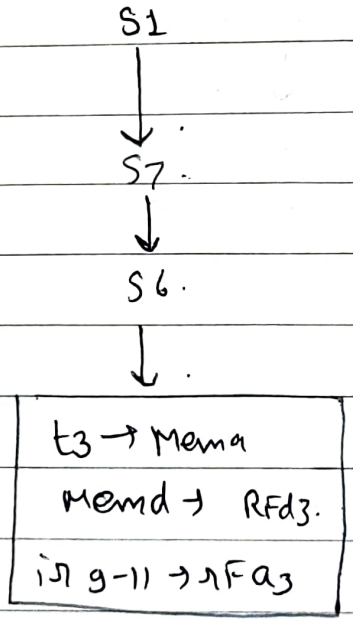
8.



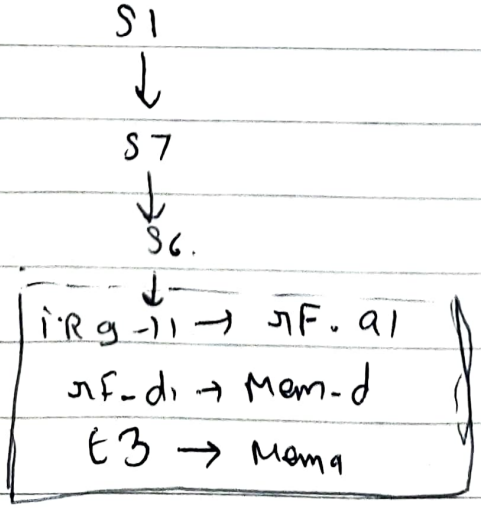
9. LHI RA, IMM.



10. LW RA, RB, IMM.



11 SW.



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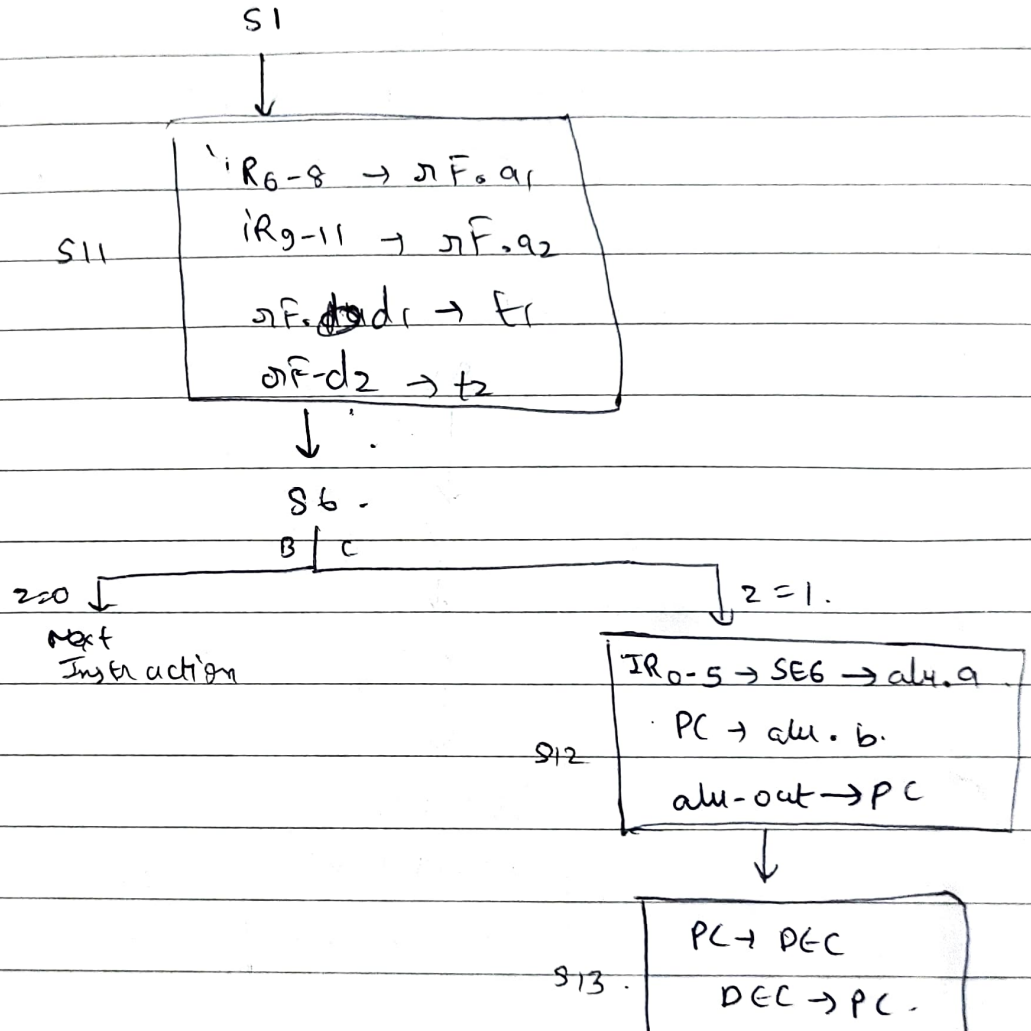
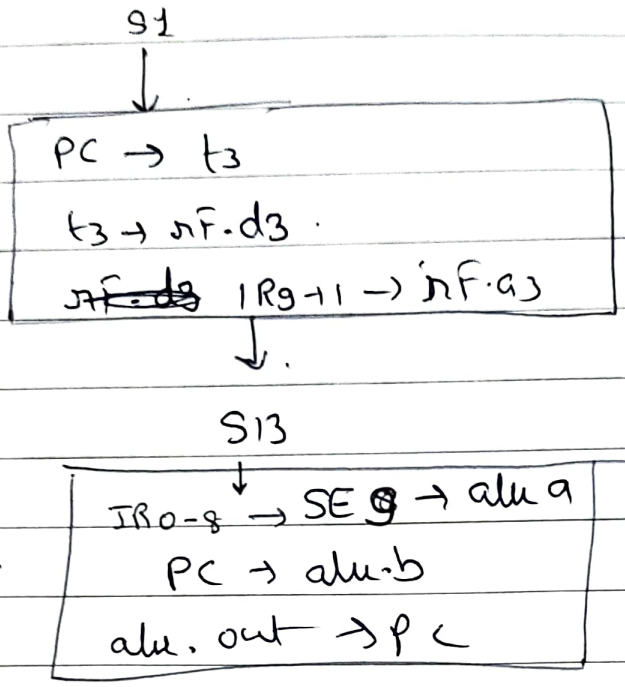
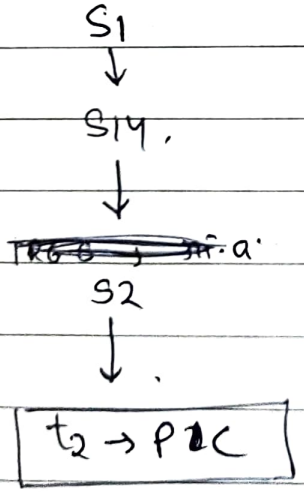
12. BEQ RA, RB, IMM.



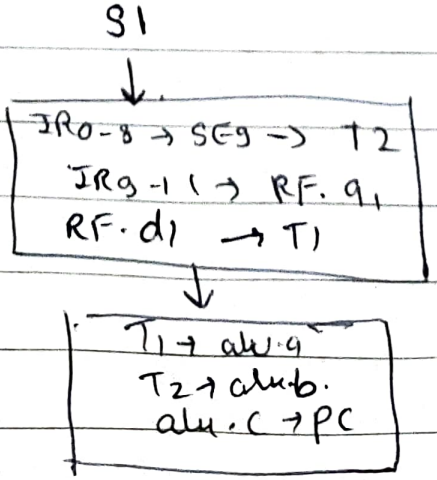
13. JALR RA IMM

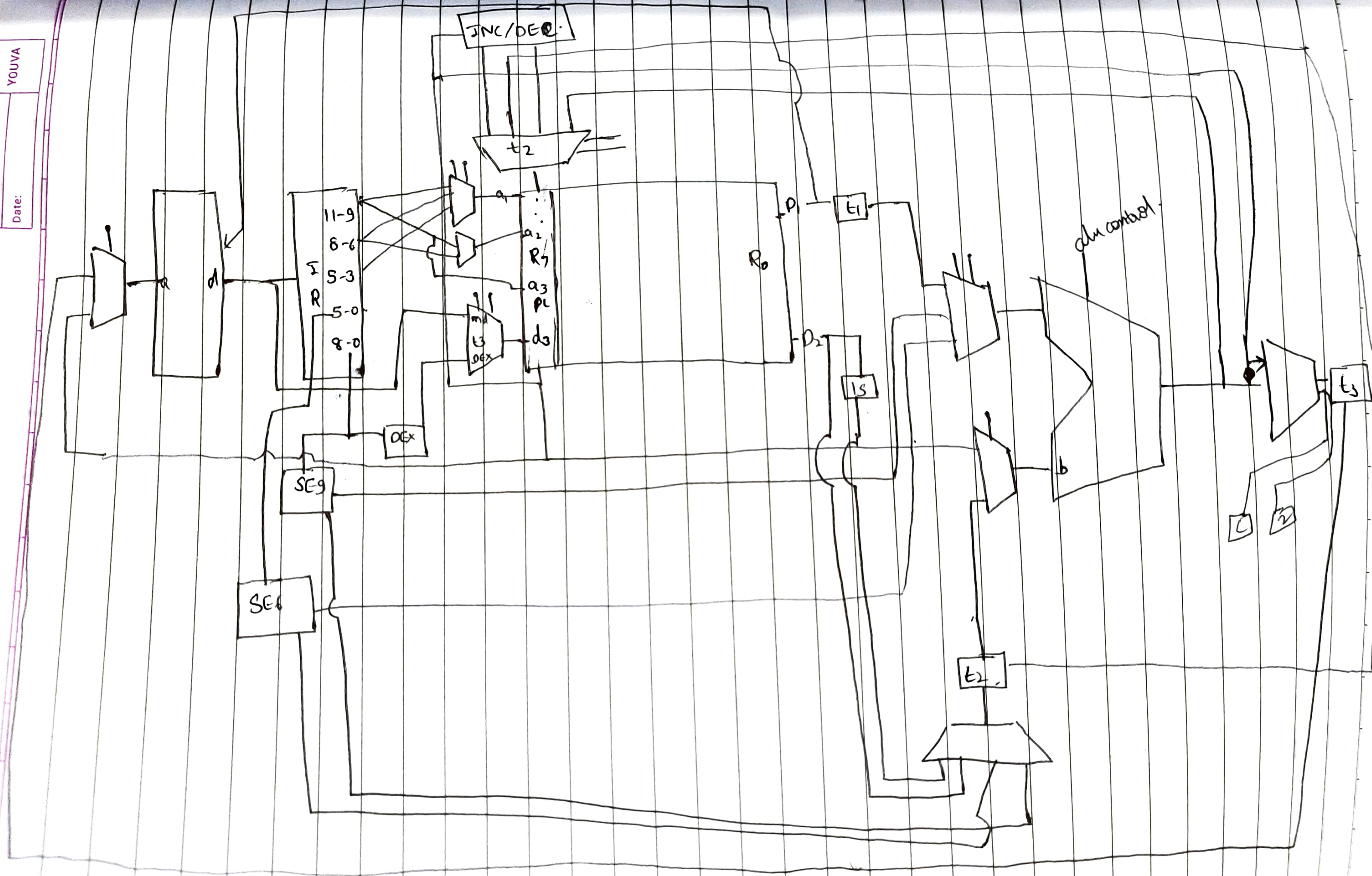

S1
PC → t3
S14
t3 → RF.d3
IRg+1 → RF.g3
S13
IR0-8 → SEG → alu.a
S15.
PC → alu.b
alu.out → PC

14. B.


S1
S14.
S2
S16.
t2 → PC

15. JRI.


S1
S17
IR0-8 → SEG → T2
IRg-1 → RF.g1
RF.d1 → T1
S18.
T1 → alu.a
T2 → alu.b.
alu.c → PC


INC/DEC
t2
a
d
I
R
11-9
8-6
5-3
5-0
8-0
a1
a2
R7
a3
PL
d3
t3
DEX
R0
D1
D2
t1
1s
alu control
b
t3
c
z
SE9
SE6
DEX
t2

Control bits:

(S1) mem_a_write = { 1 for pc(r), 0 for t3 }

pc_write = (2)
- 00 for inc
- 01 for t2
- 10 for alu_out

{ 00 for alu_out; 01 for inc; 10 for t2; 11 for dec }

pc_en = ⎍

ir_en = ⎍

(S2) a1_write = { 00 for ir 11-9; 01 for ir 8-6; 10 for ir 5-3 }

a2_write = { 0 for ir 11-9; 1 for ir 8-6 }

t2_write = { 00 for rs; 01 for d2; 10 for SE6; 11 for SE9 }

S3

(S3) alu_a_write = { 00 for t1 ; 01 for REG ; 10 for SEG }

alu_b_write = { 0 for pc ; 1 for t2 }

t3_write = { 0 for alu_out ; 1 for pc }

(S4) d3_write = { 00 for mem_d ; 01 for t3 ; 10 for DE }

Note: d3 = 00 ⇒ enable r0 ; = 001 ⇒ enable r1

rf_en = ⎍

(S5) a2_write = 1 for ir6-8

t2_write = 00 for IS

a1_write = 10 for ir3-5

(S6) ≡ S3 (only Z is modified)

(S7) t2_write = 10 for SEG

a1_write = 01 for ir8-6

(S8) d3_write = 10 for DE

Based on a3, corresponding register is enabled

rf_en = ⎍

(S9) mem_d_write = 0 for t3

d3_write = 00 for mem_d

(S10) a1_write = 00 for ir_{9-11}

~~# mem_d_en = ⎍~~

mem_a_write = 0 for t3

mem_d_en = ⎍

(S11) a1_write = 01 for ir_{8-6}

a2_write = 0 for ir_{9-11}

t2_write = 01 for d2

(S12) alu_a_write = 01 for SE6

alu_b_write = 0 for PC

pc_write = 00 for alu_out

pc_en = ⎍

(S13) pc_write = 11 for dec

pc_en = ⎍

(S14) t3_write = 1 for pc

d3_write = 01 for t3

(S15) alu_a_write = ~~01 for~~ 10 for SE9

alu_b_write = 0 for pc

pc_write = 00 for alu_out

pc_en = ⎍

(S16) pc_write = 10 for t2

pc_en = ⎍

(S17) t2_write = 11 for SE9

a1_write = 00 for ir_{9-11}

(S18) alu_a_write = 00 for t1

alu_b_write = 1 for t2

pc_write = 00 for alu_out

pc_en = ⎍