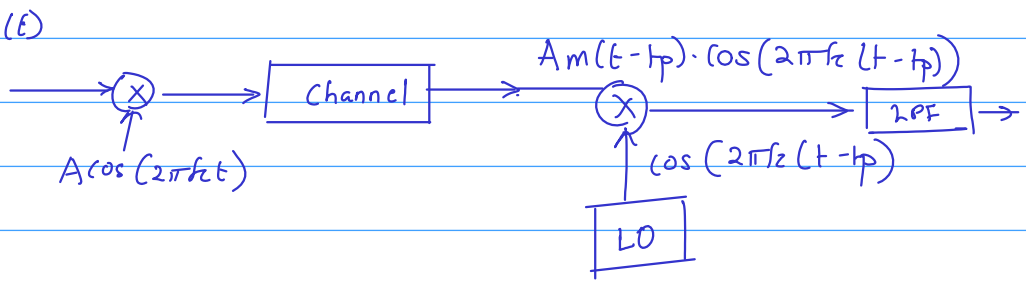
Phase locked loops.

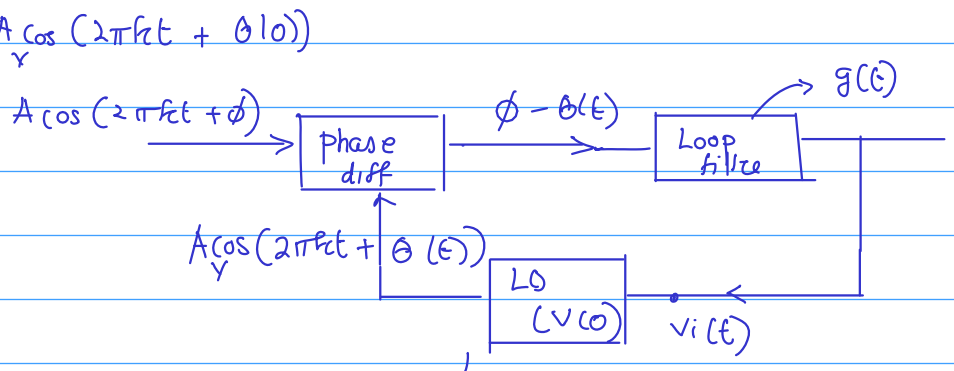
Motivation from DSBSC



how do we generate a phase matched / coherent carrier at the rx? Using a PLL.

We start with a simple case when the received signal is $A\cos(2\pi f_c t + \phi)$

LO gives $A_V \cos(2\pi f_c t + \theta(t))$



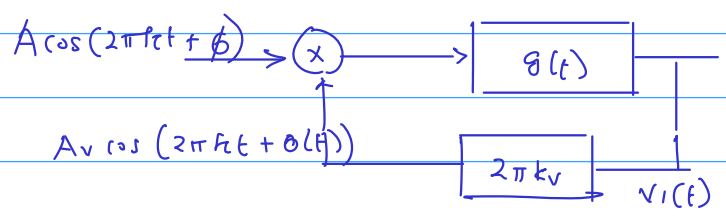
produces a sinusoidal with a freq of f_c if the input is 0.

$$\frac{d\theta(t)}{dt} = 2\pi k_v \cdot V_i(t)$$

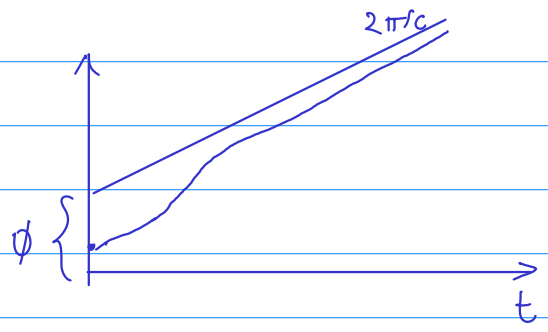
Phase diff ≡ mixer.

$$A A_v \cdot \cos(2\pi f_c t + \phi)\cdot\cos(2\pi f_c t + \theta(t))$$
$$= AA_v\left(\cos(\phi-\theta(t)) + \cos(2\pi(2f_c t) + \phi + \theta(t))\right)$$

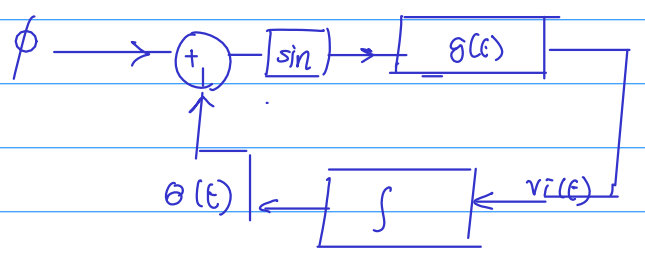
PLL



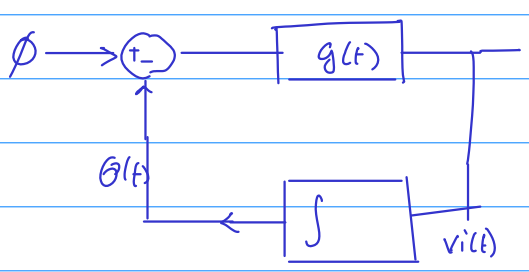
if $\theta(t) = \phi \pm \pi/2$, then PLL is in lock.



a modified model



If we assume that the PLL is already in lock



Phase offset - constant prop. delay.