Out : 11|10|2018
Not required to be submitted

AV314 - Programming Assignment | Explanation for PLL

For this programming assignment & explanation, please download PLL-Files-tar-gz from the webpage and extract the file into a folder of your choice. Please note that the simulink files were developed in Matlab 2013.

① Type I PLLs - use the files in the Type I subfolder

a) Type I PLL with a step input in phase. - use the files experiment_with_parameter_choices.m, set_parameters_Phase step.m, and pll_simulation.slx.

- In this problem, we want to design a Type I PLL for achieving phase locking to within 5% of the final value within 5ms. Using the experiment_with_parameter_choices file find out the parameters a and K, which achieves the above objective for the loop filters with $H(s) = 1$ and $H(s) = 1/s+a$; and $K = 2\pi \cdot km \cdot kv$. Here km is the gain of the mixer and kv is the sensitivity of the VCO.
- Now simulate the PLL (pll_simulation.slx) using simulink. Before you simulate the PLL, set those parameter values which you have found above in the file "set_parameters_Phase step.m".
- Check whether your design works.
- Write a Matlab function to find out the phase difference between two sinusoidal signals, of the same frequency. Use this to check whether phase locking is achieved for your system in steady state.

b) Type I PLL with a frequency step as input - use the file set_parameters_PhaseRamp_FreqStep.m.

- does the Type I PLL have zero phase error if there is a frequency step in its input?
- Find out the capture range of the PLL. How do you increase the capture range?
- In class we had used the VCO control input as a way to check whether freq. lock has been achieved for the PLL. Can you check this in a more direct way using the spectrum. Observe the spectrum of the different signals in the PLL signal loop. Try to use the plotspectrum script from an earlier lab for this.

- Suppose the VCO free running frequency is 5 KHz and the VCO is able to capture a frequency of 5050 Hz. Design the Type I PLL parameters such that the phase error that you get in steady state is $< 5°$. Verify your design with the simulation.

c) Type I PLL with frequency ramp as input - use the files set_parameters_FreqRamp.m and pll_simulation_chirpinput.slx for this.

- We note that for Type I PLLs, if the input is a frequency ramp, then the steady state error in phase grows w/o bound and the steady state error in frequency is a constant.
- Find out the lock range of the PLL. How do you increase the lock range?
- Design the PLL parameters such that the steady state error in frequency is less than 10 Hz. Check whether your design is correct using the simulation.

(2) FM and FSK demodulation. - use files in the FM-Demodulation subfolder. For this demonstration, you should use the generate_fm/fsk_signal.m file, followed by the fm/fsk_demodulation file followed by the simulink simulation

- Change the rate at which bits are transmitted in the FSK generation code. and check whether the FM demodulation (fm_pll_demodulation.slx) is able to extract a square wave corresponding to the bits
- Increase the frequency deviation of the FSK signal and see whether the FM demodulation is able to recover the square wave corresponding to the bits
- Similarly, try freq modulation of other signals (in generate_fm_signal.m) and observe how the PLL demodulates these signals.