METRO STATE UNIVERSITY

ICS 232 Computer Organization & Architecture
Homework 13 - Chapter 9 - 10 points
Due Date: 11/29/2023

Name: Key

Note: Please post your homework to ICS232 D2L on or before the due date.

Chapter 9 – Alternative Architectures

Essential Terms and Concepts

3. Describe how register windowing makes procedure call more efficient?

Storing parameters in registers is much faster than storing them in the stack. Therefore, the speed of procedures call can be improved.

7. Do all programming problems lend themselves to parallel execution? What is the limiting factor?

No. Many times serial execution is required to merge data from parallel tasks.

12. Explain the limitation inherent in a register-register vector processing machine?

The number of registers limits the number of elements that can be processed at one time.

13. Give two reasons for the efficiency of vector processors.

Fewer instructions are executed and there is a continuous source of data so pre-fetching can occur.

21. What is reentrant code?

The same code can be executed at the same time by multiple threads.

Exercises

METRO STATE UNIVERSITY

ICS 232 Computer Organization & Architecture
Homework 13 - Chapter 9 - 10 points
Due Date: 11/29/2023

1. Why do RISC machines operate on registers?

RISC machines limit the instructions that can access memory to load and store instructions only. This means that all other instructions use registers. This requires fewer cycles and speeds up the execution of the code and, thus, the performance of the hardware. The goal for RISC architectures is to achieve single-cycle instructions, which would not be possible if instructions had to access memory instead of registers.

4. Suppose a RISC machine uses overlapping register windows with:
   - 10 global registers
   - 6 input parameter registers
   - 10 local registers
   - 6 output parameter registers

How large is each overlapping register window?

6

6. A RISC processor has 152 total registers, with 12 designated as global registers. The 10 register windows each have 6 input registers and 6 output registers. How many local registers are in each register window set? HINT: Remember, due to the circular nature of the windows, the output registers of the last window are shared as the input registers of the first window.

152 = 12 + 10 x (local + 6)

local = 8

9. Recall our discussions from Chapter 8 regarding context switches. These occur when one process stops using the CPU and another process begins. In this sense, register windows could be viewed as a potential weakness of RISC. Explain why this is the case.

During a context switch, all information about the currently executing process must be saved, including the values in the register windows. When the process is restored, the values in the register windows must be restored as well. Depending on the size of the

METRO STATE UNIVERSITY

ICS 232 Computer Organization & Architecture
Homework 13 - Chapter 9 - 10 points
Due Date: 11/29/2023

windows, this could be a very time-consuming process.

13. Explain the difference between loosely coupled and tightly coupled architectures.

Loosely coupled and tightly coupled are terms that describe how multiprocessors deal with memory. If there is one large, centralized, shared memory, we say the system is tightly coupled. If there are multiple, physically distributed memories, we say the system is loosely coupled.

21. Why are distributed systems desirable?

Distributed systems allow for resource sharing (such as sharing of printers and files), and thus, can reduce system cost. They also allow for redundancy, which increases reliability (if one site fails, the remaining sites can still function). These systems also speed up computation, as jobs can be distributed and run concurrently at many sites. Lastly, distributed systems run programs that, due to the nature of the system, can share data with other systems more easily via the communications network and communicate with remote sites.

28. Compare and contrast supervised learning and unsupervised learning with regard to neural networks.

Supervised learning assumes that for each input, the output is known a priori. In unsupervised learning, no outputs are known in advance.

33. Indicate whether each of the following applies to CISC or RISC by placing either a C (for CISC) or an R (for RISC) in the blank.

__R__ 1. Simple instructions averaging 1 clock cycle to execute
__C__ 2. Single register set
__R__ 3. Complexity is in the compiler
__R__ 4. Highly pipelined
__C__ 5. Any instruction can reference memory
__C__ 6. Instructions are interpreted by the microprogram

METRO STATE UNIVERSITY

ICS 232 Computer Organization & Architecture
Homework 13 - Chapter 9 - 10 points
Due Date: 11/29/2023

__R__ 7. Fixed length, easily decoded instruction format
__C__ 8. Highly specialized, infrequently used instructions
__R__ 9. Use of overlapping register windows
__R__ 10. Relatively few addressing modes

Prepare for Final Exam

Complete Project 2

Continue working on Your Group Project

Continue working on Homework 14 (Bonus)

Optional Questions:

1. What were your favorite and least favorite parts of the course?

2. In what ways could the course be improved?

3. How many hours a week did you spend outside of class? Do you think this is too much or too little?