



## EXAMINATIONS — 2014

TRIMESTER 2

**NWEN 242  
COMPUTER ORGANISATION**

Time Allowed: THREE Hours (180 minutes)

Instructions: Answer all questions.

Use the booklet provided to answer questions. Do not write any answer directly in this examination paper.

Make sure your answers are clear and to the point.

Non-programmable calculators or silent programmable calculators with their memories cleared are permitted in this examination.

Paper foreign to English language dictionaries are allowed.

No other reference materials are allowed.

There are **100** possible marks on the exam.

Topic	Marks
1 Basic Concepts	21 marks
2 MIPS Assembly Language	20 marks
3 Combinational and Sequential Logic	10 marks
4 Pipelined Data Path	15 marks
5 Memory Technology	17 marks
6 Performance	11 marks
7 IO Basics	6 marks

**Note:** Marks are shown for each question as a whole and also for their parts.

## Question 1. Basic Concepts

[21 marks]

- a) [3 marks] What are the three different classes of applications where computers are used?
- b) [1 marks] What are the steps involved in transforming a program written in a high-level language into a representation that is directly executed by a computer processor?
- c) [4 marks] List at least four different MIPS addressing modes?
- d) [1 marks] What is an instruction set architecture?
- e) The individual stages of a datapath have the following latencies:

IF	ID	EX	MEM	WB
250ps	300ps	150ps	300ps	200ps

  - i) [2 marks] What is the clock cycle time in a pipelined multi-cycle and non-pipelined single-cycle processor?
  - ii) [2 marks] Compare the performance of the single-cycle organizations against that of the pipelined organization.
- f) [3 marks] In the context of a pipelined datapath, what are structural, data and control hazards?
- g) [2 marks] Explain the purposes of L1 and L2 caches in multilevel caches.
- h) [2 marks] What is a page and a page fault in a virtual memory system?
- i) [1 marks] In a page table, for a given entry, if the valid bit is set to “0”, what does this mean?

## Question 2. MIPS Assembly Language

[20 marks]

- a) [8 marks] Consider a C assignment statement below.

$f = A[B[g]-1];$

Assume that A and B are two arrays of words (each word comprises of 32 bits). Also assume that the base address of the arrays A and B are in registers \$s6 and \$s7, respectively.

Find the corresponding MIPS assembly code for the statement.

- b) [2 marks] Write the MIPS assembly code that creates the 32-bit constant 0010 0000 0000 0001 0100 1001 0010 0100<sub>two</sub> and stores that value to register \$t1.

- c) [2 marks] Assume the following register contents:

$\$t0=0xAAAAAAA$

What would be the value of \$t2 after executing the following sequence of instructions?

```
sll $t2, $t0, 4  
andi $t2, $t2, -1
```

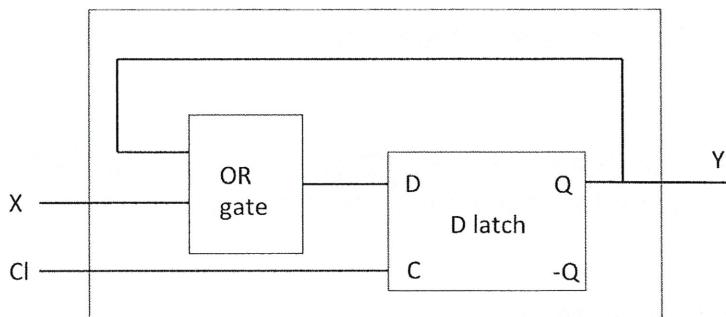
- d) [8 marks] Convert the C function below to a MIPS assembly program.

```
int f(int a, int b) {  
    if (a == 0) return 0;  
    else return f(a-1,b-1);  
}
```

### Question 3. Combinational and Sequential Logic

[10 marks]

- a) [4 marks] One logic function that is used for a variety of purposes is **exclusive OR** (XOR). The output of a two-input exclusive OR function is true only if exactly one of the inputs is true. **Show the truth table** for a two-input exclusive OR function and **implement this function** using AND gates, OR gates, and inverters.
- b) [4 marks] Give the transition table that shows the input-output relationship for the following logic block. The inputs are X and Cl, and the output is Y.



- c) [2 marks] Assume that X consists of 3 bits,  $x_2 \ x_1 \ x_0$ . Write a logic function that is true if and only if X contains only one 0.

## Question 4. Pipelined Datapath

[15 marks]

- a) Consider the following sequence of instructions.

40: lw \$t4, 2(\$t1)  
44: beq \$t4, \$t1, 9

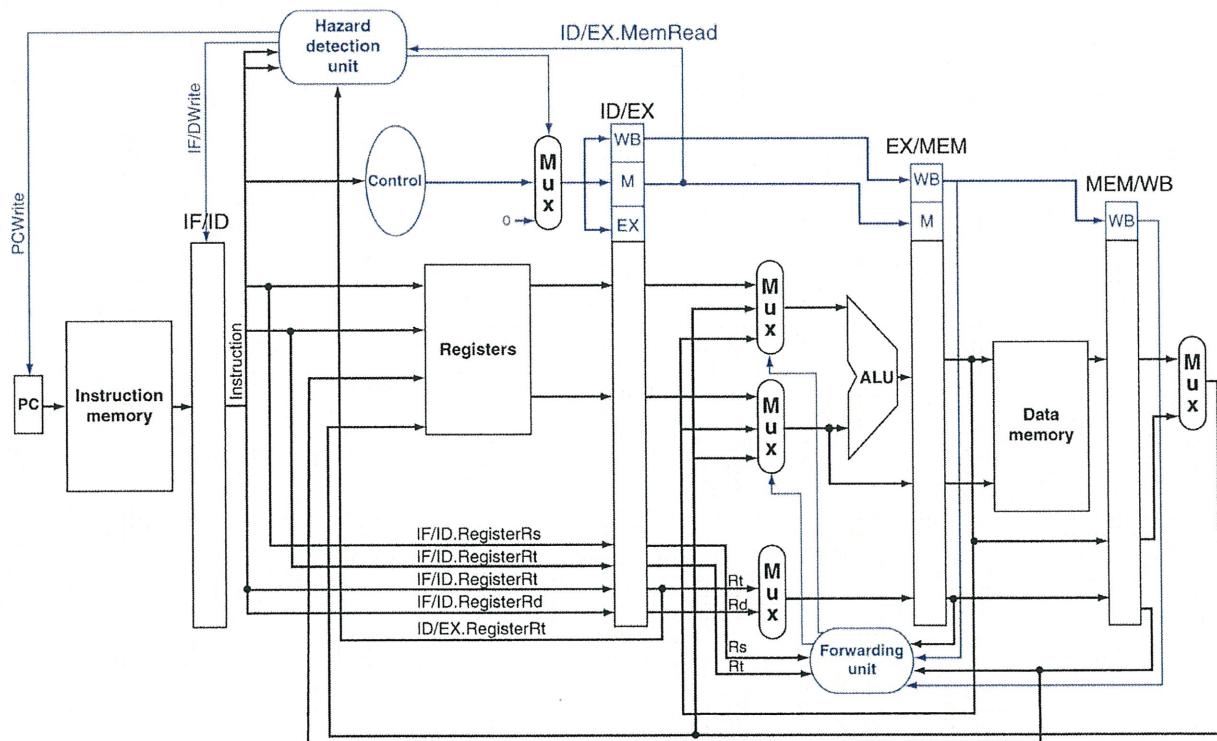
...

xx: sw \$t4, 6(\$t4)

i) [2 marks] Assuming that the store instruction (sw) is the target if the branch is taken, what should xx be?

ii) [3 marks] Assuming that the pipeline has full forwarding support, and has the extra hardware to move the branch decision to the ID stage, insert nops to the above instruction sequence to ensure correct execution.

- b) [2 marks] The following figure presents an overview of pipelined datapath. Explain the functionalities of the Forwarding Unit and Hazard Detection Unit.



- c) Consider the following sequence of instructions, with the full support of Forwarding Unit and Hazard Detection Unit (see the figure in b).

lw \$t1, 4(\$t0)  
lw \$t2, 8(\$t0)  
add \$t3, \$t1, \$t2  
sw \$t3, 20(\$t2)

i) **[6 marks]** Give the conditions for detecting the hazards in the sequence. In the conditions, you need to specify the register number, using the register number provided in the instructions instead of RegisterRs/Rt/Rd. Choose appropriate control signals from: RegDst, RegWrite, MemRead and MemWrite.

ii) **[2 marks]** At a given cycle, the first load instruction (i.e. `lw $t1, 4($t0)`) in the above instruction sequence is at the MEM stage. For each of the instructions, list the stage for the current cycle and the next cycle.

## Question 5. Memory Technology

[17 marks]

- a) Assume a system that has a processor with a base CPI of 1.0, and the main memory access time is 100 cycles.
- i) [2 marks] Assume that the system has only one level of cache, and the cache has a miss rate of **4%**. What is the effective CPI of the system?
- ii) [2 marks] The cache designer decided to add another level of cache, making it a two-level cache. The new system managed to reduce the miss rate to main memory to **1%**. Assume the L1 cache has a miss rate of **4%**. If the effective CPI of the new system is 3, what would the L2 cache access time be?
- b) Consider a 4-way set associative cache with 1024 blocks and a block size of 16 bytes.
- i) [3 marks] Identify the number of Tag bits, Index bits and Offset bits. Show your working.
- ii) [3 marks] What are the values of the Tag, Index and Offset fields for byte address 1221 (use decimal notation for the values)? Show your working.
- c) In a virtual memory system, the page size is 8KiB. Assume that a virtual address is 32 bits.
- i) [2 marks] Identify the Offset field in the virtual address (number of bits and their positions)
- ii) [2 marks] Explain how many entries the page table has (you may use power of 2 notation).
- d) [3 marks] Explain how a TLB miss is detected and how to identify that a miss is merely a TLB miss or a page fault.

## Question 6. Performance

[11 marks]

- a) [2 marks] In the computer industry, “*millions instructions per second*” (i.e. MIPS) is a measurement of program execution speed based on the number of millions of instructions. Identify two potential difficulties of using MIPS in comparing the performance of computer systems in practice.
- b) [3 marks] Identify at least three possible methods that may help to reduce the power consumption of a processor.
- c) Compilers can have a profound impact on performance of a computer application. Assume that for a program, compiler A results in a dynamic instruction count of  $1.0E9$  and has an execution time of 1.1s, while compiler B results in a dynamic instruction count of  $1.2E9$  and an execution time of 1.5s.
  - (i) [3 marks] Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.
  - (ii) [3 marks] A new compiler is developed that uses only  $6.0E8$  instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A on a processor with a clock cycle time of 1 ns?

## **Question 7. IO Basics**

**[6 marks]**

- a) **[2 marks]** What would be the most appropriate bus type (synchronous or asynchronous) for handling communications between a CPU and a printer? Justify your answer.
  
- b) **[2 marks]** Describe interrupt-driven I/O. Explain the disadvantage of polling in comparison with interrupt driven I/O.
  
- c) **[2 marks]** Does the CPU relinquish control of memory when DMA is active? For example, can a peripheral simply communicate with memory directly, avoiding the CPU completely?

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