TE WHARE WĀNANGA O TE ŪPOKO O TE IKA A MĀUI

VICTORIA
UNIVERSITY OF WELLINGTON

EXAMINATIONS – 2015

TRIMESTER 2

NWEN242

COMPUTER ORGANISATION

Time allowed: TWO HOURS

CLOSED BOOK

Permitted materials: Only silent non-programmable calculators or silent programmable calculators with their memories cleared are permitted in this examination.

Paper foreign to English language dictionaries are allowed.

Instructions: This exam consists of 100 marks in total. There are FIVE questions to be answered. They are

Question 1: Basic Concepts
Question 2: MIPS Assembly Language
Question 3: Combinational and Sequential Logic
Question 4: Pipelined Datapath
Question 5: Memory Technology

You need to answer all questions.

Remember to show working.

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Question 1: Basic Concepts [33 MARKS]

a) List the four design principles for the MIPS instruction set architecture.

(4 Marks)

b) Describe the difference between volatile and non-volatile memories.

(2 Marks)

c) If the current value of the PC (program counter) is 0x00100000, can you use a single branch instruction to get to branch target at address 0x00000000? Make sure that you explain your answer.

(3 Marks)

d) The individual stages of a datapath have the following latencies:

IF	ID	EX	MEM	WB
200ps	300ps	150ps	350ps	200ps

(i) Briefly explain the functionality of the FIVE stages.

(5 Marks)

(ii) What is the clock cycle time in a pipelined multi-cycle, non-pipelined multi-cycle and single-cycle processor?

(3 Marks)

(iii) Assume that there are *N* instructions to execute and no hazards present in the pipeline. State how many cycles it takes to execute the *N* instructions for the single-cycle organization and the pipelined organization, respectively.

(2 Marks)

e) Explain the types of locality in the context of memory and cache design.

(3 Marks)

f) Briefly explain the difference between direct-mapped cache and set-associative cache?

(2 Marks)

g) State the concept of virtual memory?

(2 Marks)

h) State the difference between a TLB miss and a page fault.

(2 Marks)

i) What is an asynchronous I/O bus?

(2 Marks)

j) Consider a computer running a program that requires 250 seconds, with 70 seconds spent executing FP (i.e. floating point) instructions; 85 seconds spent executing L/S (i.e. load and store) instructions; 40 seconds spent executing branch instructions; and 55 seconds spent executing other instructions. Can the total execution time be reduced by 20% by reducing only the time for executing branch instructions? Make sure that you explain your answer.

(3 Marks)

Question 2: MIPS Assembly Language [25 MARKS]

a) Implement the C assignment expression below in MIPS.

```
B[6]=A[i*2];
```

Assume that the base address of array B is in $s1 and the base address of array A is in $s2. The index variable i is allocated to $s3.

(5 Marks)

b) Given the do-while loop in C below, implement this loop in MIPS.

```
do{
   --i;
} while (i > 10);
```

Assume that variable i is allocated to $s1.

(8 Marks)

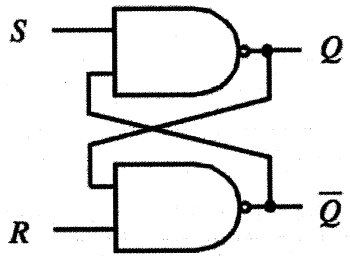
c) Implement the C function below in MIPS.

```
int f(int a)
{
   a++;
   if(a < 10) return f(a);
   else return a;
}
```

(12 Marks)

Question 3: Combinational and Sequential Logic [12 Marks]

a) Below please find the design of a SR latch by using NAND (i.e. Not AND) gates.



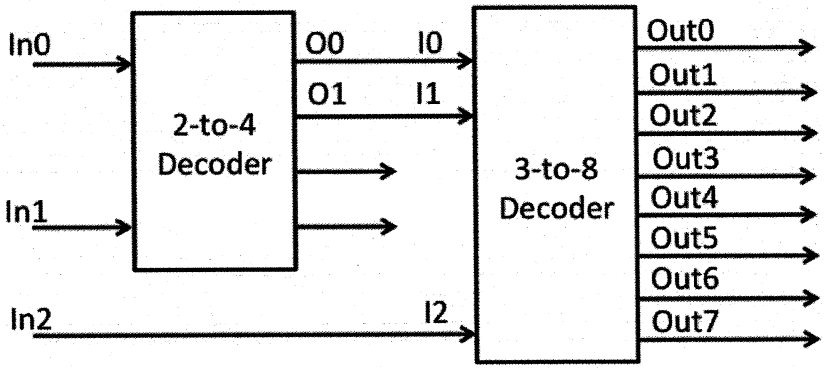
(i) Present a truth table for an NAND gate. Assume that the inputs to the NAND gate are A and B. The NAND gate produces an output denoted as C.

(4 Marks)

(ii) Present the state transition table for the SR latch design that uses NAND gates. Please also indicate in the state transition table which inputs should be considered as illegal.

(5 Marks)

b) Based on the following logic block, identify all possible inputs (for In0, In1, and In2) in order for out4 to be asserted. Make sure that you explain your answer.



(3 Marks)

Question 4: Pipelined Datapath [15 MARKS]

Consider the following sequence of instructions.

```
08:  lw   $t1, 8($t1)
12:  add  $t1, $t1, $t2
16:  beq  $t4, $t1, 10
...
xx:  sw   $t4, 4($t4)
```

a) Assuming that the `store` instruction is the target if the branch is taken, what xx should be?

(2 Marks)

b) Assuming that the pipeline has no forwarding support, and branches execute in the EX stage, insert nops to ensure correct execution

(3 Marks)

c) Assuming that the pipeline has full forwarding support, and has the extra hardware to move the branch decision to the ID stage, insert nops to ensure correct execution.

(3 Marks)

d) Assume that the pipeline has full forwarding support, and has the extra hardware to move the branch decision to the ID stage. Also assume that the **`load`** instruction is currently in the MEM stage. List the stage for each of the instructions for the current cycle, the next cycle, and the cycle after next cycle (ignore the instructions if they are not in the pipeline).

(3 Marks)

e) Assume that the pipeline has full forwarding and hazard detection support. Give the conditions for detecting the hazards associated with the **`load`** instruction (you need to specify the register number and whether it is Rs/Rt/Rd, e.g., $t3/Rs). Choose the appropriate control signals from: RegDst, RegWrite, MemRead and MemWrite.

(4 Marks)

Question 5: Memory Technology [15 MARKS]

a) For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-8	7-4	3-0

(i) What is the cache block size in words?

(2 Marks)

(ii) How many entries does the cache have?

(2 Marks)

b) In a two-level cache system where the L1 cache access time is **1** cycle, the L2 cache access time is **10** cycles, and the main memory access time is **100** cycles. Assume that the L1 cache has a miss rate of **8%** and the L2 cache has a miss rate of **80%**. Determine the effective CPI of the system.

(3 Marks)

c) Considering a 4-way set associative cache, with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-12	11-5	4-0

(i) Determine the usable size of the cache in words.

(3 Marks)

(ii) What are the values of the Tag, Index and Offset fields for byte address 1030 (use decimal notation for the values)? Show your working.

(3 Marks)

d) In a virtual memory system, assuming no misses, briefly explain how a data item is read.

(2 Marks)

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