This document will be updated as the computer is developed

TITLE:	DATE:
8 Bits Computer	25/04/2021
Block Diagram	PAGE:
BY: Tec. Vinicius Moraes REV: @REV	1/19

U1:A NE556
- +5V — 14 VCC
- 4 R
- 5 Q → CLOCK_AUTO
- 1 DC
- R2 10R
- RV1 100K 20%
- 3 CV
- 6 TR
- 2 TH
- 7 GND
- R1 150R
- C1 10nF
- C2 10uF

U1:B NE556
- +5V — 14 VCC
- 10 R
- 9 Q → CLOCK_MANUAL
- 13 DC
- R3 10k
- 11 CV
- 8 TR
- 12 TH
- 7 GND
- R4 330K
- C4 10nF
- C3 330nF

CLOCK ▷ — D1 LED-GREEN — R5 470R

U3:A 74HC00 — CLOCK_AUTO (1, 2 → 3)
U3:B 74HC00 (4, 5 → 6)
U3:D 74HC00 (13, 12 → 11)
U2:A 74HC04 (1 → 2) → CLOCK, CLOCK̄
U?:A 74HC04 — SELECT (1 → 2)
U3:C 74HC00 (10, 9 → 8)

HLT ▷

SW1 SW-SPDT
U49:E 74HC04 (11 → 10)
U49:F 74HC04 (9 → 8) → SELECT
R6 470R — D2 LED-RED
D3 LED-BLUE — R7 470R
+5V

HLT ○ — +5V

C5 100nF, C6 100nF, C7 100nF (+5V)

TITLE:	DATE:
8 Bits Computer	25/04/2021
Control - Oscillator	PAGE:
BY: Tec. Vinicius Moraes REV: @REV	2/19

U4
74HC161

	Pin			Pin	
BUS_0	3	D0	Q0	14	PC_B7
BUS_1	4	D1	Q1	13	PC_B6
BUS_2	5	D2	Q2	12	PC_B5
BUS_3	6	D3	Q3	11	PC_B4
			RCO	15	
PC_INC	7	ENP			
	10	ENT			
CLOCK	2	CLK			
JMP	9	LOAD			
RESET	1	MR			

U8
74HC245

	Pin			Pin	
	2	A0	B0	18	BUS_7
	3	A1	B1	17	BUS_6
	4	A2	B2	16	BUS_5
	5	A3	B3	15	BUS_4
	6	A4	B4	14	BUS_3
	7	A5	B5	13	BUS_2
	8	A6	B6	12	BUS_1
	9	A7	B7	11	BUS_0
PC_OUT	19	CE			
	1	AB/BA			

+5V

U5
74HC161

	Pin			Pin	
BUS_4	3	D0	Q0	14	PC_B3
BUS_5	4	D1	Q1	13	PC_B2
BUS_6	5	D2	Q2	12	PC_B1
BUS_7	6	D3	Q3	11	PC_B0
			RCO	15	
	7	ENP			
	10	ENT			
CLOCK	2	CLK			
JMP	9	LOAD			
RESET	1	MR			

PC_B0
PC_B1
PC_B2
PC_B3
PC_B4
PC_B5
PC_B6
PC_B7

D4 D5 D6 D7 D8 D9 D10 D11

R8	R9	R10	R11	R12	R13	R14	R15
470R	470R	470R	470R	470R	470R	470R	470R

+5V +5V +5V

C8	C9	C10
100nF	100nF	100nF

TITLE:
8 Bits Computer
Program Counter

DATE:
25/04/2021

PAGE:
3/19

BY: Tec. Vinicius Moraes   REV: @REV

U6
74HC173

Pin	Label		Pin	Label

- BUS_7 — 14 — D0
- BUS_6 — 13 — D1
- BUS_5 — 12 — D2
- BUS_4 — 11 — D3
- Q0 — 3 — ACC_B7
- Q1 — 4 — ACC_B6
- Q2 — 5 — ACC_B5
- Q3 — 6 — ACC_B4
- CLOCK — 7 — CLK
- 1 — $\overline{OE1}$
- 2 — $\overline{OE2}$
- $\overline{ACC\_IN}$ — 9 — E1
- 10 — E2
- RESET — 15 — MR

U7
74HC173

- BUS_3 — 14 — D0
- BUS_2 — 13 — D1
- BUS_1 — 12 — D2
- BUS_0 — 11 — D3
- Q0 — 3 — ACC_B3
- Q1 — 4 — ACC_B2
- Q2 — 5 — ACC_B1
- Q3 — 6 — ACC_B0
- CLOCK — 7 — CLK
- 1 — $\overline{OE1}$
- 2 — $\overline{OE2}$
- $\overline{ACC\_IN}$ — 9 — E1
- 10 — E2
- RESET — 15 — MR

U9
74HC245

+5V

- 2 — A0 — B0 — 18 — BUS_7
- 3 — A1 — B1 — 17 — BUS_6
- 4 — A2 — B2 — 16 — BUS_5
- 5 — A3 — B3 — 15 — BUS_4
- 6 — A4 — B4 — 14 — BUS_3
- 7 — A5 — B5 — 13 — BUS_2
- 8 — A6 — B6 — 12 — BUS_1
- 9 — A7 — B7 — 11 — BUS_0
- 19 — $\overline{CE}$
- 1 — AB/$\overline{BA}$

$\overline{ACC\_OUT}$

ACC_B0
ACC_B1
ACC_B2
ACC_B3
ACC_B4
ACC_B5
ACC_B6
ACC_B7

D12 D13 D14 D15 D16 D17 D18 D19

R16 470R	R17 470R	R18 470R	R19 470R	R20 470R	R21 470R	R22 470R	R23 470R

+5V +5V +5V

C11 100nF   C12 100nF   C13 100nF

U13 74HC173

Pin	Signal		Pin	Signal
14	D0		3	Q0 IR_B7
13	D1		4	Q1 IR_B6
12	D2		5	Q2 IR_B5
11	D3		6	Q3 IR_B4

BUS_7, BUS_6, BUS_5, BUS_4

CLOCK 7 CLK
1 OE1
2 OE2
IR_IN 9 E1
10 E2
RESET 15 MR

U14 74HC173

BUS_3, BUS_2, BUS_1, BUS_0

Pin	Signal		Pin	Signal
14	D0		3	Q0 IR_B3
13	D1		4	Q1 IR_B2
12	D2		5	Q2 IR_B1
11	D3		6	Q3 IR_B0

CLOCK 7 CLK
1 OE1
2 OE2
IR_IN 9 E1
10 E2
RESET 15 MR

+5V

U15 74HC245

Pin	A	B	Pin	Bus
2	A0	B0	18	BUS_7
3	A1	B1	17	BUS_6
4	A2	B2	16	BUS_5
5	A3	B3	15	BUS_4
6	A4	B4	14	BUS_3
7	A5	B5	13	BUS_2
8	A6	B6	12	BUS_1
9	A7	B7	11	BUS_0

19 CE
1 AB/BA

IR_OUT

IR_B0
IR_B1
IR_B2
IR_B3
IR_B4
IR_B5
IR_B6
IR_B7

D28 D29 D30 D31 D32 D33 D34 D35

R32 470R, R33 470R, R34 470R, R35 470R, R36 470R, R37 470R, R38 470R, R39 470R

+5V +5V +5V

C17 100nF C18 100nF C19 100nF

U16 — 74HC283

Pin	Signal		Pin	Signal
5	A0	ACC_B4	4	S0 — SUM_B4
3	A1	ACC_B5	1	S1 — SUM_B5
14	A2	ACC_B6	13	S2 — SUM_B6
12	A3	ACC_B7	10	S3 — SUM_B7
6	B0	B_REG_B4		
2	B1	B_REG_B5		
15	B2	B_REG_B6		
11	B3	B_REG_B7		
7	C0		9	C4

U17 — 74HC283

Pin	Signal		Pin	Signal
5	A0	ACC_B0	4	S0 — SUM_B0
3	A1	ACC_B1	1	S1 — SUM_B1
14	A2	ACC_B2	13	S2 — SUM_B2
12	A3	ACC_B3	10	S3 — SUM_B3
6	B0	B_REG_B0		
2	B1	B_REG_B1		
15	B2	B_REG_B2		
11	B3	B_REG_B3		
7	C0	$\overline{ADD}$	SUB	9	C4

U18:A 74HC86 — B_B4 (1), $\overline{ADD}$ | SUB (2), 3 — B_REG_B4
U18:B 74HC86 — B_B5 (4), (5), 6 — B_REG_B5
U18:C 74HC86 — B_B6 (9), (10), 8 — B_REG_B6
U18:D 74HC86 — B_B7 (12), (13), 11 — B_REG_B7

U19:A 74HC86 — B_B3 (1), $\overline{ADD}$ | SUB (2), 3 — B_REG_B0
U19:B 74HC86 — B_B2 (4), (5), 6 — B_REG_B1
U19:C 74HC86 — B_B1 (9), (10), 8 — B_REG_B2
U19:D 74HC86 — B_B0 (12), (13), 11 — B_REG_B3

+5V C23 100nF
+5V C20 100nF
+5V C21 100nF
+5V C22 100nF

TITLE:	DATE:
8 Bits Computer	25/04/2021
ALU - Arithmetic Unity	PAGE:
BY: Tec. Vinicius Moraes REV: @REV	7/19

ALU - Logic Unity schematic (page 8/19).

Gate groups:

U20:A (74HC08) — ACC_B0 (1), B_B0 (2) → AND_B0 (3)
U20:B (74HC08) — ACC_B1 (4), B_B1 (5) → AND_B1 (6)
U20:C (74HC08) — ACC_B2 (9), B_B2 (10) → AND_B2 (8)
U20:D (74HC08) — ACC_B3 (12), B_B3 (13) → AND_B3 (11)
U21:A (74HC08) — ACC_B4 (1), B_B4 (2) → AND_B4 (3)
U21:B (74HC08) — ACC_B5 (4), B_B5 (5) → AND_B5 (6)
U21:C (74HC08) — ACC_B6 (9), B_B6 (10) → AND_B6 (8)
U21:D (74HC08) — ACC_B7 (12), B_B7 (13) → AND_B7 (11)

U22:A (74HC32) — ACC_B0 (1), B_B0 (2) → OR_B0 (3)
U22:B (74HC32) — ACC_B1 (4), B_B1 (5) → OR_B1 (6)
U22:C (74HC32) — ACC_B2 (9), B_B2 (10) → OR_B2 (8)
U22:D (74HC32) — ACC_B3 (12), B_B3 (13) → OR_B3 (11)
U23:A (74HC32) — ACC_B4 (1), B_B4 (2) → OR_B4 (3)
U23:B (74HC32) — ACC_B5 (4), B_B5 (5) → OR_B5 (6)
U23:C (74HC32) — ACC_B6 (9), B_B6 (10) → OR_B6 (8)
U23:D (74HC32) — ACC_B7 (12), B_B7 (13) → OR_B7 (11)

$\overline{\text{XOR | NOT}}$

U25:A (74HC32) — U24:A (74HC86) → XOR_NOT_B0 (3), ACC_B0 (1)
U26:A (74HC32) — U24:B (74HC86) → XOR_NOT_B1 (6)
U25:B (74HC32) — U24:C (74HC86) → XOR_NOT_B2 (8)
U25:C (74HC32) — U24:D (74HC86) → XOR_NOT_B3 (11)
U28:A (74HC32) — U27:A (74HC86) → XOR_NOT_B4 (3)
U28:B (74HC32) — U27:B (74HC86) → XOR_NOT_B5 (6)
U28:C (74HC32) — U27:C (74HC86) → XOR_NOT_B6 (8)
U28:D (74HC32) — U27:D (74HC86) → XOR_NOT_B7 (11)

Decoupling capacitors (all 100nF, +5V):
C31, C28, C29, C30, C27, C24, C25, C26

TITLE: 8 Bits Computer — ALU - Logic Unity
DATE: 25/04/2021
PAGE: 8/19
BY: Tec. Vinicius Moraes
REV: @REV

SUM_B0 2
U55:A 1
74HC02

SUM_B1 3

SUM_B2 5
U55:B 4
74HC02

SUM_B3 6

U56:A 3
74HC08
1
2

SUM_B4 8
U55:C 10
74HC02

SUM_B5 9

SUM_B6 11
U55:D 13
74HC02

SUM_B7 12

U56:B 6
74HC08
4
5

U56:C 8 STATUS_ZF
74HC08
9
10

SUM_OUT 2
U57:A 1
74HC02

ADD | SUB 3

U29

Pin	Signal		Signal	Pin
6	SUM_B0 — 1X0	1Y	— ALU_B0	7
5	AND_B0 — 1X1			
4	OR_B0 — 1X2			
3	XOR_NOT_B0 — 1X3			
10	SUM_B1 — 2X0	2Y	— ALU_B1	9
11	AND_B1 — 2X1			
12	OR_B1 — 2X2			
13	XOR_NOT_B1 — 2X3			
14	ALU_0 — A			
2	ALU_1 — B			
1	1E			
15	2E			

74HC153

U32

Pin	Signal		Signal	Pin
6	SUM_B4 — 1X0	1Y	— ALU_B4	7
5	AND_B4 — 1X1			
4	OR_B4 — 1X2			
3	XOR_NOT_B4 — 1X3			
10	SUM_B5 — 2X0	2Y	— ALU_B5	9
11	AND_B5 — 2X1			
12	OR_B5 — 2X2			
13	XOR_NOT_B5 — 2X3			
14	ALU_0 — A			
2	ALU_1 — B			
1	1E			
15	2E			

74HC153

U58

Pin	Signal		Signal	Pin
14	STATUS_ZF — D0	Q0	— ZF	3
13	STATUS_CF — D1	Q1	— CF	4
12	D2	Q2		5
11	D3	Q3		6
7	CLOCK — CLK			
1	$\overline{OE1}$			
2	$\overline{OE2}$			
9	$\overline{ST\_IN}$ — E1			
10	E2			
15	RESET — MR			

74HC173

+5V

U30

Pin	Signal		Signal	Pin
6	SUM_B2 — 1X0	1Y	— ALU_B2	7
5	AND_B2 — 1X1			
4	OR_B2 — 1X2			
3	XOR_NOT_B2 — 1X3			
10	SUM_B3 — 2X0	2Y	— ALU_B3	9
11	AND_B3 — 2X1			
12	OR_B3 — 2X2			
13	XOR_NOT_B3 — 2X3			
14	ALU_0 — A			
2	ALU_1 — B			
1	1E			
15	2E			

74HC153

U31

Pin	Signal		Signal	Pin
6	SUM_B6 — 1X0	1Y	— ALU_B6	7
5	AND_B6 — 1X1			
4	OR_B6 — 1X2			
3	XOR_NOT_B6 — 1X3			
10	SUM_B7 — 2X0	2Y	— ALU_B7	9
11	AND_B7 — 2X1			
12	OR_B7 — 2X2			
13	XOR_NOT_B7 — 2X3			
14	ALU_0 — A			
2	ALU_1 — B			
1	1E			
15	2E			

74HC153

U33

Pin	Signal		Signal	Pin
2	ALU_B7 — A0	B0	BUS_7	18
3	ALU_B6 — A1	B1	BUS_6	17
4	ALU_B5 — A2	B2	BUS_5	16
5	ALU_B4 — A3	B3	BUS_4	15
6	ALU_B3 — A4	B4	BUS_3	14
7	ALU_B2 — A5	B5	BUS_2	13
8	ALU_B1 — A6	B6	BUS_1	12
9	ALU_B0 — A7	B7	BUS_0	11
19	$\overline{ALU\_OUT}$ — $\overline{CE}$			
1	AB/$\overline{BA}$			

74HC245

ALU_B0
ALU_B1
ALU_B2
ALU_B3
ALU_B4
ALU_B5
ALU_B6
ALU_B7

D36 D37 D38 D39 D40 D41 D42 D43

R40	R41	R42	R43	R44	R45	R46	R47
470R	470R	470R	470R	470R	470R	470R	470R

+5V +5V +5V +5V +5V

C36	C35	C32	C33	C34
100nF	100nF	100nF	100nF	100nF

U34

Pin	Label		Label	Pin	Net
10	A0		D0	11	RAM_IO0
9	A1		D1	12	RAM_IO1
8	A2		D2	13	RAM_IO2
7	A3		D3	15	RAM_IO3
6	A4		D4	16	RAM_IO4
5	A5		D5	17	RAM_IO5
4	A6		D6	18	RAM_IO5
3	A7		D7	19	RAM_IO7
25	A8				
24	A9				
21	A10				
23	A11				
2	A12				

ADDR_00 … ADDR_12

CE (20), CS (26), WE (27), OE (22)

6264

+5V

U35 74HC245

Pin	Label		Label	Pin	Net
2	A0		B0	18	BUS_7
3	A1		B1	17	BUS_6
4	A2		B2	16	BUS_5
5	A3		B3	15	BUS_4
6	A4		B4	14	BUS_3
7	A5		B5	13	BUS_2
8	A6		B6	12	BUS_1
9	A7		B7	11	BUS_0

RAM_IO7 … RAM_IO0

RAM_OUT — CE (19), AB/BA (1)

+5V

RAM_IO0, RAM_IO1, RAM_IO2, RAM_IO3, RAM_IO4, RAM_IO5, RAM_IO5, RAM_IO7

D59 D60 D61 D62 D63 D64 D65 D66

R80	R81	R82	R83	R84	R85	R86	R87
470R	470R	470R	470R	470R	470R	470R	470R

+5V +5V

C45 100nF   C46 100nF

U37 — 74HC157

Pin	Signal
2 MAR_DIP7	1A
3 MAR_B7	1B
5 MAR_DIP6	2A
6 MAR_B6	2B
11 MAR_DIP5	3A
10 MAR_B5	3B
14 MAR_DIP4	4A
13 MAR_B4	4B
1 $\overline{PROGRAMM} \mid RUN$	$\overline{A}/B$
15	E

1Y 4 → ADDR_07
2Y 7 → ADDR_06
3Y 9 → ADDR_05
4Y 12 → ADDR_04

U38 — 74HC157

Pin	Signal
2 MAR_DIP3	1A
3 MAR_B3	1B
5 MAR_DIP2	2A
6 MAR_B2	2B
11 MAR_DIP1	3A
10 MAR_B1	3B
14 MAR_DIP0	4A
13 MAR_B0	4B
1 $\overline{PROGRAMM} \mid RUN$	$\overline{A}/B$
15	E

1Y 4 → ADDR_03
2Y 7 → ADDR_02
3Y 9 → ADDR_01
4Y 12 → ADDR_00

U39 — 74HC173

BUS_7 14 D0   Q0 3 → MAR_B7
BUS_6 13 D1   Q1 4 → MAR_B6
BUS_5 12 D2   Q2 5 → MAR_B5
BUS_4 11 D3   Q3 6 → MAR_B4
CLOCK 7 CLK
1 $\overline{OE1}$
2 $\overline{OE2}$
$\overline{MAR\_IN}$ 9 E1
10 E2
RESET 15 MR

U40 — 74HC173

BUS_3 14 D0   Q0 3 → MAR_B3
BUS_2 13 D1   Q1 4 → MAR_B2
BUS_1 12 D2   Q2 5 → MAR_B1
BUS_0 11 D3   Q3 6 → MAR_B0
CLOCK 7 CLK
1 $\overline{OE1}$
2 $\overline{OE2}$
$\overline{MAR\_IN}$ 9 E1
10 E2
RESET 15 MR

Switch / LEDs

+5V
+5V
R48 470R
D45 PROGRAMM
SW2 SW-SPDT
$\overline{PROGRAMM} \mid RUN$
D44 RUN
R49 470R

DSW3 — DIPSW_8

MAR_DIP7
MAR_DIP6
MAR_DIP5
MAR_DIP4
MAR_DIP3
MAR_DIP2
MAR_DIP1
MAR_DIP0

Address LEDs

ADDR_00
ADDR_01
ADDR_02
ADDR_03
ADDR_04
ADDR_05
ADDR_06
ADDR_07
ADDR_08
ADDR_09
ADDR_10
ADDR_11
ADDR_12

D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58
R50 470R	R51 470R	R52 470R	R53 470R	R54 470R	R55 470R	R56 470R	R57 470R	R75 470R	R76 470R	R77 470R	R78 470R	R79 470R

Decoupling

+5V +5V +5V +5V
C40 100nF   C39 100nF   C37 100nF   C38 100nF

+5V

R74
10k

WR_BUTTON

U41
74HC157

DATA_7	BUS_7	1A
DATA_6	BUS_6	2A
DATA_5	BUS_5	3A
DATA_4	BUS_4	4A

1Y → RAM_IO7
2Y → RAM_IO6
3Y → RAM_IO5
4Y → RAM_IO4

PROGRAMM | RUN A/B
E

U42
74HC157

DATA_3	BUS_3	1A
DATA_2	BUS_2	2A
DATA_1	BUS_1	3A
DATA_0	BUS_0	4A

1Y → RAM_IO3
2Y → RAM_IO2
3Y → RAM_IO1
4Y → RAM_IO0

PROGRAMM | RUN A/B
E

+5V

DSW2
DIPSW_8

DATA_7
DATA_6
DATA_5
DATA_4
DATA_3
DATA_2
DATA_1
DATA_0

U36:A
74LS00

RAM_IN
CLOCK

U36:B
74LS00

U43:A
74LS00

WE

U36:C
74LS00

PROGRAMM | RUN

U36:D
74LS00

WR_BUTTON

+5V   +5V   +5V   +5V

C44   C43   C41   C42
100nF 100nF 100nF 100nF

TITLE:
8 Bits Computer
Memory Address Register - Data

DATE:
25/04/2021

PAGE:
13/19

BY: Tec. Vinicius Moraes   REV: @REV

+5V

+5V

RESET

RESET

CICLE_RESET

U44:A
1
2
3
74HC00

U44:B
4
5
6
74HC00

U44:C
10
9
8
74HC00

U44:D
13
12
11
74HC00

CICLE_END

R88
10k

C47
100nF

U45

BUS_7	14	D0	Q0	3	OUT_B7
BUS_6	13	D1	Q1	4	OUT_B6
BUS_5	12	D2	Q2	5	OUT_B5
BUS_4	11	D3	Q3	6	OUT_B4

CLOCK 7 CLK
1 OE1
2 OE2
OPR_IN 9 E1
10 E2
RESET 15 MR

74HC173

U46

BUS_3	14	D0	Q0	3	OUT_B3
BUS_2	13	D1	Q1	4	OUT_B2
BUS_1	12	D2	Q2	5	OUT_B1
BUS_0	11	D3	Q3	6	OUT_B0

CLOCK 7 CLK
1 OE1
2 OE2
OPR_IN 9 E1
10 E2
RESET 15 MR

74HC173

OUT_B0
OUT_B1
OUT_B2
OUT_B3
OUT_B4
OUT_B5
OUT_B6
OUT_B7

D67 D68 D69 D70 D71 D72 D73 D74

R89 R90 R91 R92 R93 R94 R95 R96
470R 470R 470R 470R 470R 470R 470R 470R

+5V +5V

C48 C49
100nF 100nF

TITLE:
8 Bits Computer
Output Register

DATE:
25/04/2021

PAGE:
15/19

BY: Tec. Vinicius Moraes

REV: @REV

FEC_B0
FEC_B1
FEC_B2

D75 D76 D77

R97 R98 R99
470R 470R 470R

+5V   +5V

U48   U47
3 D0   Q0 14 FEC_B0   1 A   Y0 15 T0
4 D1   Q1 13 FEC_B1   2 B   Y1 14 T1
5 D2   Q2 12 FEC_B2   3 C   Y2 13 T2
6 D3   Q3 11   Y3 12 T3
         RCO 15   Y4 11 T4
7 ENP   6 E1   Y5 10 T5
10 ENT   4 E2   Y6 9   T6
2 CLK   5 E3   Y7 7   CYCLE_END
9 LOAD   74HC138
CLOCK
1 MR
CYCLE_RESET
74HC161

+5V +5V +5V +5V +5V +5V +5V

R100 R101 R102 R103 R104 R105 R106
470R 470R 10k   470R 470R 470R 470R

D78 D79 D80 D81 D82 D83 D84

T0
T1
T2
T3
T4
T5
T6

+5V +5V

C50   C51
100nF 100nF

TITLE:
8 Bits Computer
Control - Fetch Execution Counter

DATE:
25/04/2021
PAGE:
16/19

BY: Tec. Vinicius Moraes   REV: @REV

U49:A — MAR_IN — 1 — 2 — $\overline{MAR\_IN}$ — 74HC04
U50:C — JMP — 5 — 6 — $\overline{JMP}$ — 74HC04
U49:B — RAM_OUT — 3 — 4 — $\overline{RAM\_OUT}$ — 74HC04
U50:D — PC_OUT — 13 — 12 — $\overline{PC\_OUT}$ — 74HC04
U49:C — IR_IN — 5 — 6 — $\overline{IR\_IN}$ — 74HC04
U50:E — IR_OUT — 11 — 10 — $\overline{IR\_OUT}$ — 74HC04
U49:D — ACC_OUT — 13 — 12 — $\overline{ACC\_OUT}$ — 74HC04
U50:F — BR_IN — 9 — 8 — $\overline{BR\_IN}$ — 74HC04
U50:A — ACC_IN — 1 — 2 — $\overline{ACC\_IN}$ — 74HC04
U51:A — OPR_IN — 1 — 2 — $\overline{OPR\_IN}$ — 74HC04
U50:B — ALU_OUT — 3 — 4 — $\overline{ALU\_OUT}$ — 74HC04

HLT
PC_INC
JMP
PC_OUT
MAR_IN
RAM_IN
RAM_OUT
$\overline{IR\_IN}$
IR_OUT
ACC_IN
ACC_OUT
BR_IN
ALU_1
ALU_0
$\overline{ADD}$ | SUB
$\overline{XOR}$ | NOT
ALU_OUT
OPR_IN

R107 470R, R108 470R, R109 470R, R110 470R, R111 470R, R112 470R, R113 470R, R114 470R, R115 470R, R116 470R, R117 470R, R124 470R, R123 470R, R122 470R, R121 470R, R120 470R, R119 470R, R118 470R

U52

Pin	Signal		Pin	Signal

FEC_B0 — 10 — A0   D0 — 11 — IR_IN
FEC_B1 — 9 — A1   D1 — 12 — RAM_OUT
FEC_B2 — 8 — A2   D2 — 13 — RAM_IN
I_REG_B0 — 7 — A3   D3 — 15 — MAR_IN
I_REG_B1 — 6 — A4   D4 — 16 — PC_OUT
I_REG_B2 — 5 — A5   D5 — 17 — JMP
I_REG_B3 — 4 — A6   D6 — 18 — PC_INC
I_REG_B4 — 3 — A7   D7 — 19 — HLT
I_REG_B5 — 25 — A8
I_REG_B6 — 24 — A9
I_REG_B7 — 21 — A10
23 — A11
2 — A12

20 — $\overline{CE}$ RDY/$\overline{B}$ — 1
22 — $\overline{OE}$
27 — $\overline{WE}$

2864

U53

FEC_B0 — 10 — A0   D0 — 11 — $\overline{XOR}$ | NOT
FEC_B1 — 9 — A1   D1 — 12 — ALU_OUT
FEC_B2 — 8 — A2   D2 — 13 — ALU_0
I_REG_B0 — 7 — A3   D3 — 15 — ALU_1
I_REG_B1 — 6 — A4   D4 — 16 — $\overline{ADD}$ | SUB
I_REG_B2 — 5 — A5   D5 — 17 — ACC_IN
I_REG_B3 — 4 — A6   D6 — 18 — ACC_OUT
I_REG_B4 — 3 — A7   D7 — 19 — IR_OUT
I_REG_B5 — 25 — A8
I_REG_B6 — 24 — A9
I_REG_B7 — 21 — A10
23 — A11
2 — A12

20 — $\overline{CE}$ RDY/$\overline{B}$ — 1
22 — $\overline{OE}$
27 — $\overline{WE}$

2864

U54

FEC_B0 — 10 — A0   D0 — 11
FEC_B1 — 9 — A1   D1 — 12
FEC_B2 — 8 — A2   D2 — 13
I_REG_B0 — 7 — A3   D3 — 15
I_REG_B1 — 6 — A4   D4 — 16
I_REG_B2 — 5 — A5   D5 — 17
I_REG_B3 — 4 — A6   D6 — 18
I_REG_B4 — 3 — A7   D7 — 19
I_REG_B5 — 25 — A8
I_REG_B6 — 24 — A9
I_REG_B7 — 21 — A10
23 — A11
2 — A12

20 — $\overline{CE}$ RDY/$\overline{B}$ — 1
22 — $\overline{OE}$
27 — $\overline{WE}$

2864

TITLE:
8 Bits Computer
Control - Decoder

DATE: 25/04/2021
PAGE: 18/19

BY: Tec. Vinicius Moraes   REV: @REV

J1
CONN-SIL10

+5V

U59
JOY1_START 14 — D0   Q0 3 — JOY1_B7
JOY1_SELECT 13 — D1   Q1 4 — JOY1_B6
JOY1_UP   12 — D2   Q2 5 — JOY1_B5
JOY1_DOWN   11 — D3   Q3 6 — JOY1_B4
CLOCK   7 — CLK
             1 — OE1
             2 — OE2
JOY1_IN   9 — E1
            10 — E2
RESET   15 — MR
74HC173

U61
+5V
2 — A0   B0 — 18 BUS 7
3 — A1   B1 — 17 BUS 6
4 — A2   B2 — 16 BUS 5
5 — A3   B3 — 15 BUS 4
6 — A4   B4 — 14 BUS 3
7 — A5   B5 — 13 BUS 2
8 — A6   B6 — 12 BUS 1
9 — A7   B7 — 11 BUS 0
19 — CE
1 — AB/BA
74HC245

U60
JOY1_LEFT 14 — D0   Q0 3 — JOY1_B3
JOY1_RIGHT 13 — D1   Q1 4 — JOY1_B2
JOY1_A   12 — D2   Q2 5 — JOY1_B1
JOY1_B   11 — D3   Q3 6 — JOY1_B0
CLOCK   7 — CLK
            1 — OE1
            2 — OE2
JOY1_IN   9 — E1
           10 — E2
RESET   15 — MR
74HC173
JOY1_OUT

J2
CONN-SIL10

+5V

U62
JOY2_START 14 — D0   Q0 3 — JOY2_B7
JOY2_SELECT 13 — D1   Q1 4 — JOY2_B6
JOY2_UP   12 — D2   Q2 5 — JOY2_B5
JOY2_DOWN   11 — D3   Q3 6 — JOY2_B4
CLOCK   7 — CLK
             1 — OE1
             2 — OE2
JOY2_IN   9 — E1
            10 — E2
RESET   15 — MR
74HC173

U64
+5V
2 — A0   B0 — 18 BUS 7
3 — A1   B1 — 17 BUS 6
4 — A2   B2 — 16 BUS 5
5 — A3   B3 — 15 BUS 4
6 — A4   B4 — 14 BUS 3
7 — A5   B5 — 13 BUS 2
8 — A6   B6 — 12 BUS 1
9 — A7   B7 — 11 BUS 0
19 — CE
1 — AB/BA
74HC245

U63
JOY2_LEFT 14 — D0   Q0 3 — JOY2_B3
JOY2_RIGHT 13 — D1   Q1 4 — JOY2_B2
JOY2_A   12 — D2   Q2 5 — JOY2_B1
JOY2_B   11 — D3   Q3 6 — JOY2_B0
CLOCK   7 — CLK
            1 — OE1
            2 — OE2
JOY2_IN   9 — E1
           10 — E2
RESET   15 — MR
74HC173
JOY2_OUT

TITLE:
8 Bits Computer
I/O - Joysticks
BY: Tec. Vinicius Moraes
DATE: 25/04/2021
PAGE: 19/19
REV: @REV